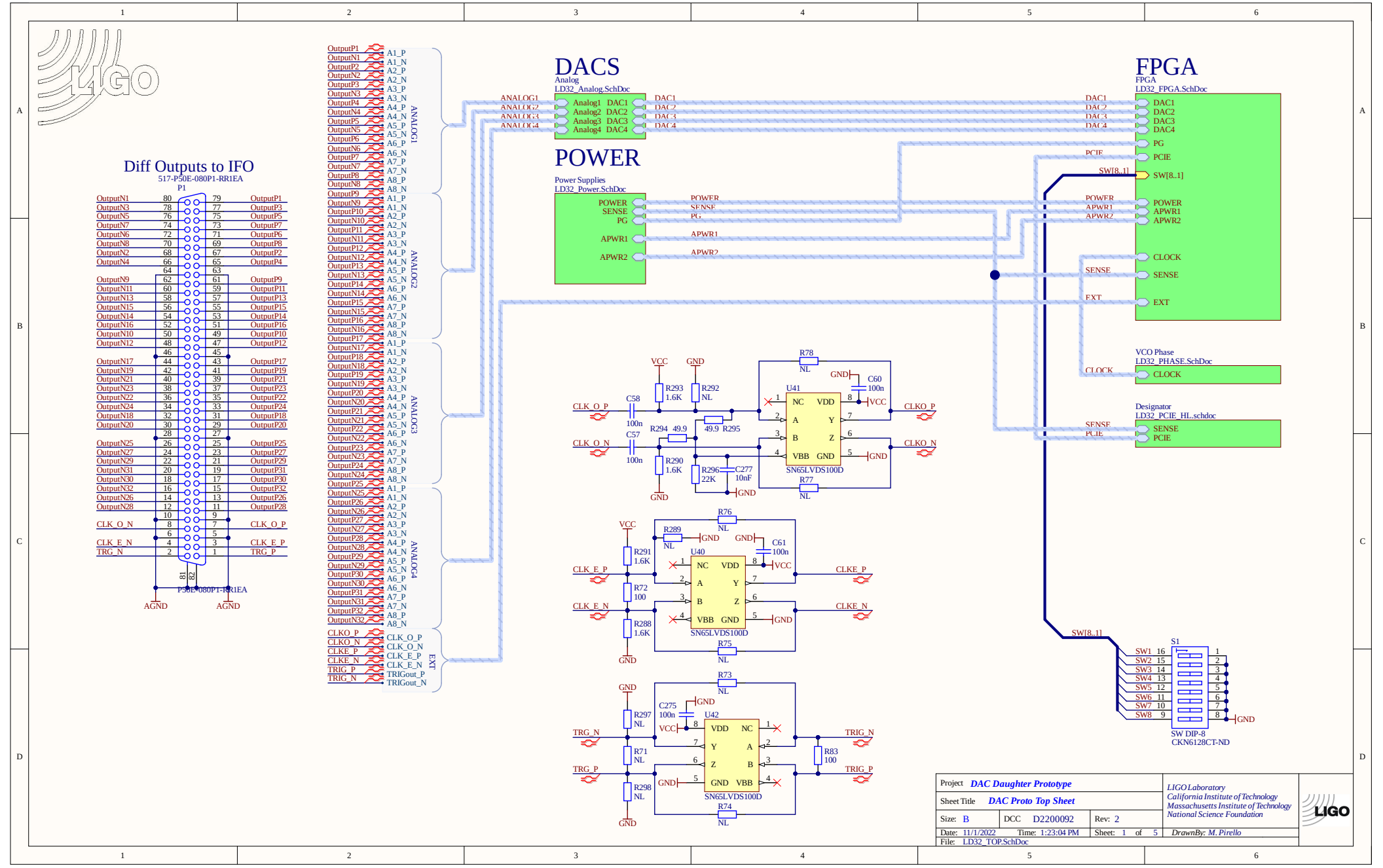
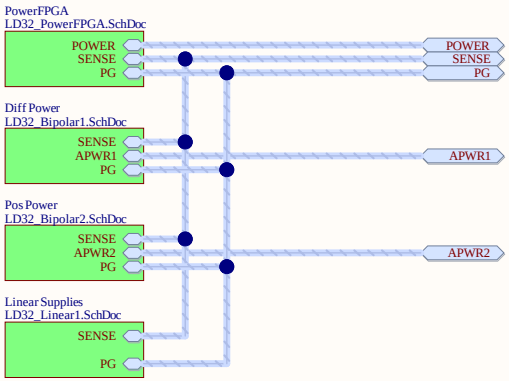

Diff Outputs to IFO
517-P50E-080P1-RR1EA
P1
AGND
AGND
DACS
Analog
LD32_Analog.SchDoc
POWER
Power Supplies
LD32_Power.SchDoc
FPGA
FPGA
LD32_FPGA.SchDoc
VCO Phase
LD32_PHASE.SchDoc
Designator
LD32_PCIE_HL.schdoc
SN65LVDS100D
SW DIP-8
CKN6128CT-ND
Project DAC Daughter Prototype
Sheet Title DAC Proto Top Sheet
Size: B
DCC D2200092
Rev: 2
Date: 11/1/2022
Time: 1:23:04 PM
Sheet: 1 of 5
File: LD32_TOP.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

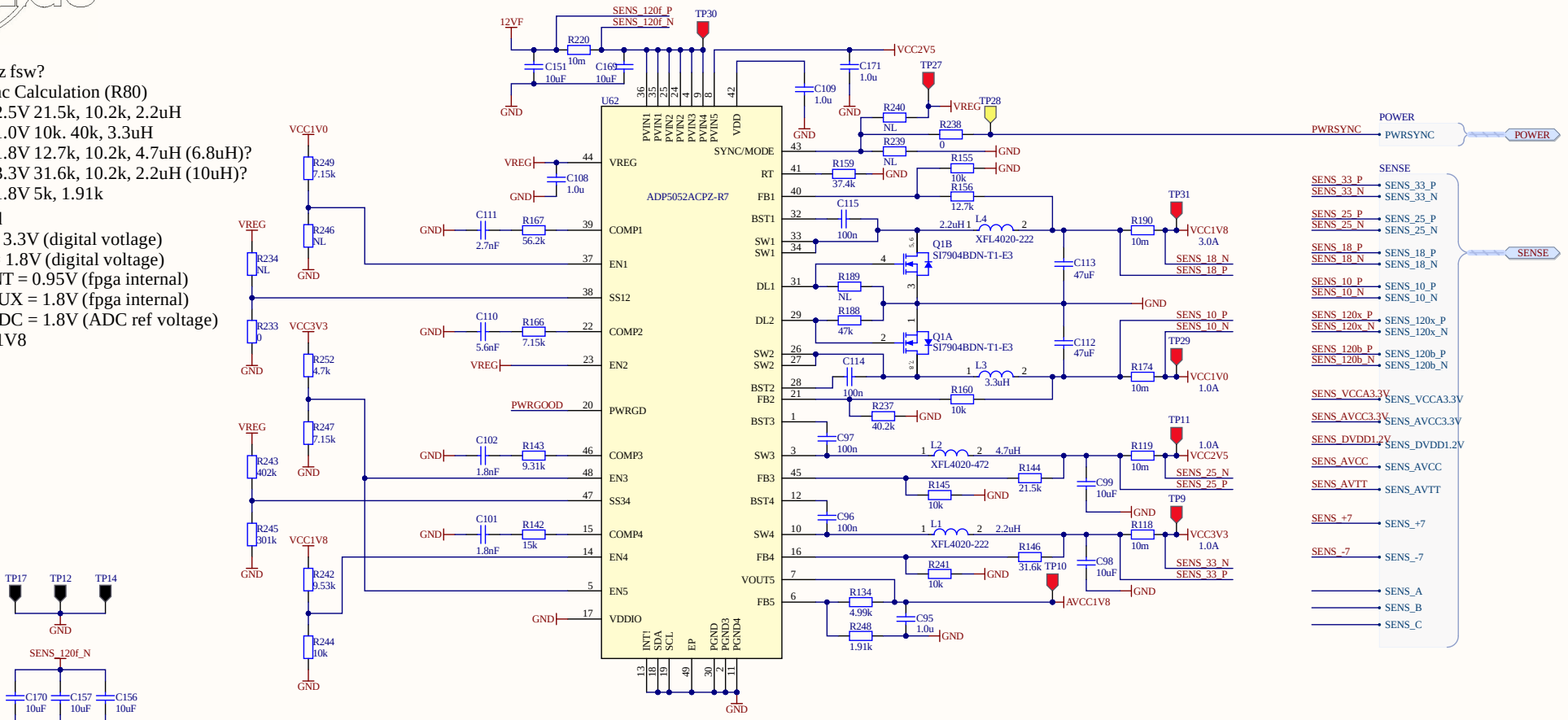


Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Top Sheet***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022 Time: 1:23:04 PM		Sheet: 1 of 5	*DrawnBy: M. Pirello*
File: LD32_Power.SchDoc			

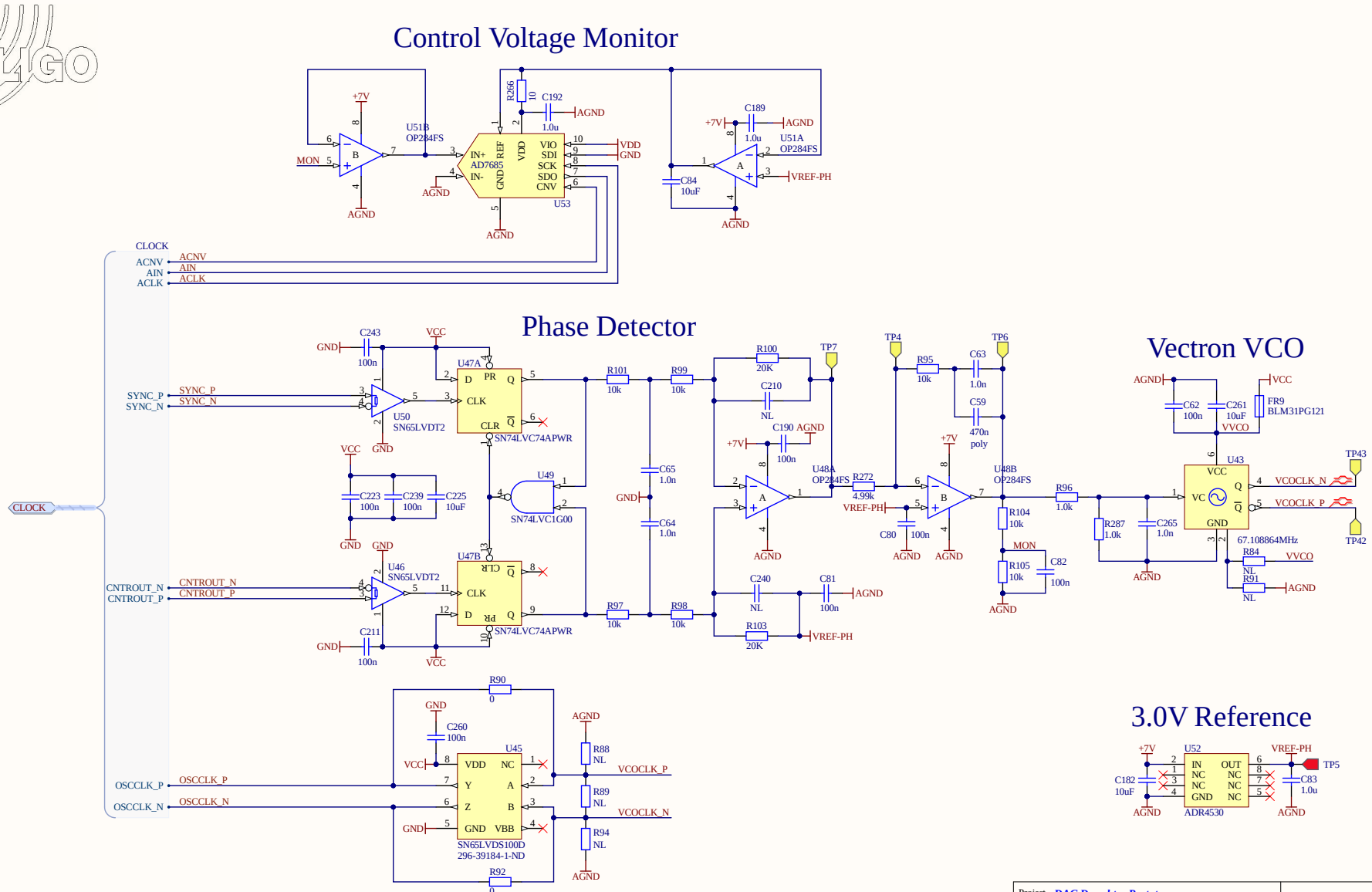
Switched FPGA Power

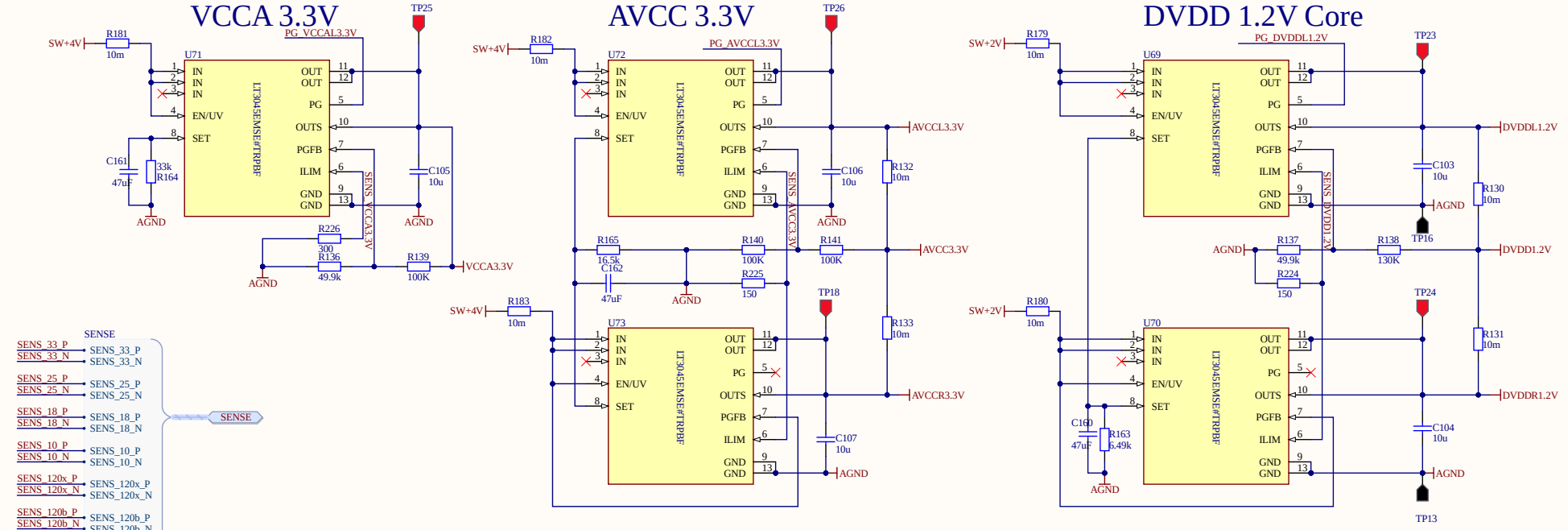
600kHz fsw?
RT Sync Calculation (R80)
FB1 - 2.5V 21.5k, 10.2k, 2.2uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 1.8V 12.7k, 10.2k, 4.7uH (6.8uH)?
FB4 - 3.3V 31.6k, 10.2k, 2.2uH (10uH)?
FB5 - 1.8V 5k, 1.91k

Legend
VCC = 3.3V (digital votlage)
VDD = 1.8V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8



Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto Dual Analog Supply*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:06 PM	Sheet: 2 of 19	*DrawnBy: M. Pirello*
File: LD32_PowerFPGA.SchDoc			


Control Voltage Monitor
Phase Detector
Vectron VCO
3.0V Reference
Optional LVPECL-LVDS Translator
U51B OP284FS
U51A OP284FS
U53 AD7685
U50 SN65LVDT2
U46 SN65LVDT2
U47A SN74LVC74APWR
U47B SN74LVC74APWR
U49 SN74LVC1G00
U48A OP284FS
U48B OP284FS
U43 67.108864MHz
U45 SN65LVDS100D
296-39184-1-ND
U52 ADR4530
CLOCK
ACNV
AIN
ACLK
SYNC_P
SYNC_N
CNTROUT_N
CNTROUT_P
OSCCLK_P
OSCCLK_N
VCOCLK_P
VCOCLK_N
MON
VREF-PH
AGND
GND
VCC
+7V
VDD
VVCO
Project DAC Daughter Prototype
Sheet Title VCO & Phase Detector
Size: B
DCC D2200092
Rev: 2
Date: 11/1/2022
Time: 1:23:07 PM
Sheet: 2 of 12
File: LD32_PHASE.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello



SENSE

SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N
SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N
SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N
SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N
SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N
SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N
SENS_VCCA3.3V → SENS_VCCA3.3V
SENS_AVCC3.3V → SENS_AVCC3.3V
SENS_DVDD1.2V → SENS_DVDD1.2V
SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT
SENS_+7 → SENS_+7
SENS_-7 → SENS_-7
SENS_A
SENS_B
SENS_C

→ SENSE

LT3045-1 Configs:
VCCA3V3
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

AVCC3V3:
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

LT3045-1 Configs:
DVDD1V2:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

POWER GOOD

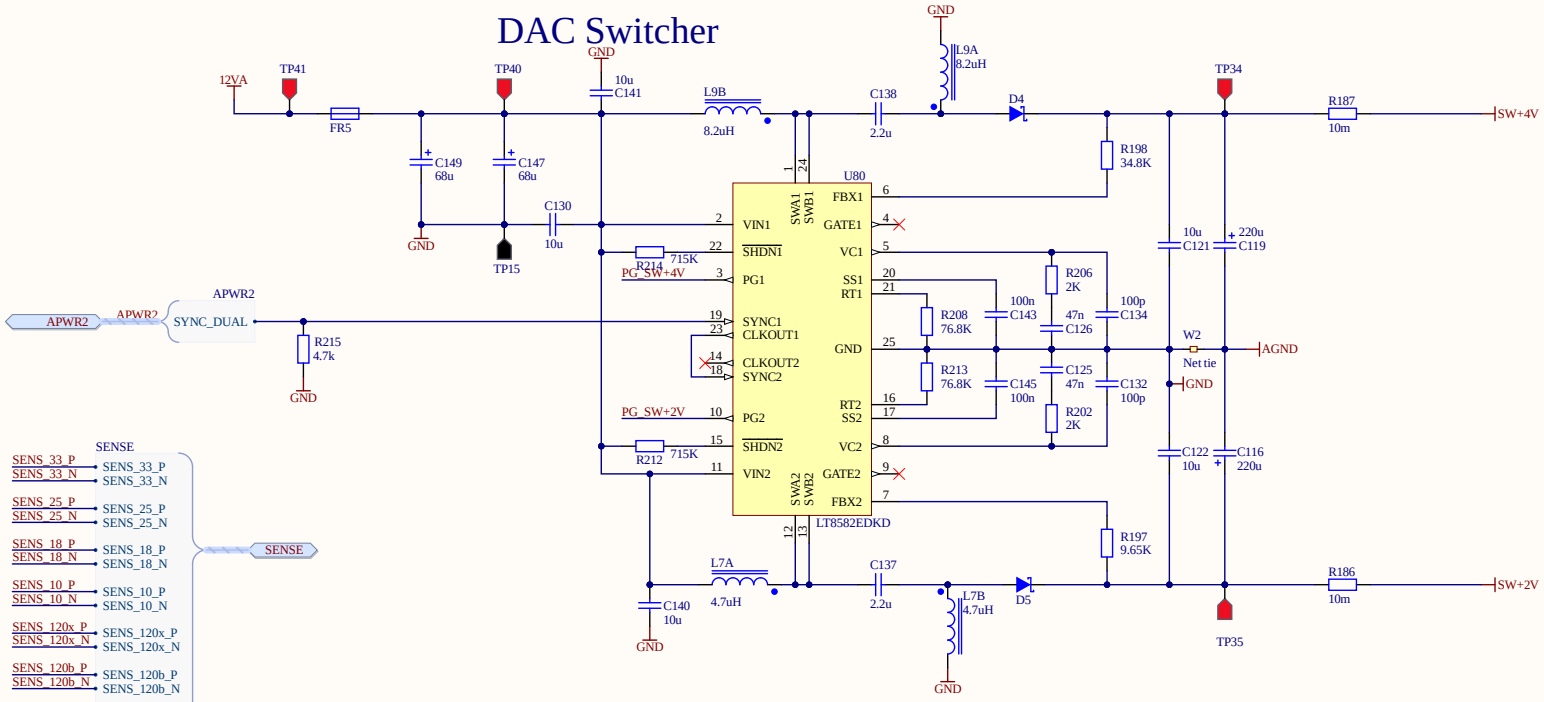
PG_VCCAL3.3V → PG_VCCAL3.3V
PG_AVCCL3.3V → PG_AVCCL3.3V
PG_DVDDL1.2V → PG_DVDDL1.2V
PG_SW+2V → PG_SW+2V
PG_SW+4V → PG_SW+4V
PWRGOOD → PG_FPGA
PG_SW+8V → PG_SW+8
PG_SW-8V → PG_SW-8
PG-7 → PG_L-7v
PG+7 → PG_L+7v

→ PG

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto Linear Supplies*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:08 PM	Sheet: 2 of 19	*DrawnBy: M. Pirello*
File: LD32_Linear1.SchDoc			

Front End Power +/- 7V
QC per channel 5.5mA * 64 = 352mA so single supplies are sufficient
DVDD 1.2V 128 * 4 = 512mA > 500mA so two supplies
VCCA 3.3V one supply
AVDD 1.8V one suppply
AVCC_R 3.3V 90*4 = 360mA one supply
AVCC_L 3.3V 90*4 = 360mA one supply
VDD_R, VDD_L 3.3V 128 per DAC * 4 = 512mA > 500mA is two supplies

DAC Switcher



SENSE

SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N
SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N
SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N
SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N
SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N
SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N
SENS_VCCA3.3V → SENS_VCCA3.3V
SENS_AVCC3.3V → SENS_AVCC3.3V
SENS_DVDD1.2V → SENS_DVDD1.2V
SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT
SENS_+7 → SENS_+7
SENS_-7 → SENS_-7
SENS_A
SENS_B
SENS_C

→ SENSE

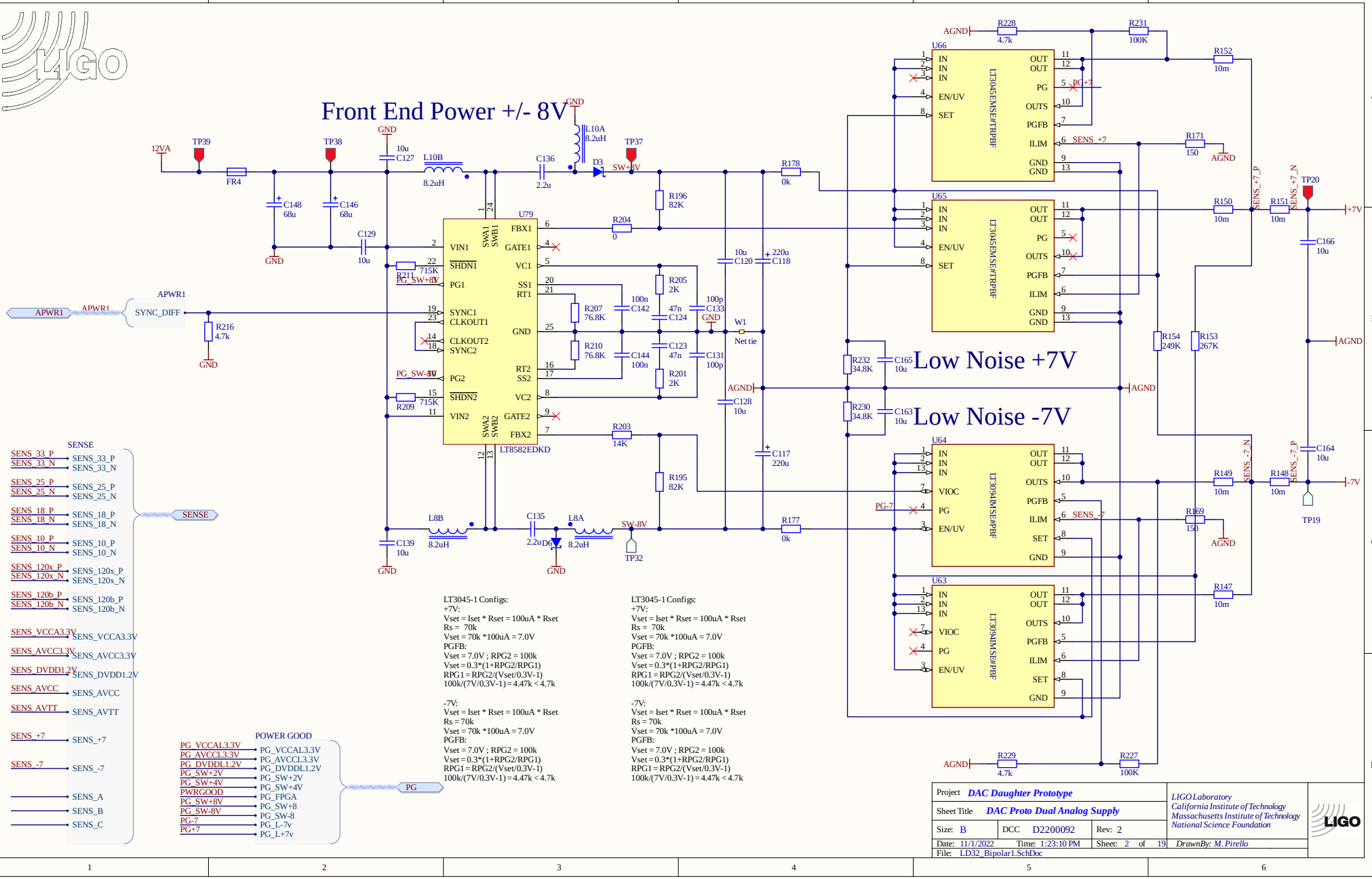
POWER GOOD

PG_VCCAL3.3V → PG_VCCAL3.3V
PG_AVCCL3.3V → PG_AVCCL3.3V
PG_DVDDL1.2V → PG_DVDDL1.2V
PG_SW+2V → PG_SW+2V
PG_SW+4V → PG_SW+4V
PWRGOOD → PG_FPGA
PG_SW+8V → PG_SW+8
PG_SW-8V → PG_SW-8
PG-7 → PG_L-7v
PG+7 → PG_L+7v

→ PG

Project	DAC Daughter Prototype		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	DAC Proto Dual Analog Supply		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022 Time: 1:23:09 PM	Sheet: 2 of 19	DrawnBy: M. Pirello	
File: LD32_Bipolar2.SchDoc			

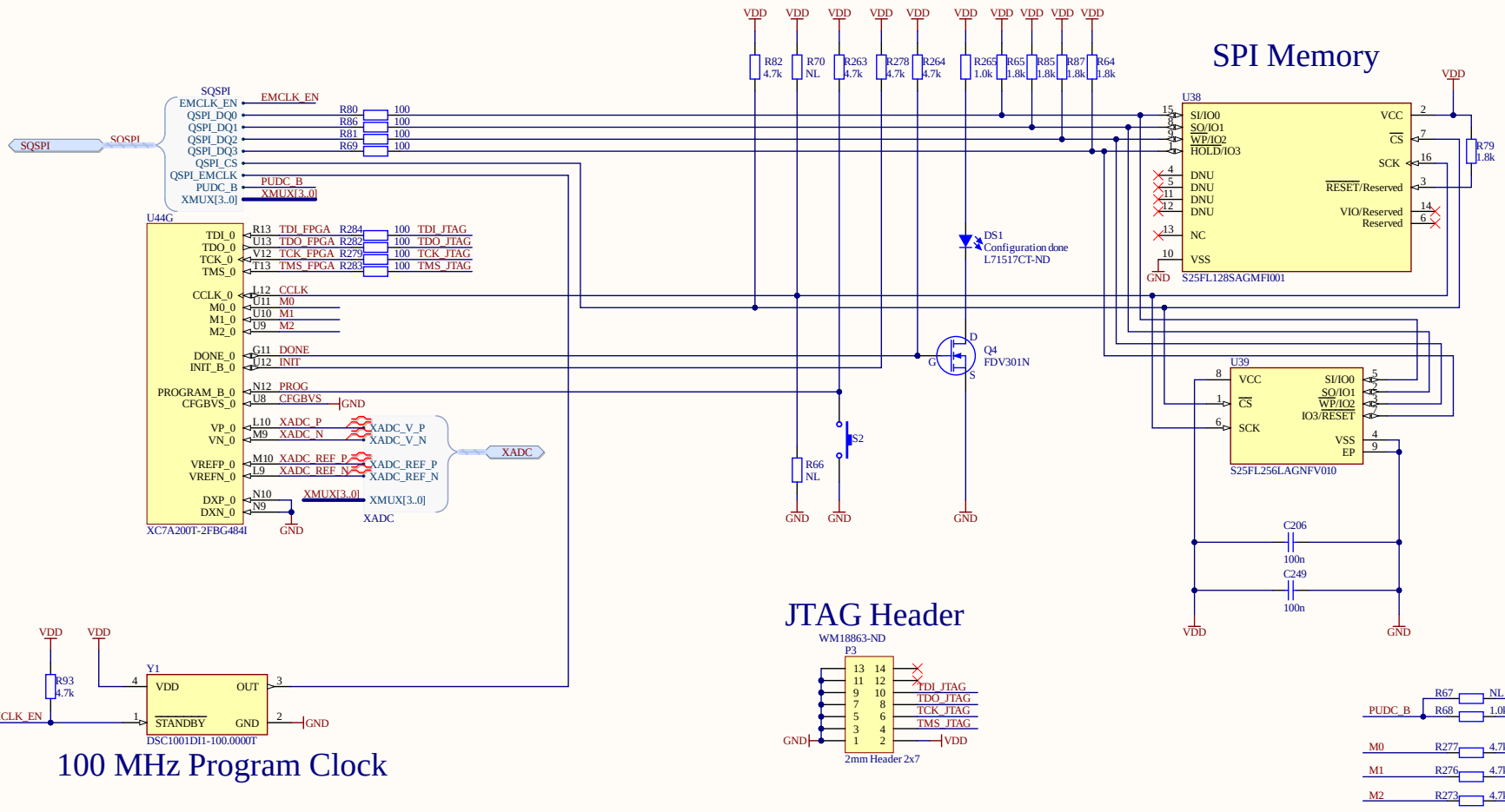
Front End Power +/- 8V



JTAG and SPI Flash

VDD is 1.8V for this design

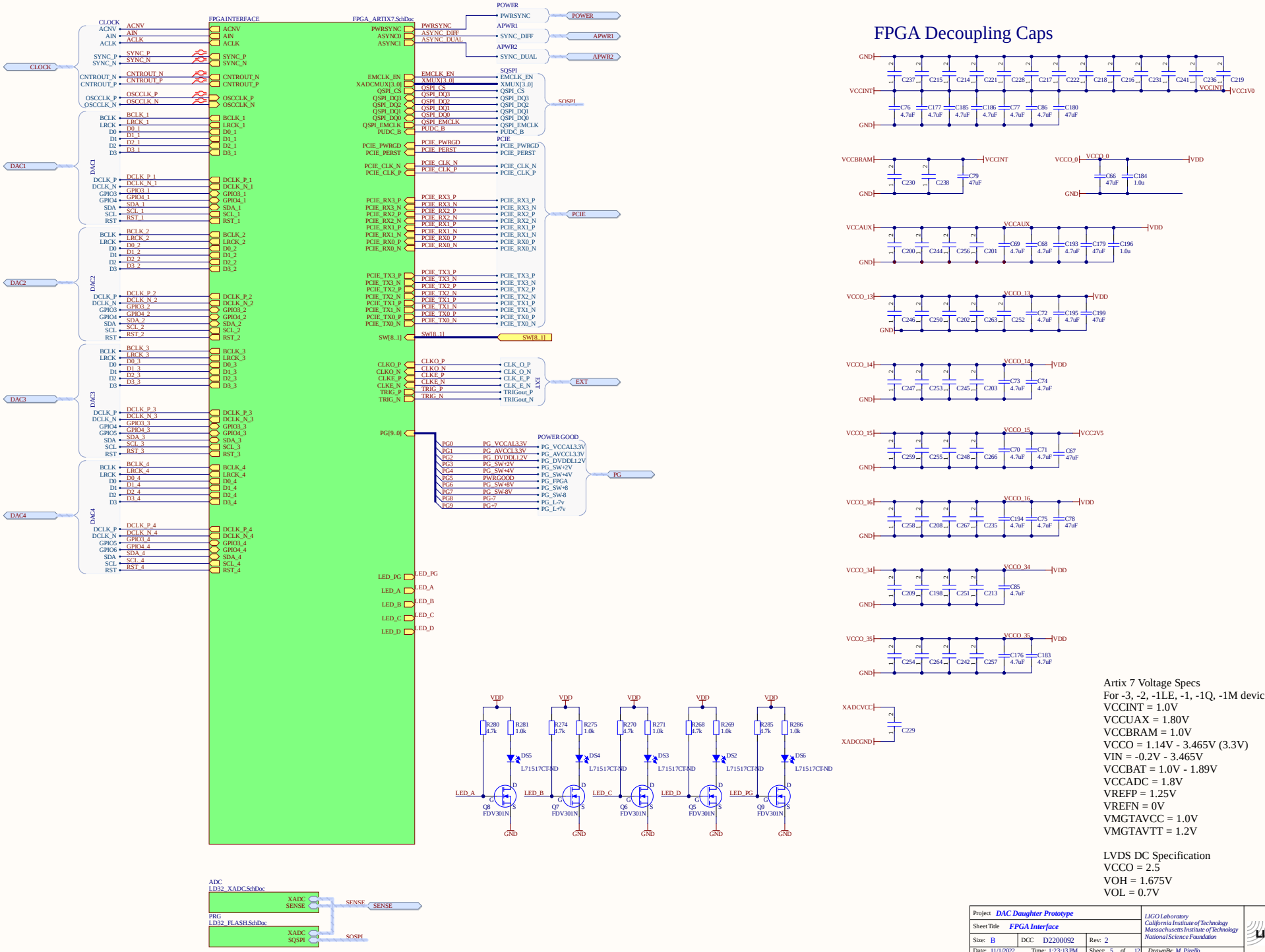
SPI Memory



JTAG Header

100 MHz Program Clock

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:11 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: LD32_FLASH.SchDoc			

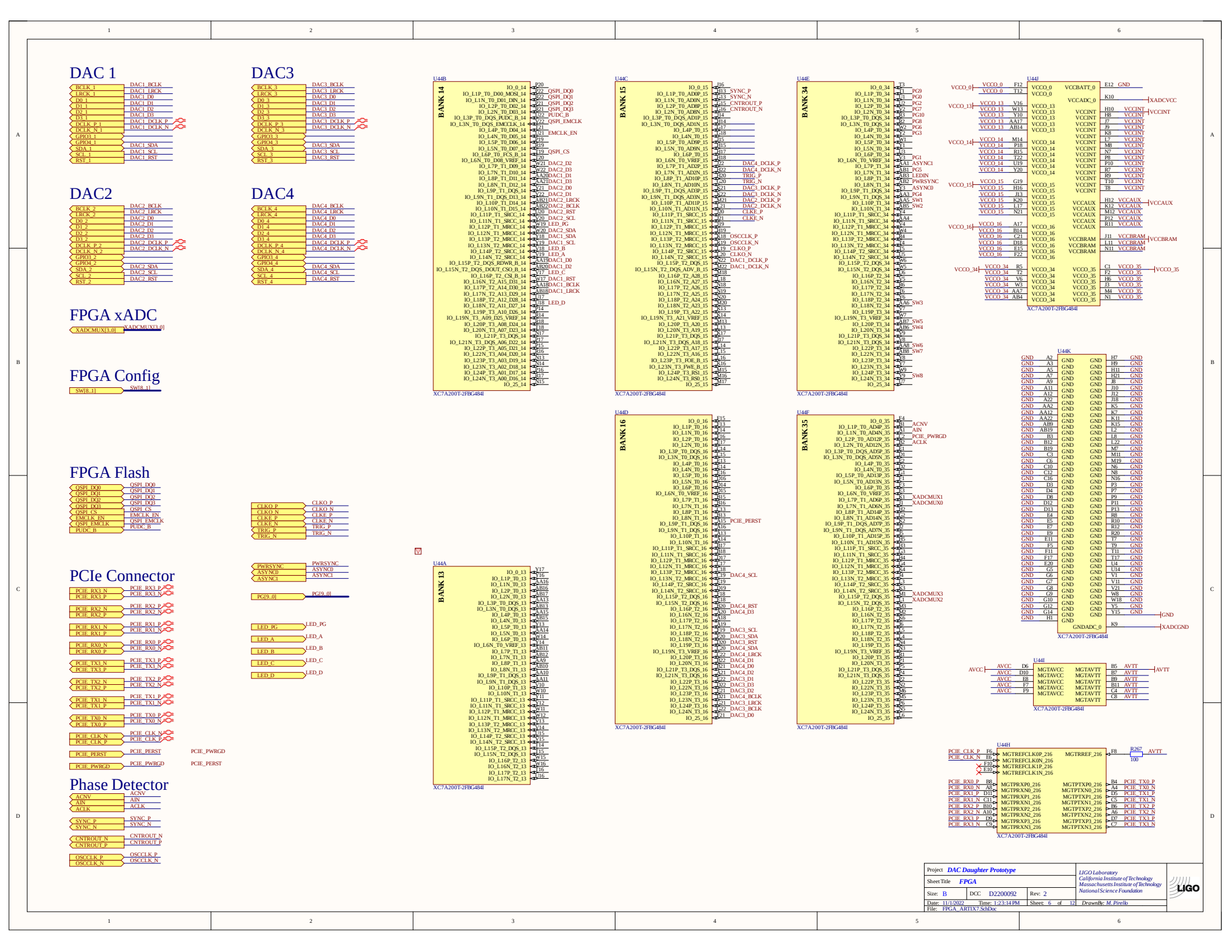


FPGA Decoupling Caps

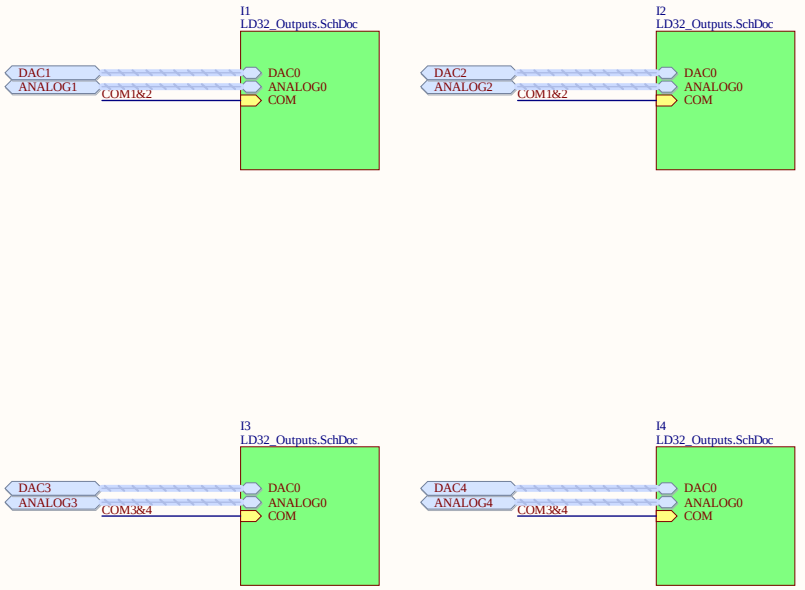
Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

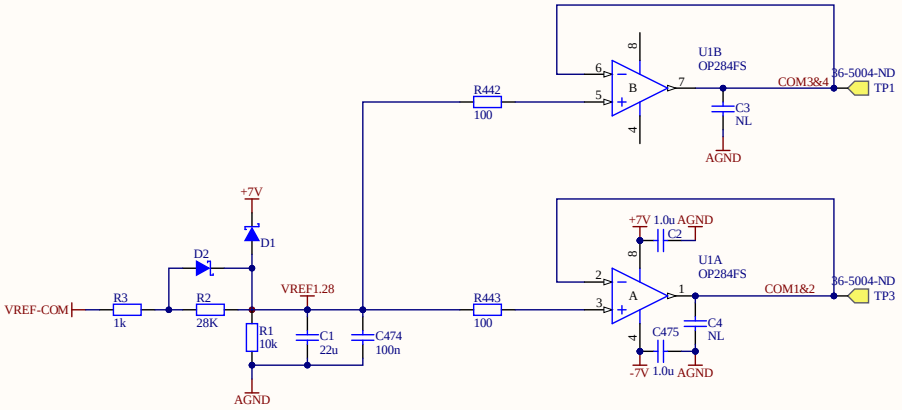
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Interface*		
Size: B	DCC: D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:13 PM	Sheet 5 of 12	*DrawnBy: M. Pirello*
File: LD32_FPGA.SchDoc			

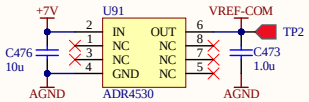

DAC 1
DAC3
DAC2
DAC4
FPGA xADC
FPGA Config
FPGA Flash
PCIe Connector
Phase Detector
BANK 14
BANK 15
BANK 34
BANK 16
BANK 35
BANK 13
XC7A200T-2FBG484I
Project DAC Daughter Prototype
Sheet Title FPGA
Size: B
DCC D2200092
Rev: 2
Date: 11/1/2022
Time: 1:23:14 PM
Sheet 6 of 12
File: FPGA_ARTIX7.SchDoc
DrawnBy: M.Pirello
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
LIGO

Multiple DAC's COM Distro





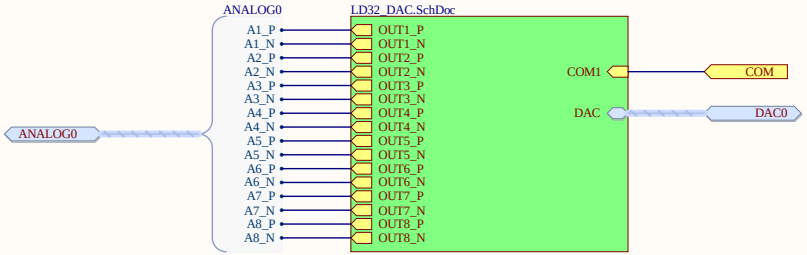
3.0V COM Reference



Parts Checked for Value and Consistency

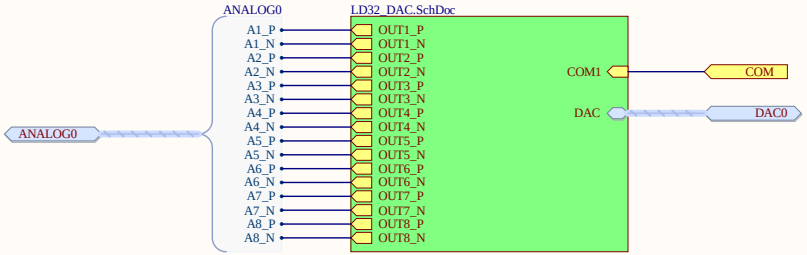
Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto DAC Outputs*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:15 PM	Sheet: 9 of 19	*DrawnBy: M. Pirello*
File: LD32_Analog.SchDoc			

DAC Overview



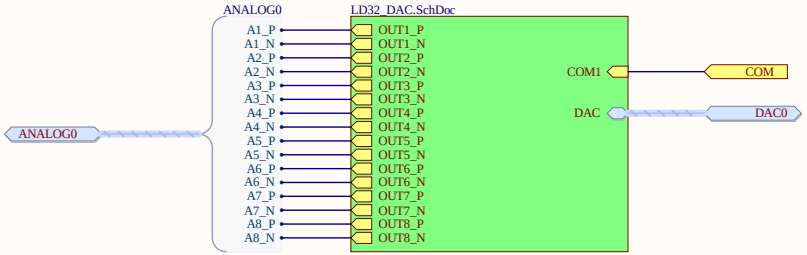
Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto DAC Outputs***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022 Time: 1:23:16 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello*
File: LD32_Outputs.SchDoc			

DAC Overview



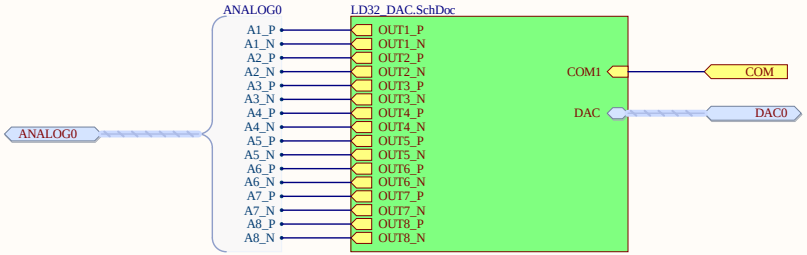
Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto DAC Outputs***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022 Time: 1:23:16 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello*
File: LD32_Outputs.SchDoc			

DAC Overview

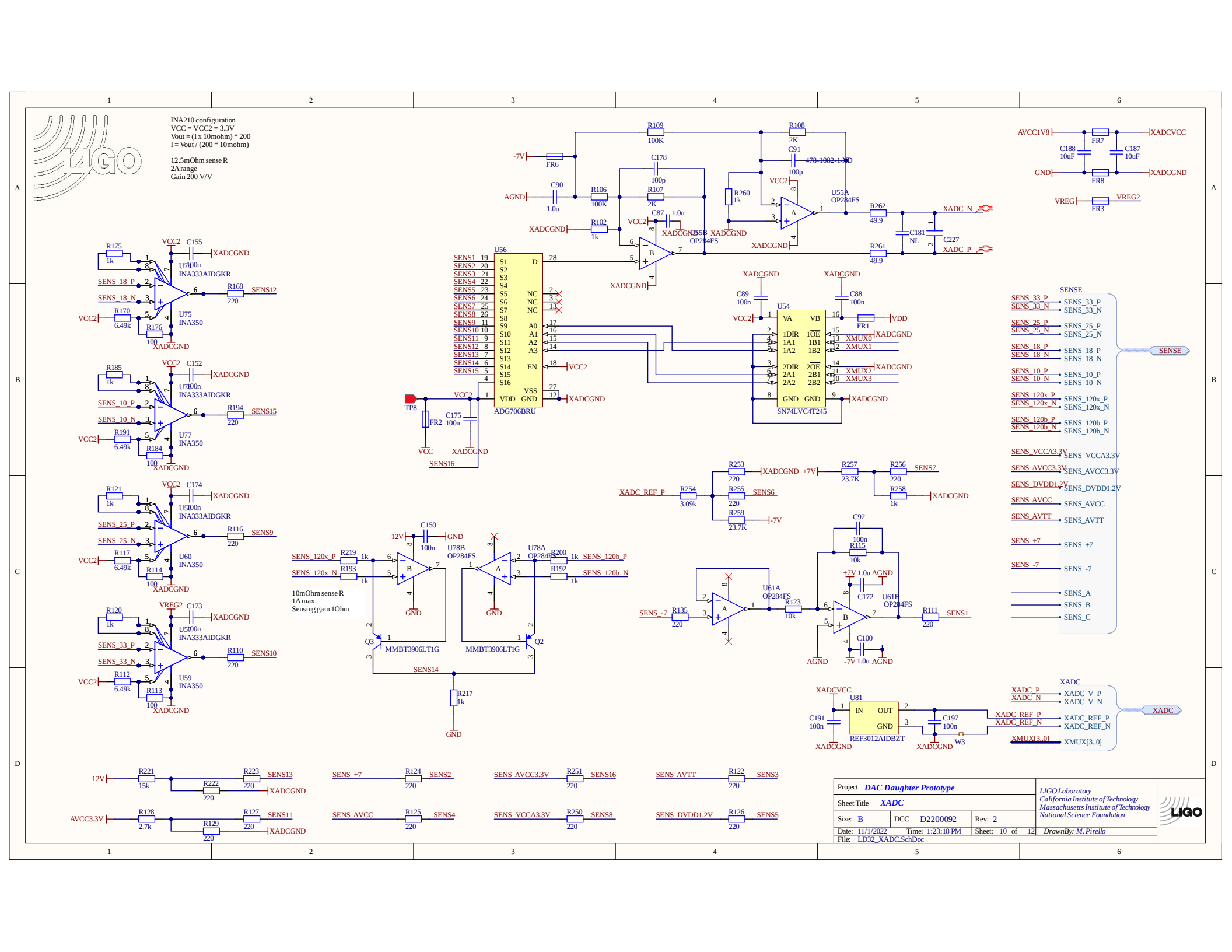


Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto DAC Outputs***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022 Time: 1:23:16 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello*
File: LD32_Outputs.SchDoc			

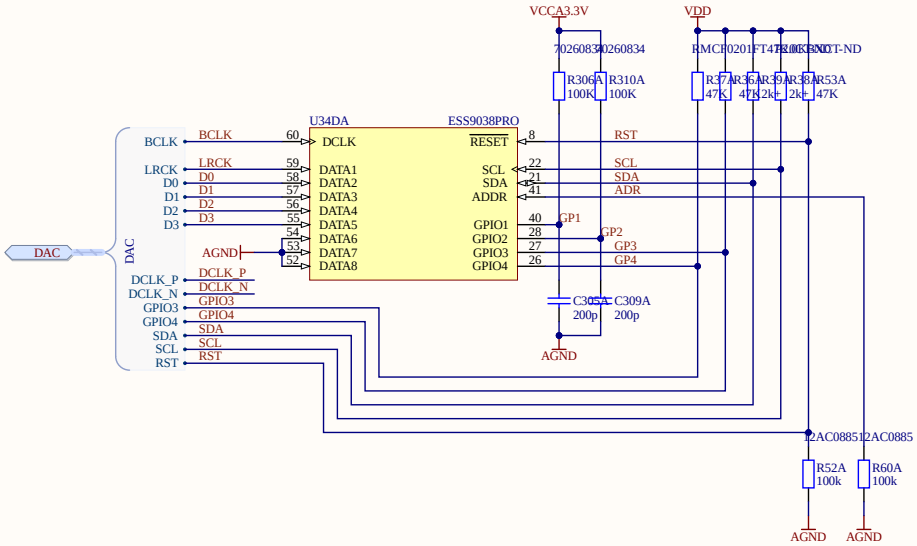
DAC Overview



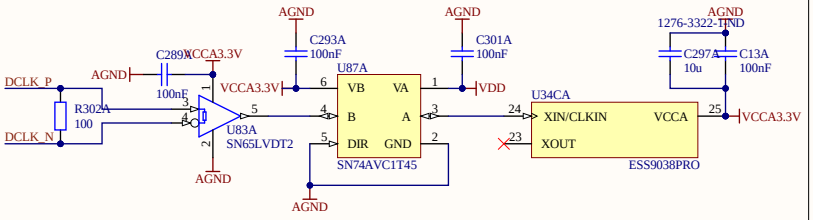
Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto DAC Outputs***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022 Time: 1:23:17 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello*
File: LD32_Outputs.SchDoc			


INA210 configuration
VCC = VCC2 = 3.3V
Vout = (I x 10mohm) * 200
I = Vout / (200 * 10mohm)
12.5mOhm sense R
2A range
Gain 200 V/V
U75 INA333AIDGKR
U77 INA333AIDGKR
U60 INA333AIDGKR
U59 INA333AIDGKR
INA350
U56 ADG706BRU
U54 SN74LVC4T245
U55A OP284FS
U55B OP284FS
U78B OP284FS
U78A OP284FS
U61A OP284FS
U61B OP284FS
Q3 MMBT3906LT1G
Q2 MMBT3906LT1G
U81 REF3012AIDBZT
10mOhm sense R
1A max
Sensing gain 1Ohm
SENSE
XADC
Project DAC Daughter Prototype
Sheet Title XADC
Size: B
DCC D2200092
Rev: 2
Date: 11/1/2022
Time: 1:23:18 PM
Sheet: 10 of 12
File: LD32_XADC.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

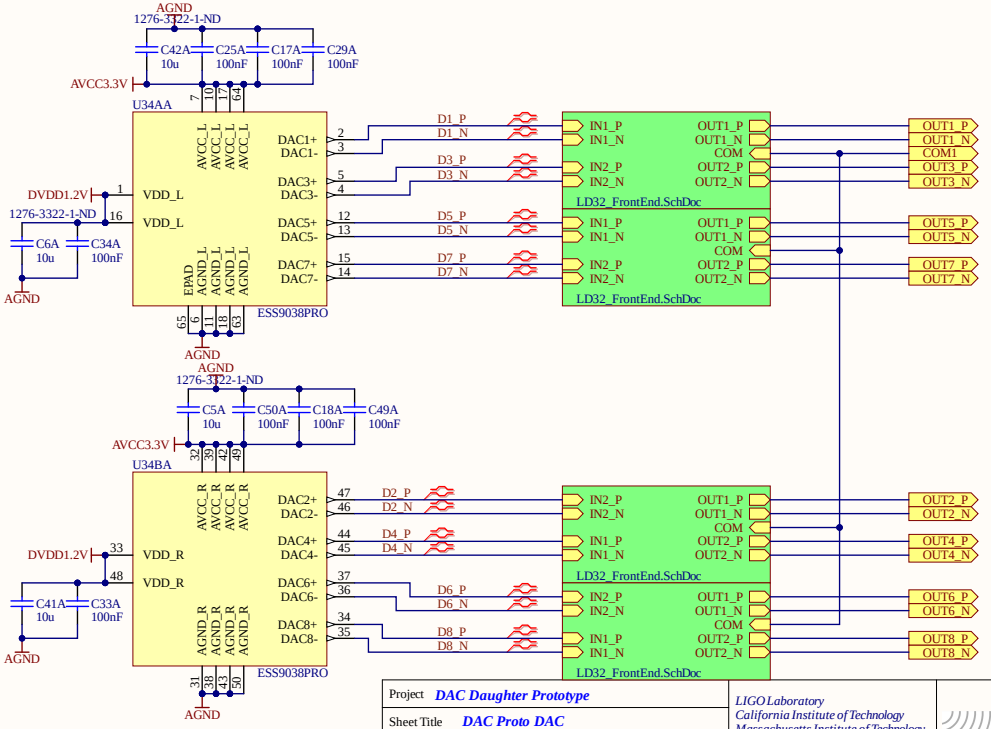
DAC Inputs



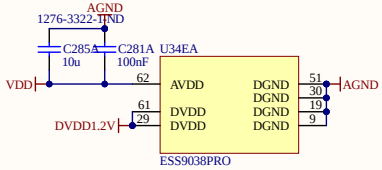
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

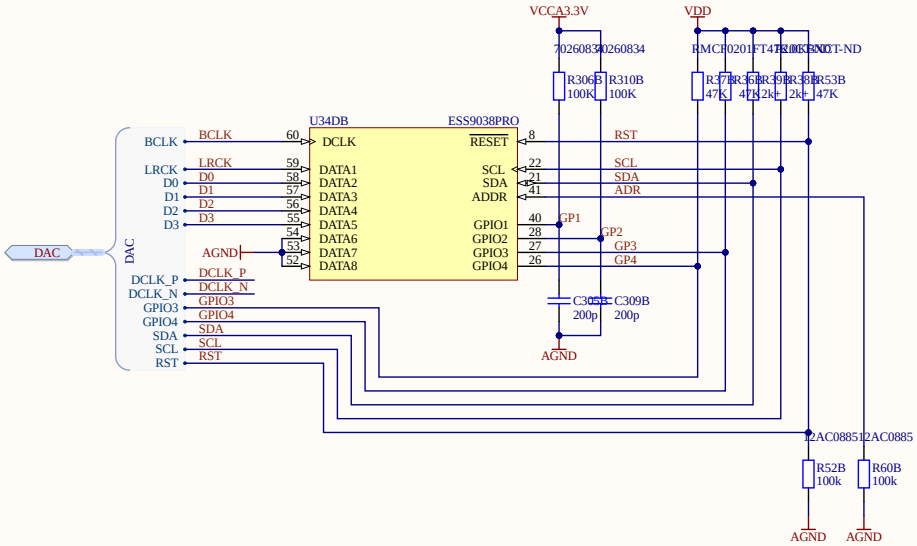
Parts Checked for Value and Consistency

Project	*DAC Daughter Prototype*		
Sheet Title	*DAC Proto DAC*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:18 PM	Sheet: 10 of 19	*DrawnBy: M. Pirello*
File: LD32_DAC.SchDoc			

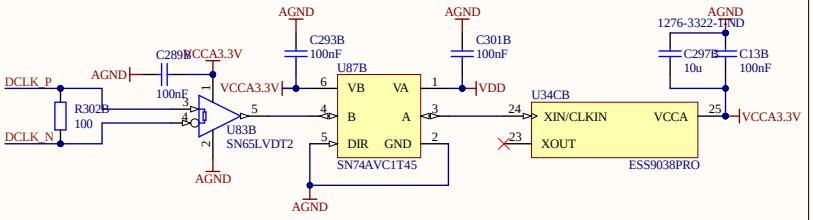
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation

LIGO

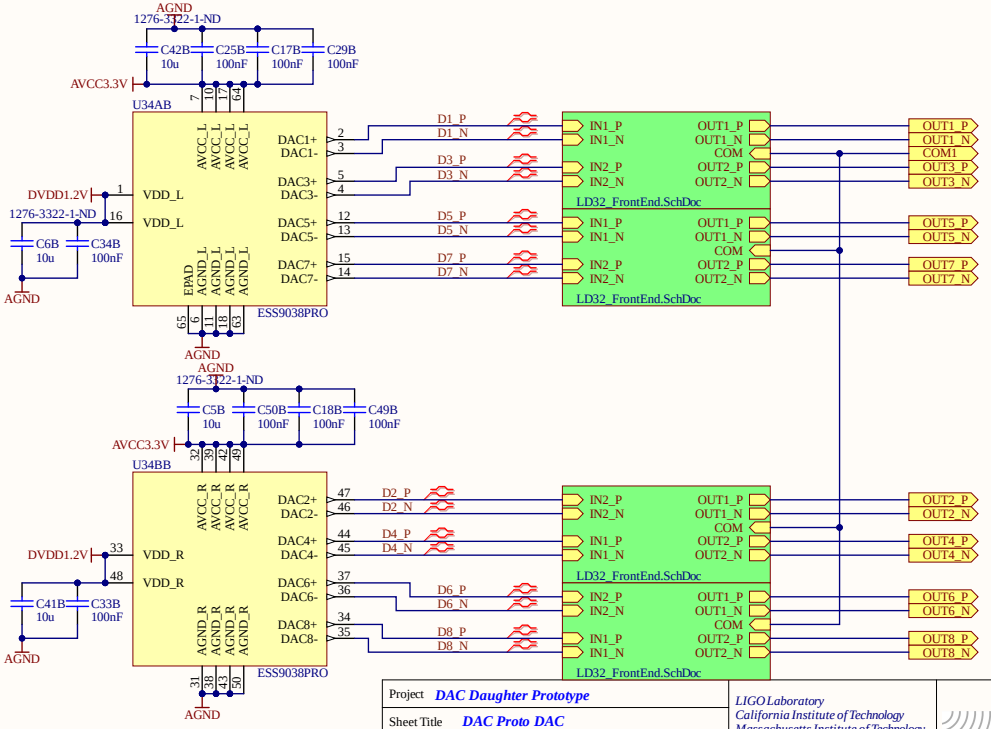
DAC Inputs



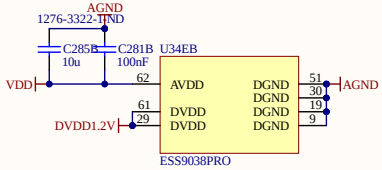
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

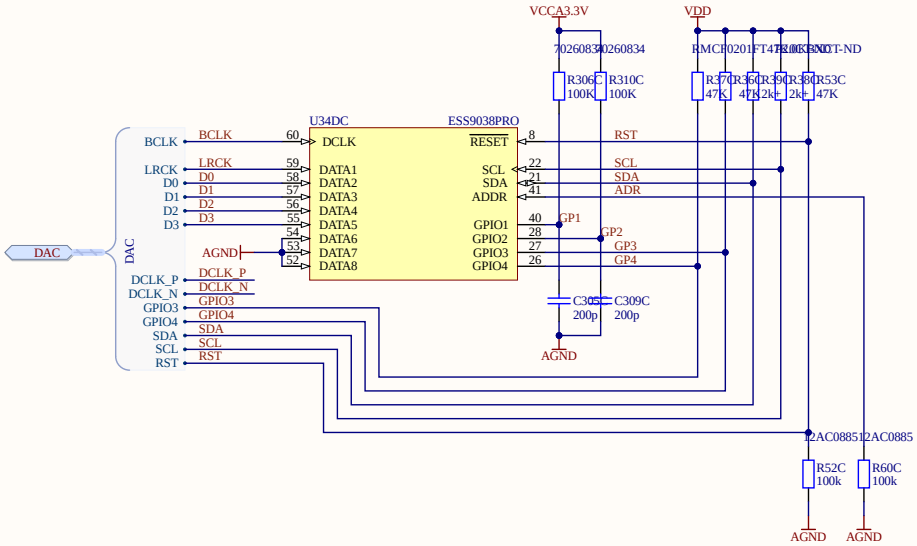
There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

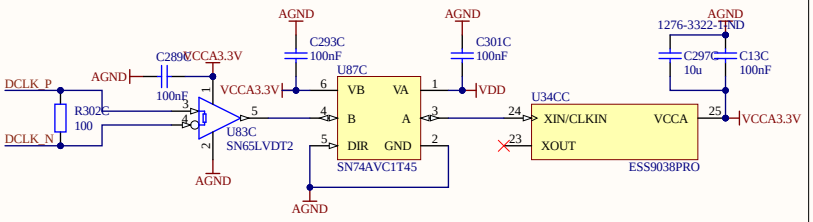
Parts Checked for Value and Consistency

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto DAC*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:19 PM	Sheet: 10 of 19	*DrawnBy: M. Pirello*
File: LD32_DAC.SchDoc			

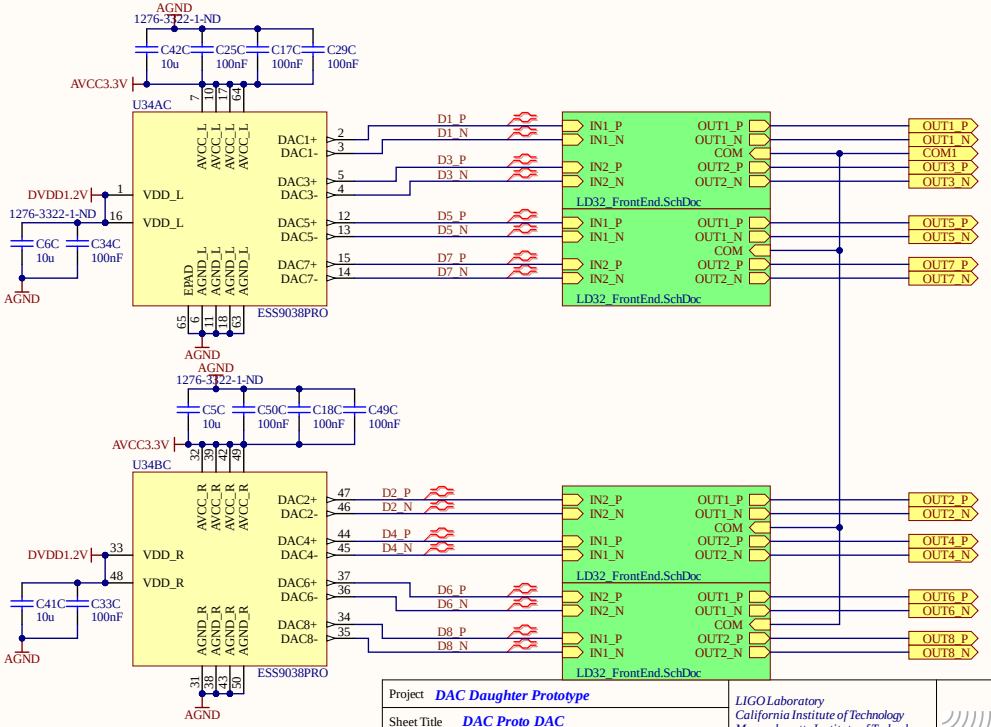
DAC Inputs



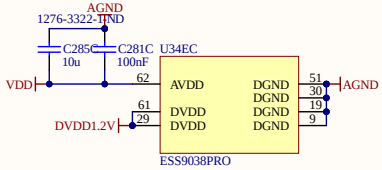
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

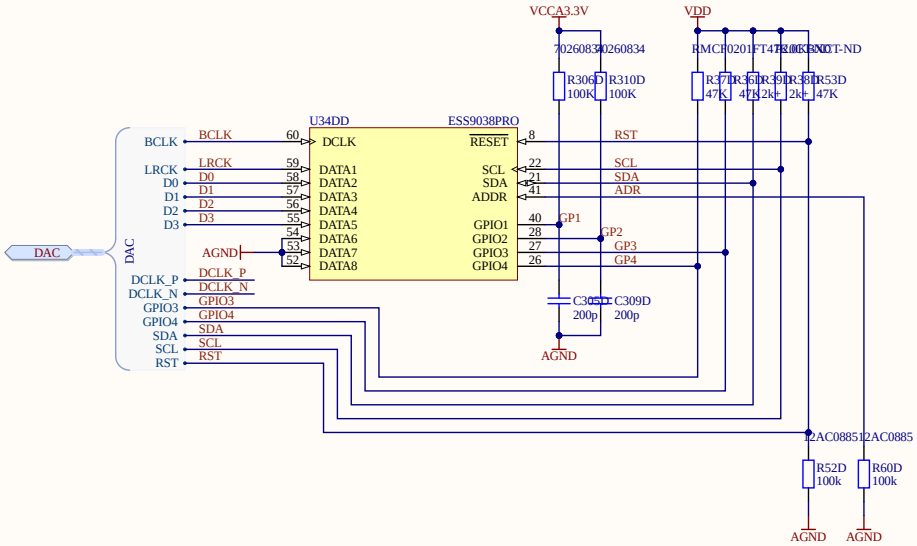
There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

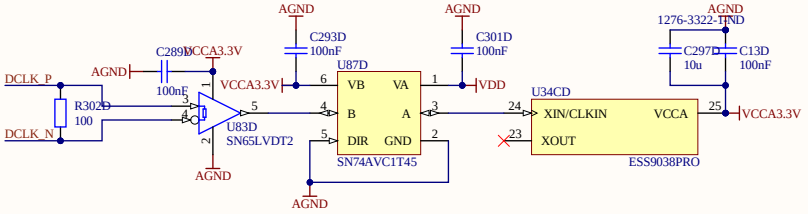
Parts Checked for Value and Consistency

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto DAC*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:19 PM	Sheet: 10 of 19	*DrawnBy: M. Pirello*
File: LD32_DAC.SchDoc			

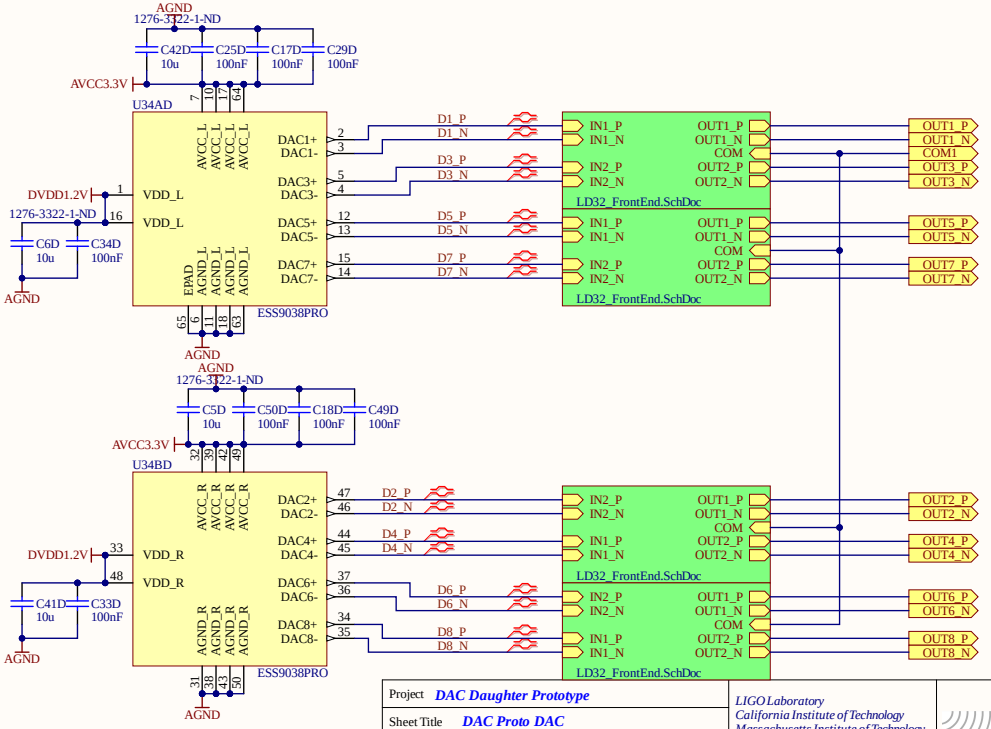
DAC Inputs



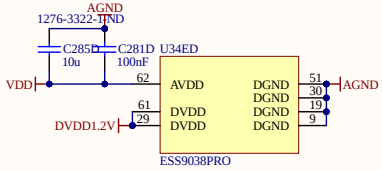
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

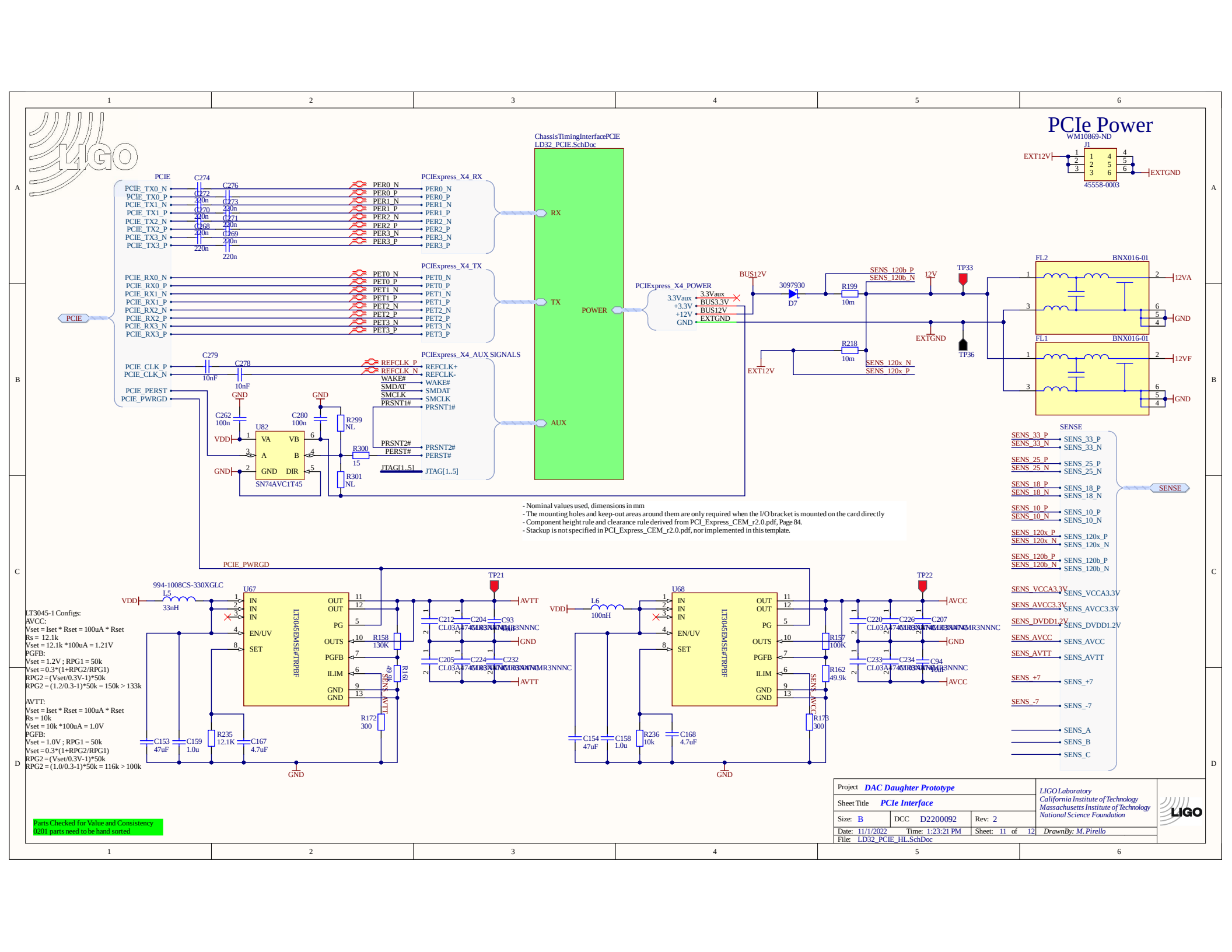
There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

Daniel

Parts Checked for Value and Consistency

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto DAC*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:20 PM	Sheet: 10 of 19	*DrawnBy: M. Pirello*
File: LD32_DAC.SchDoc			

PCIe Power



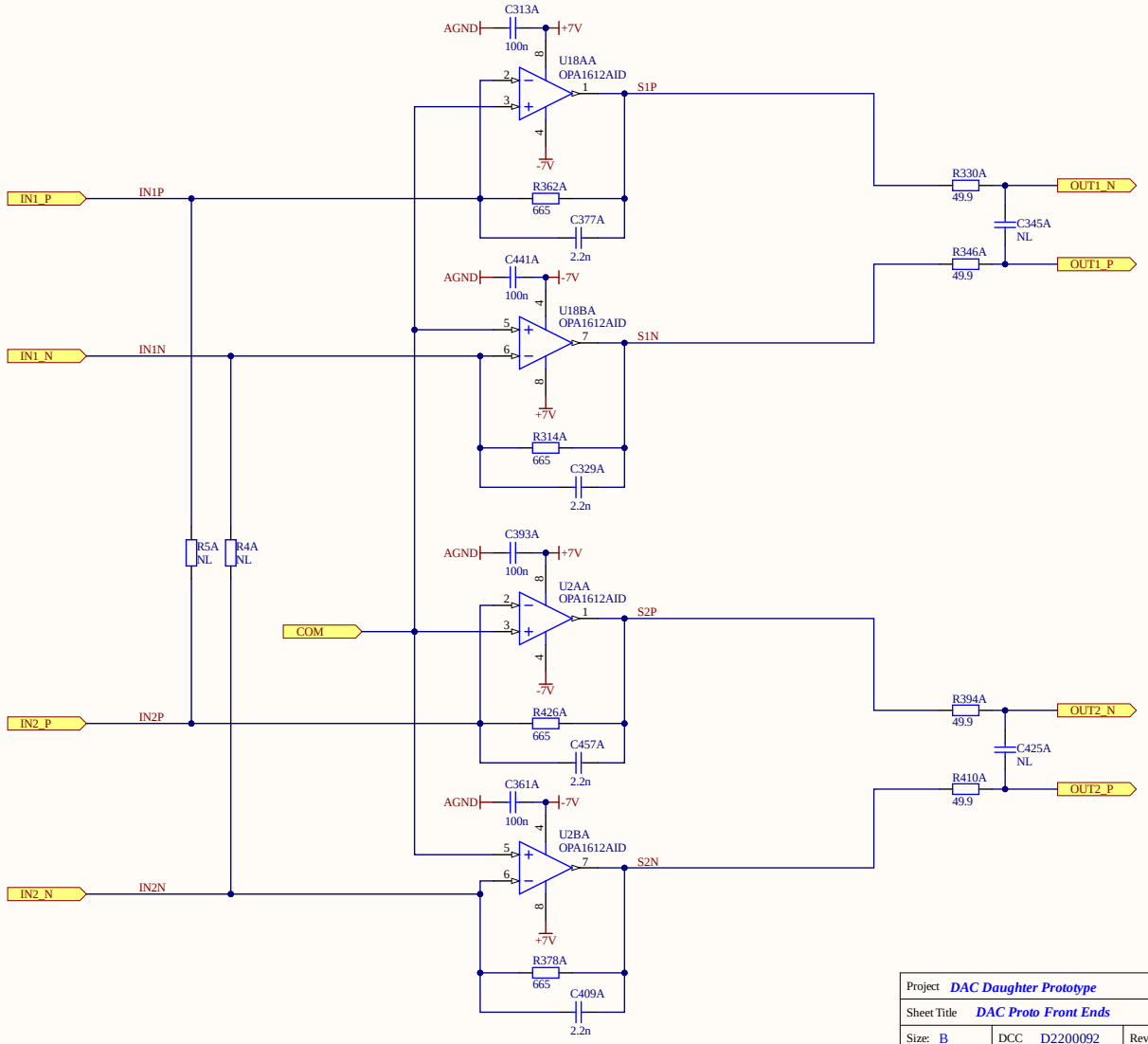
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

LT3045-1 Configs:
AVCC:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

AVTT:
Vset = Iset * Rset = 100uA * Rset
Rs = 10k
Vset = 10k *100uA = 1.0V
PGFB:
Vset = 1.0V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.0/0.3-1)*50k = 116k > 100k

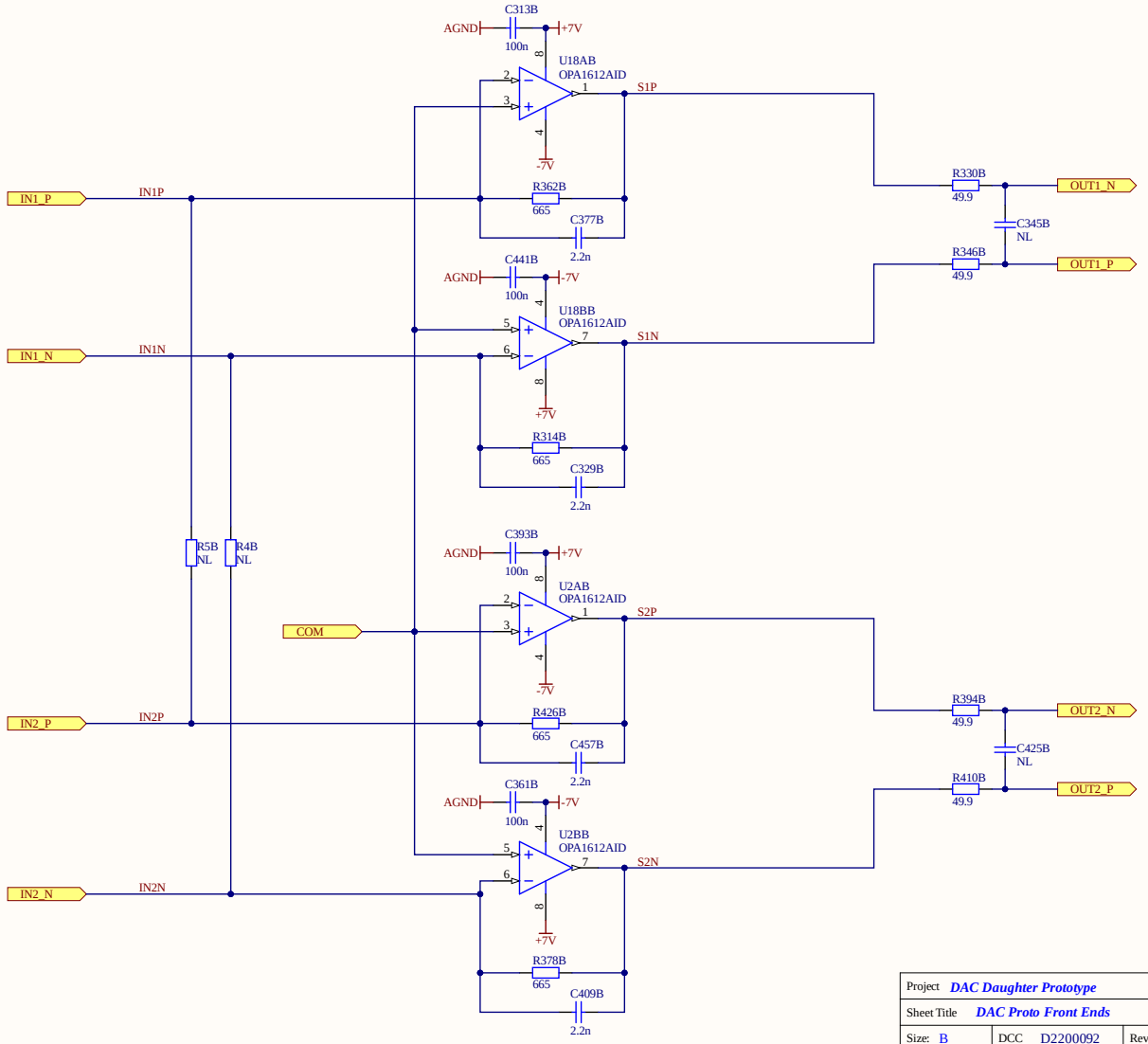
Parts Checked for Value and Consistency
0201 parts need to be hand sorted

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:21 PM	Sheet: 11 of 12	*DrawnBy: M. Pirello*
File: LD32_PCIE_HL.SchDoc			



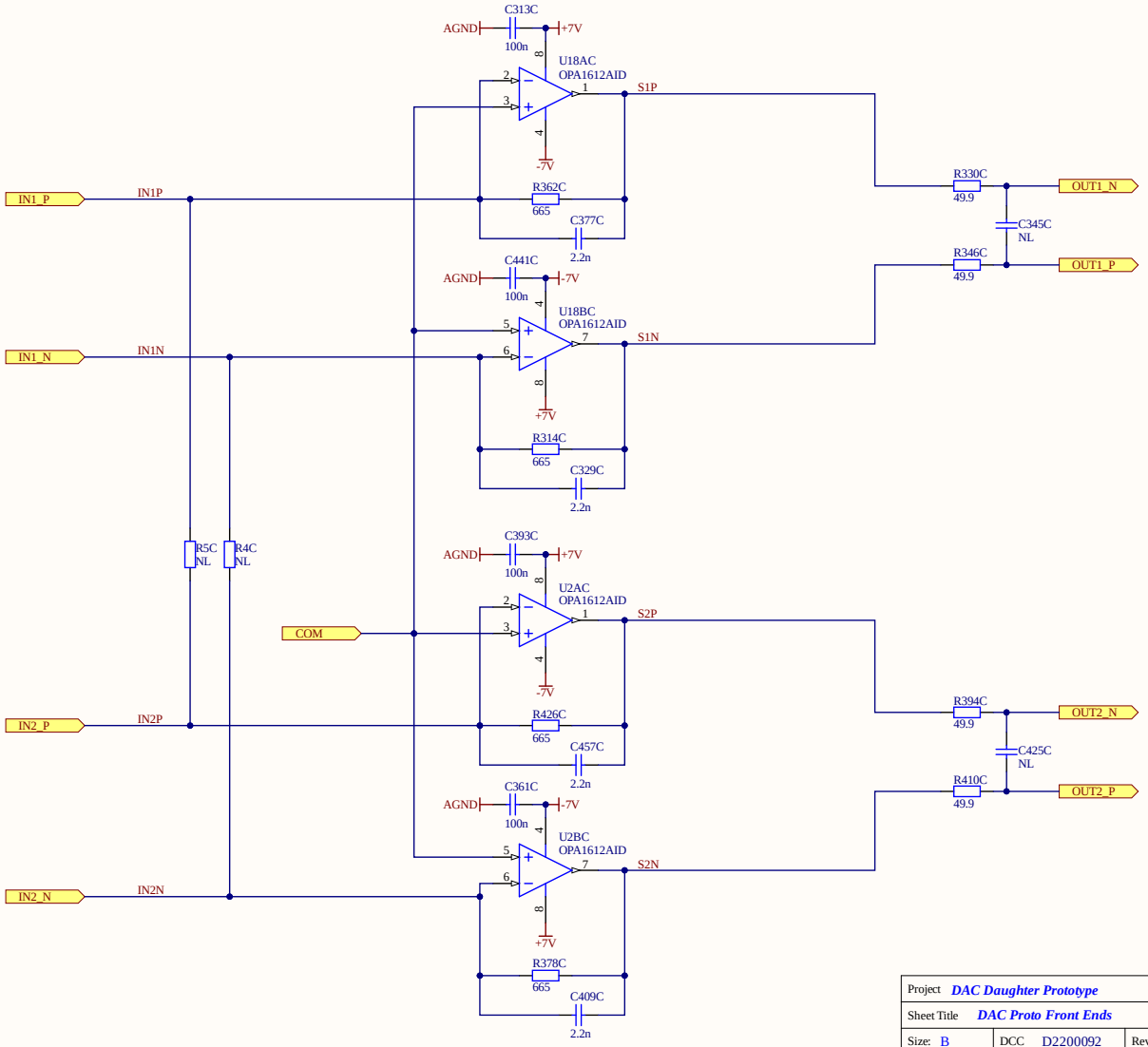
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:22 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



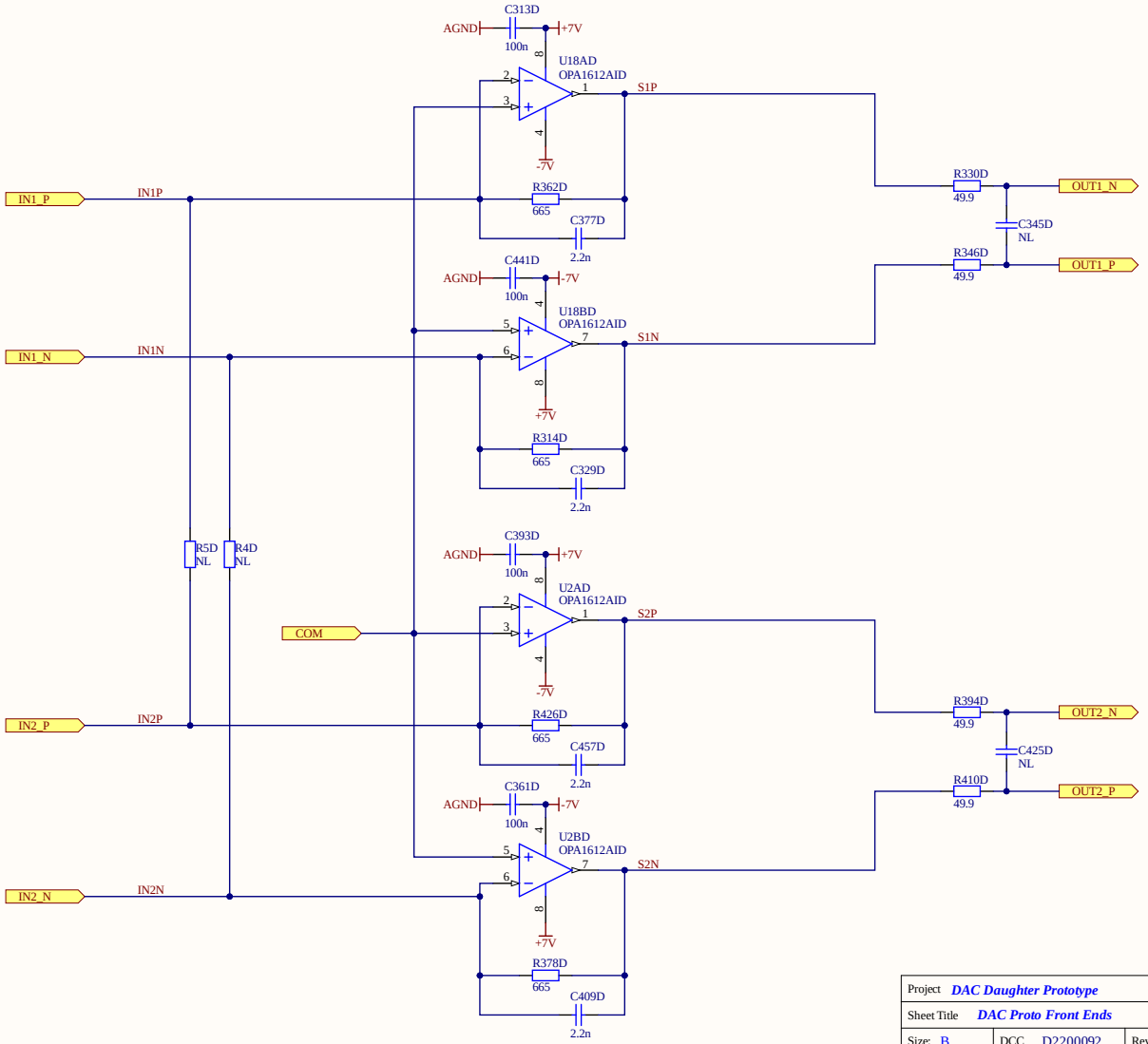
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:22 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



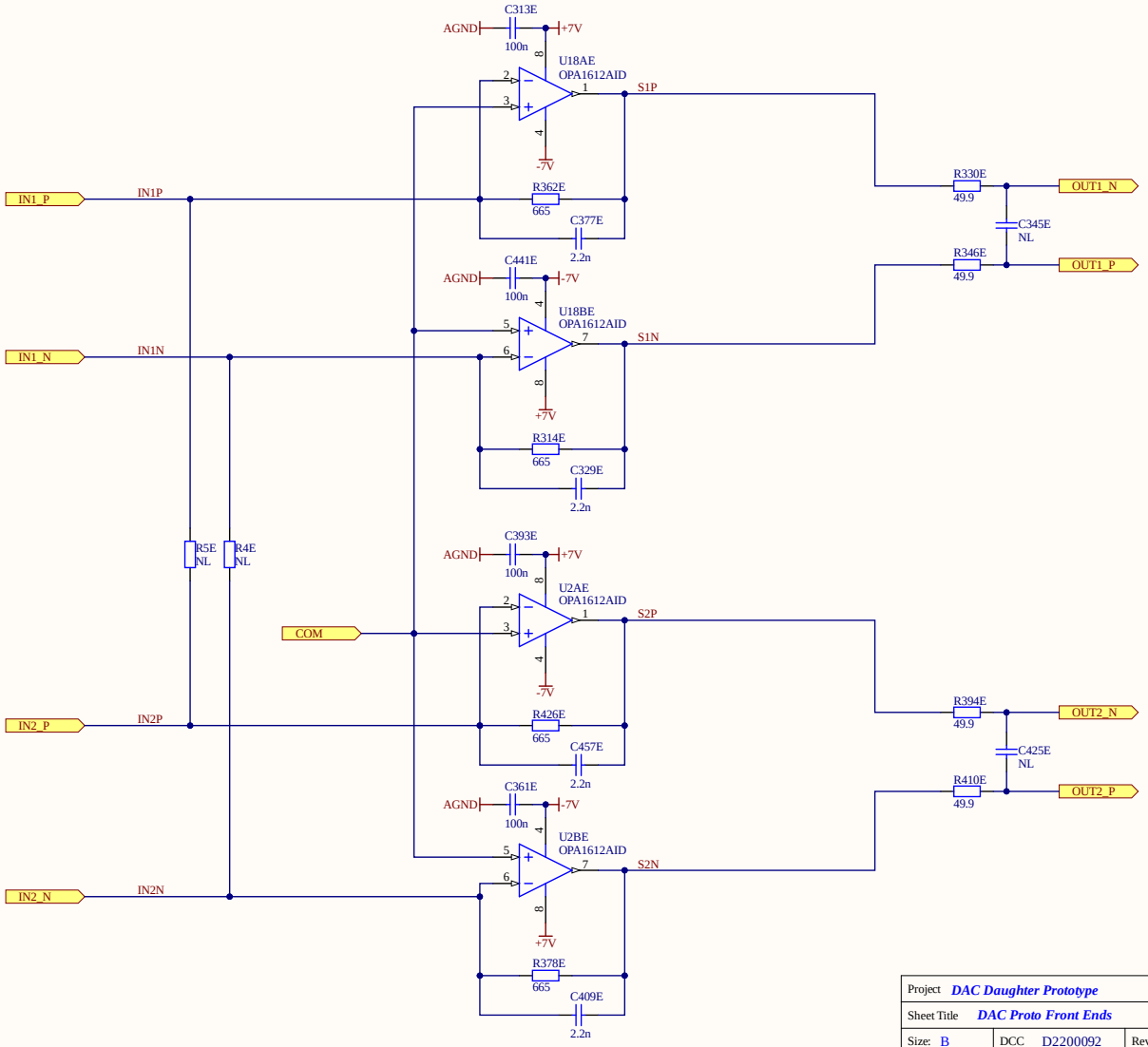
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:22 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



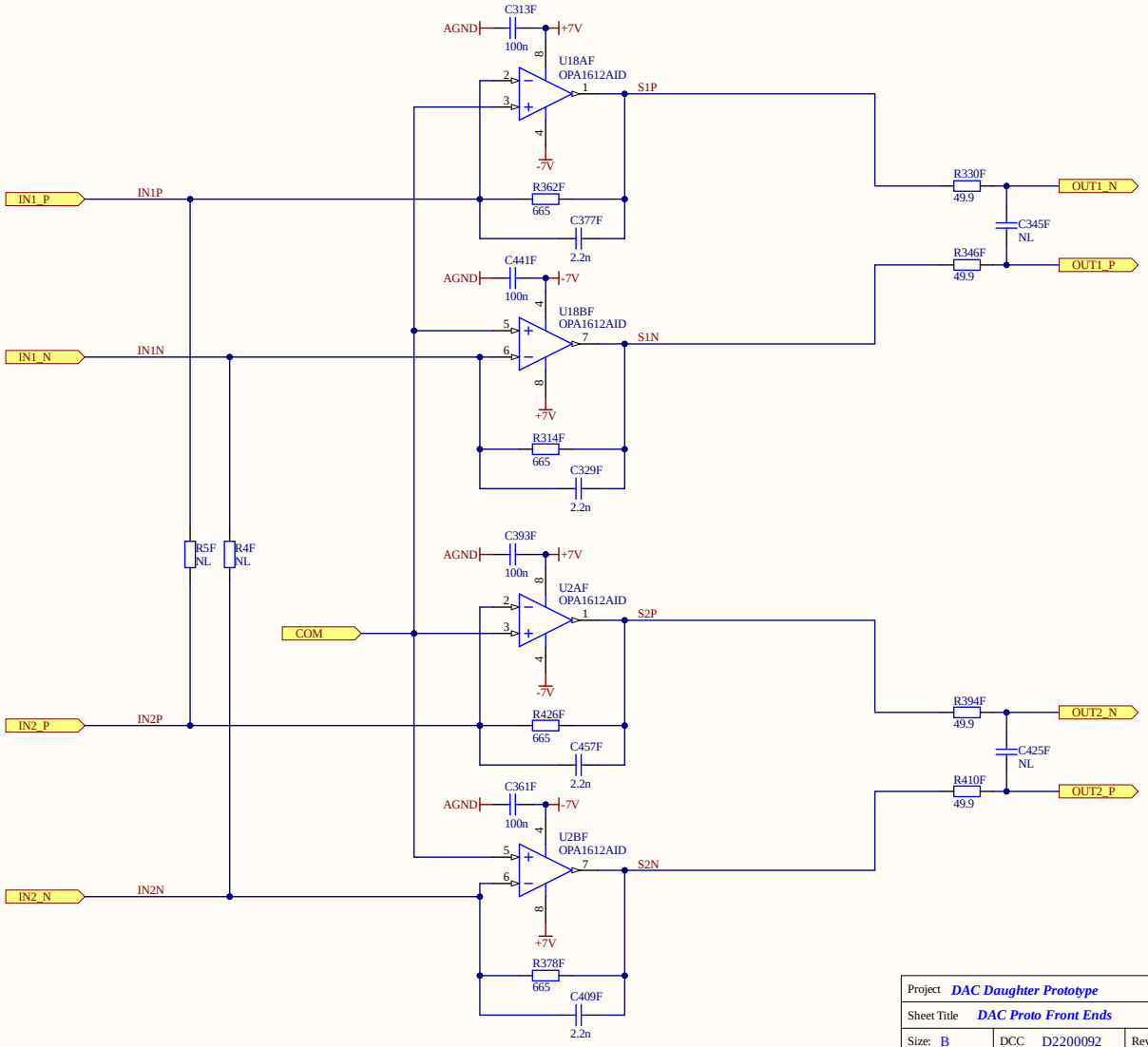
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:23 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



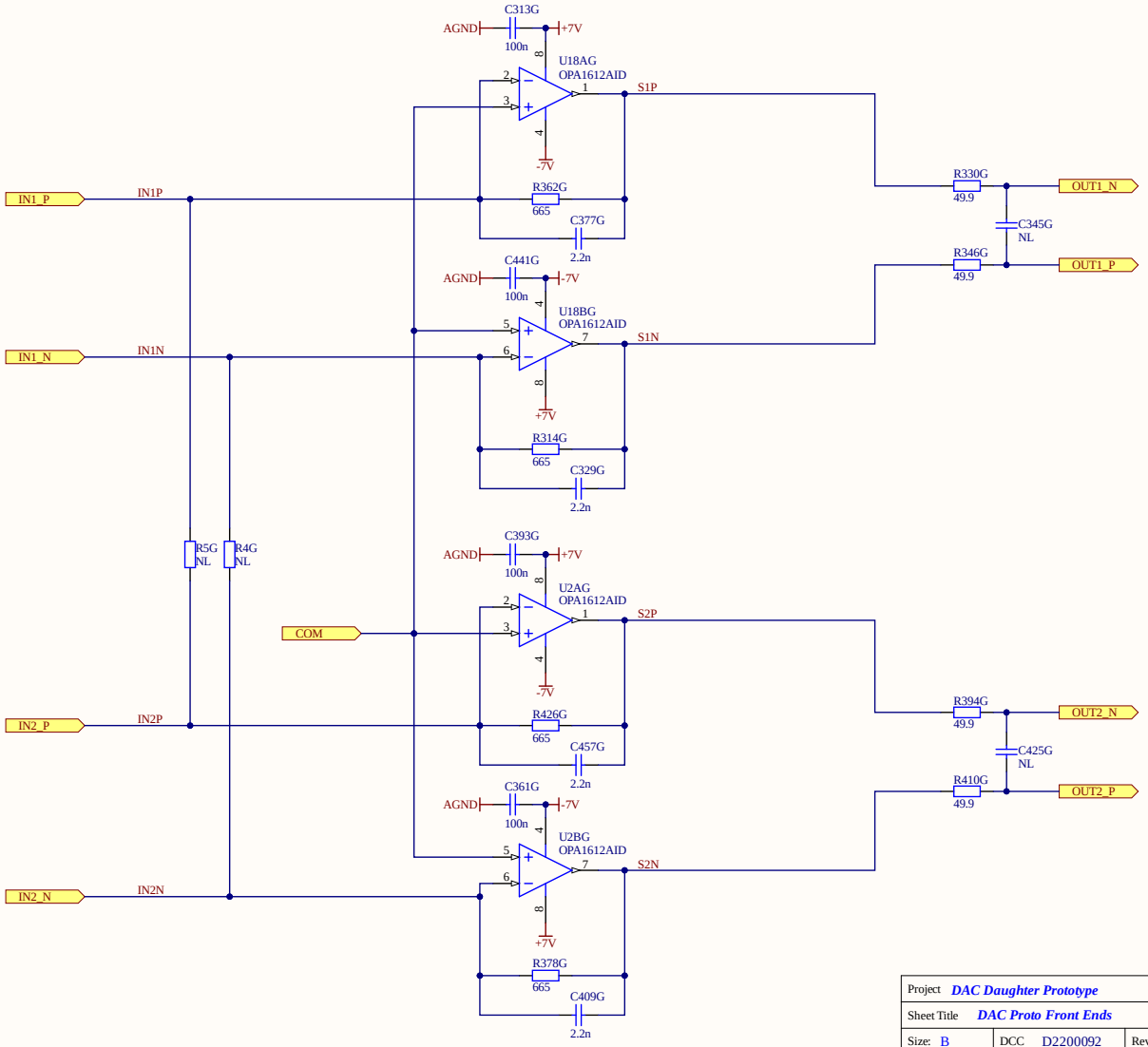
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:23 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



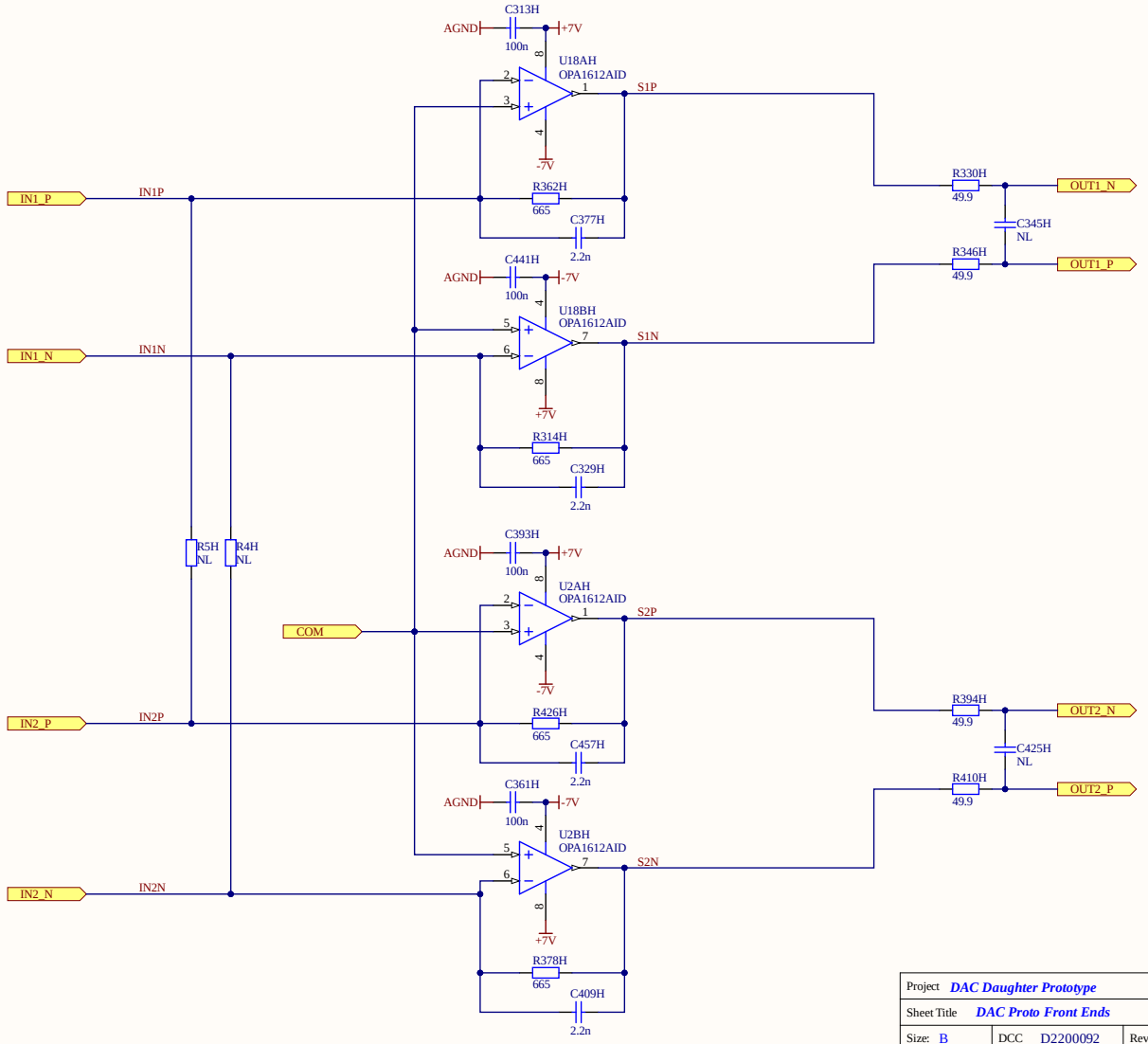
Parts Checked for Value and Consistency

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto Front Ends*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:24 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



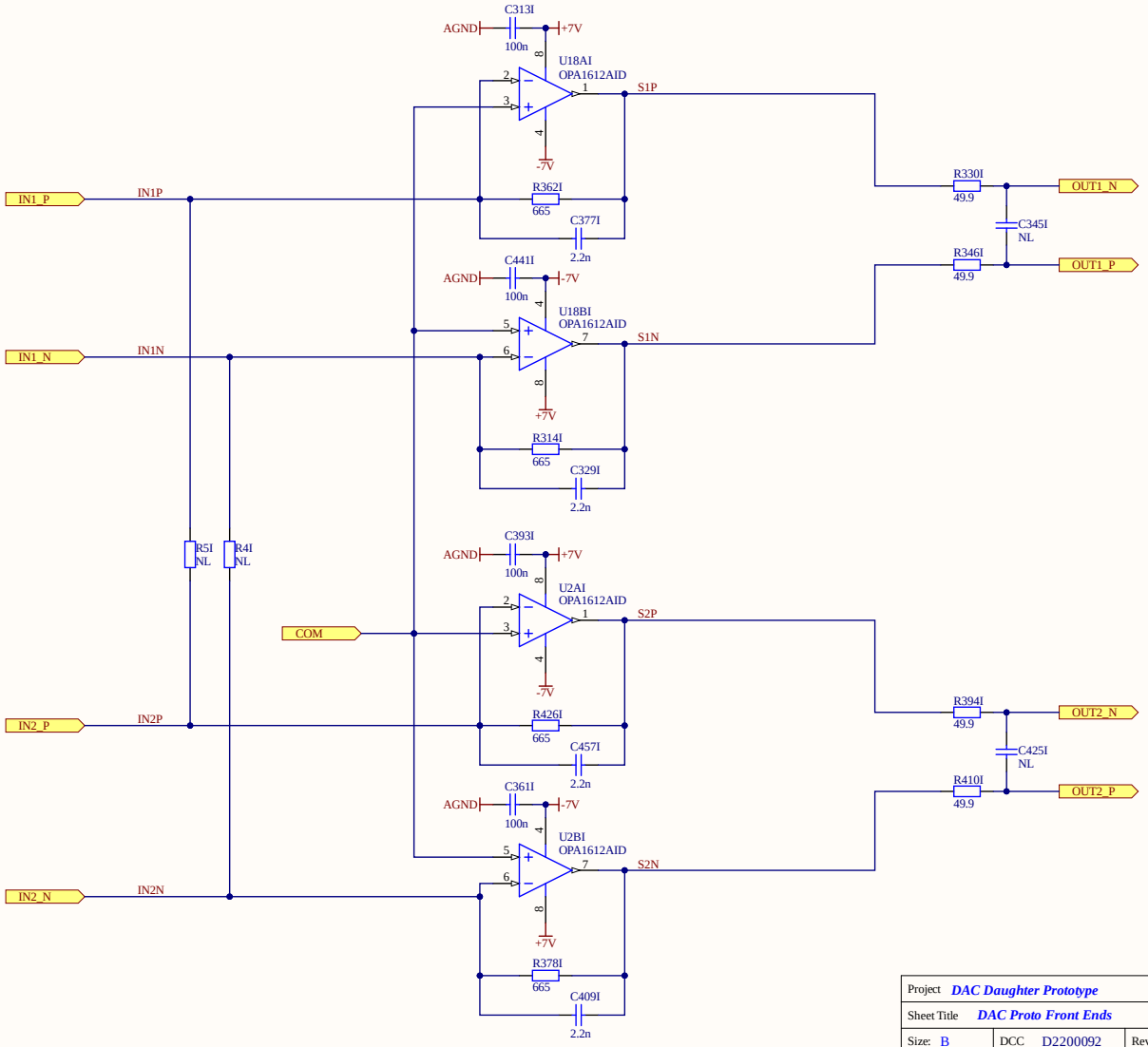
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:24 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



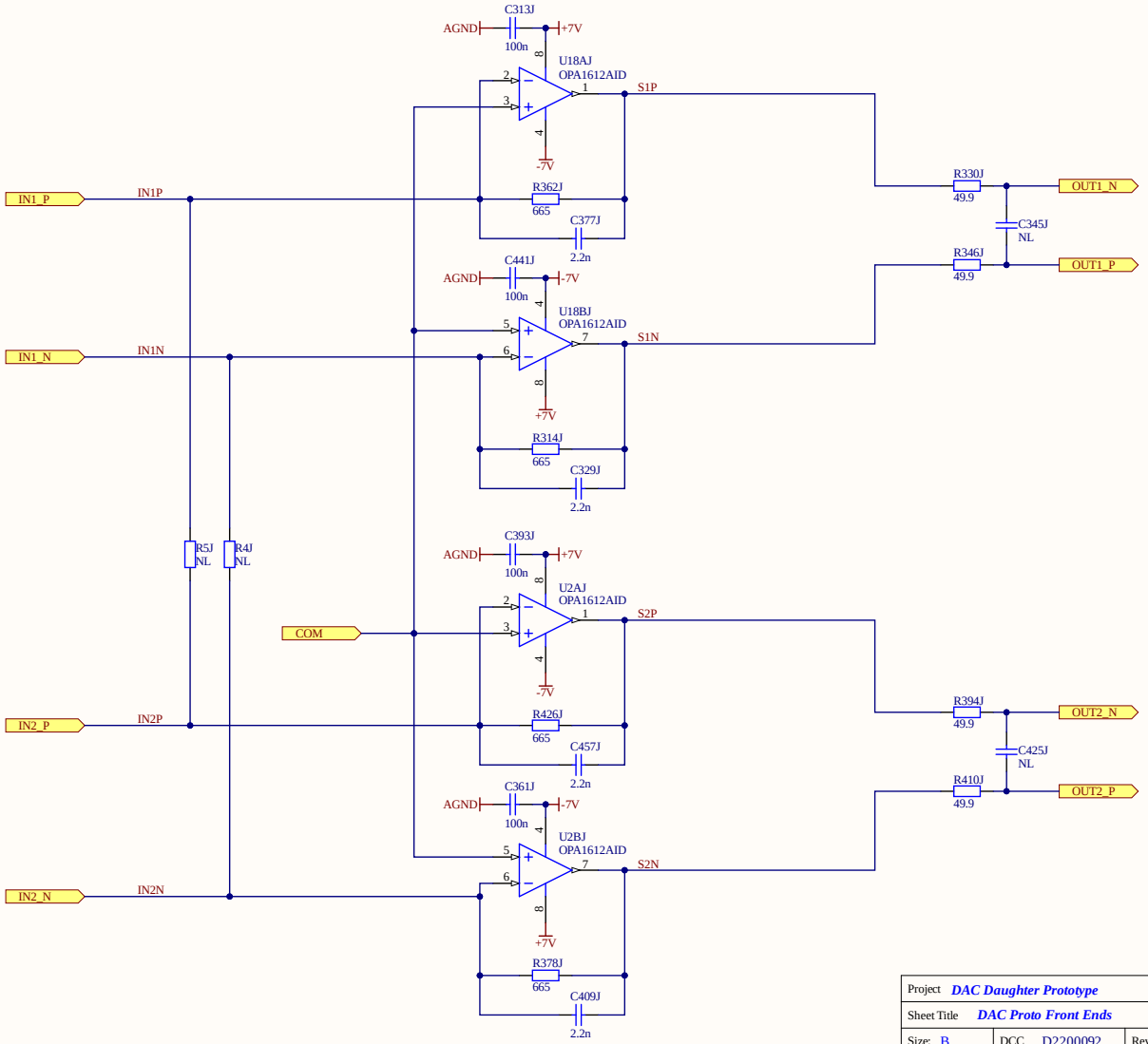
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:25 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



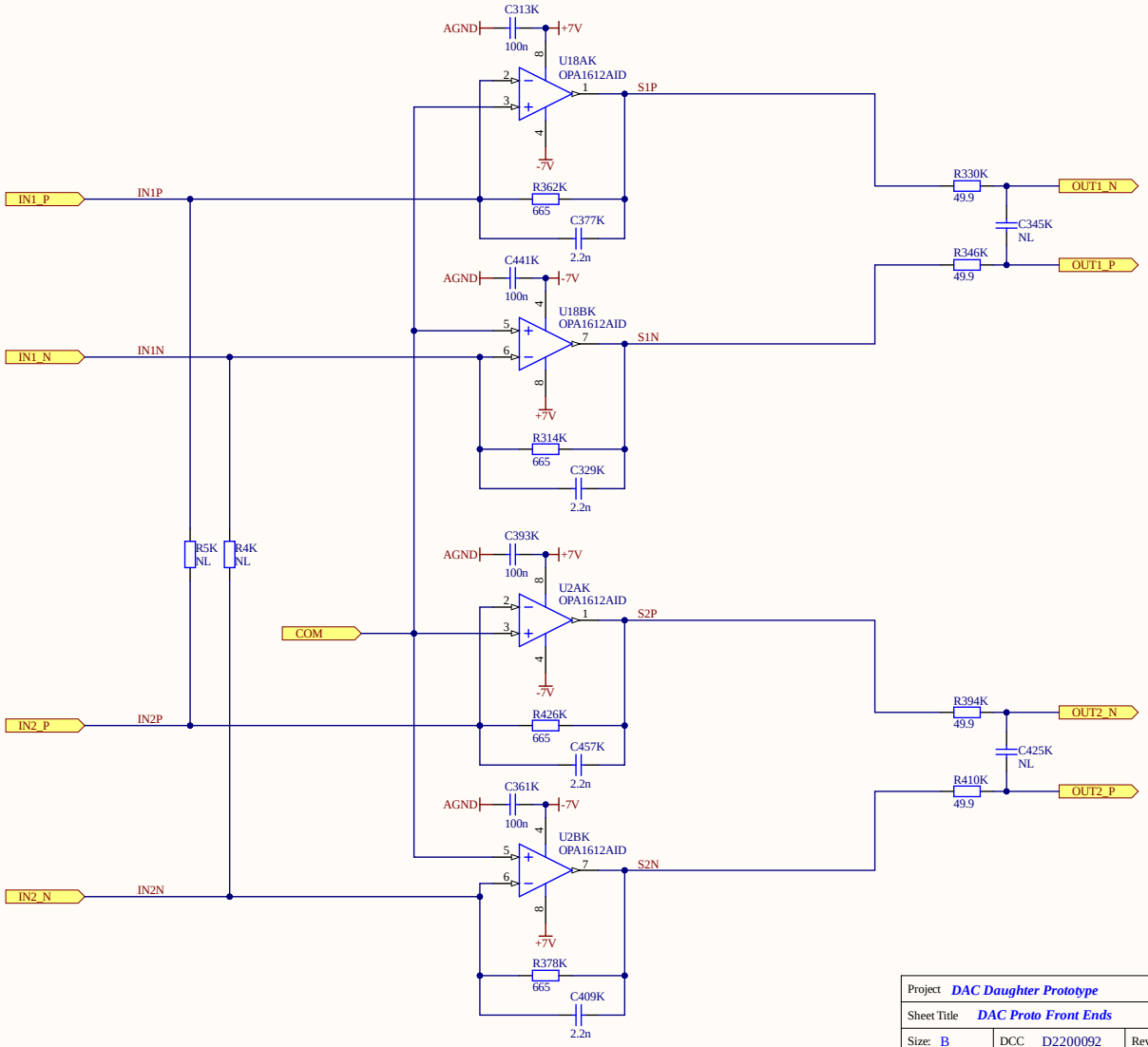
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:25 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



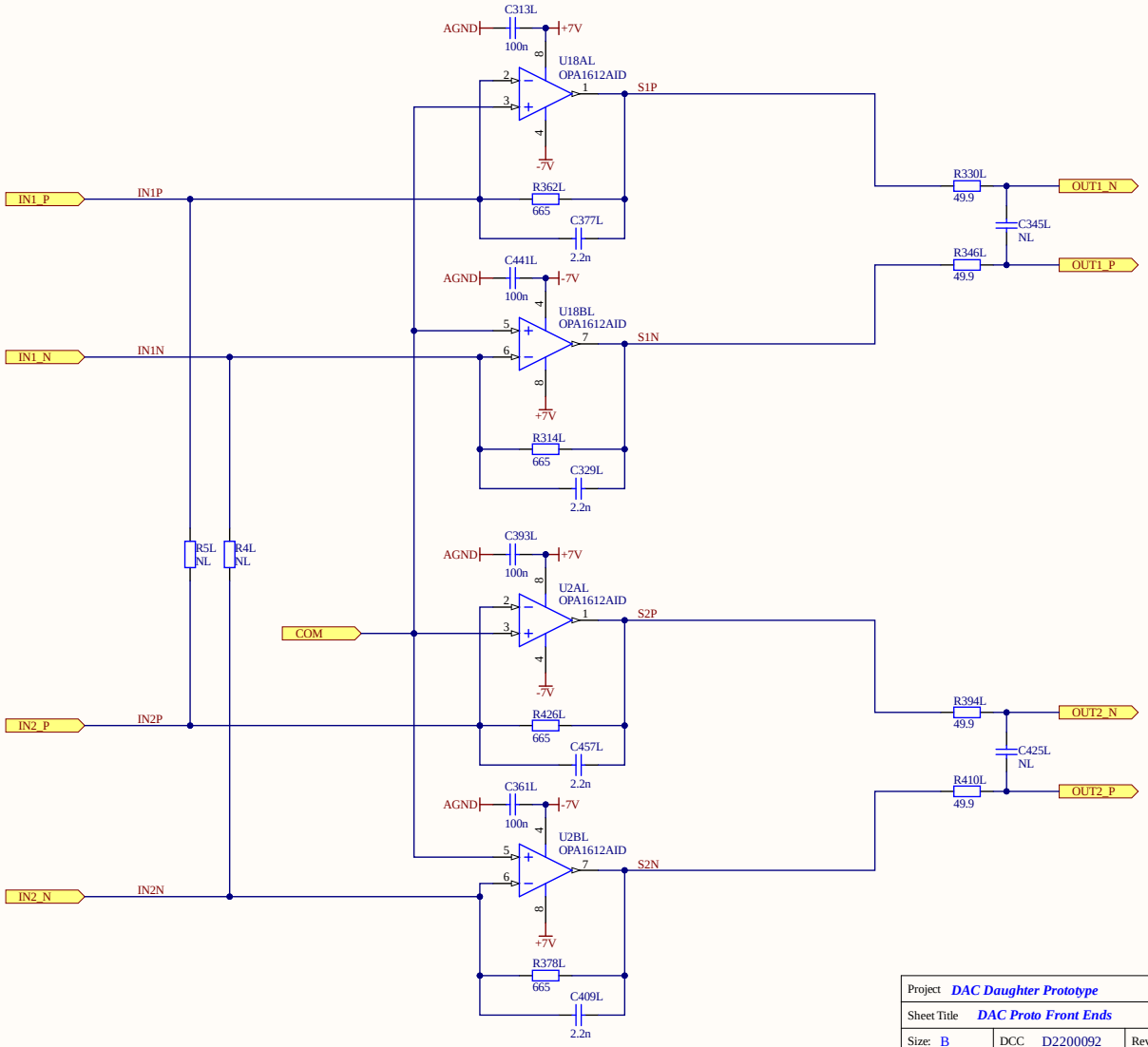
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:25 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



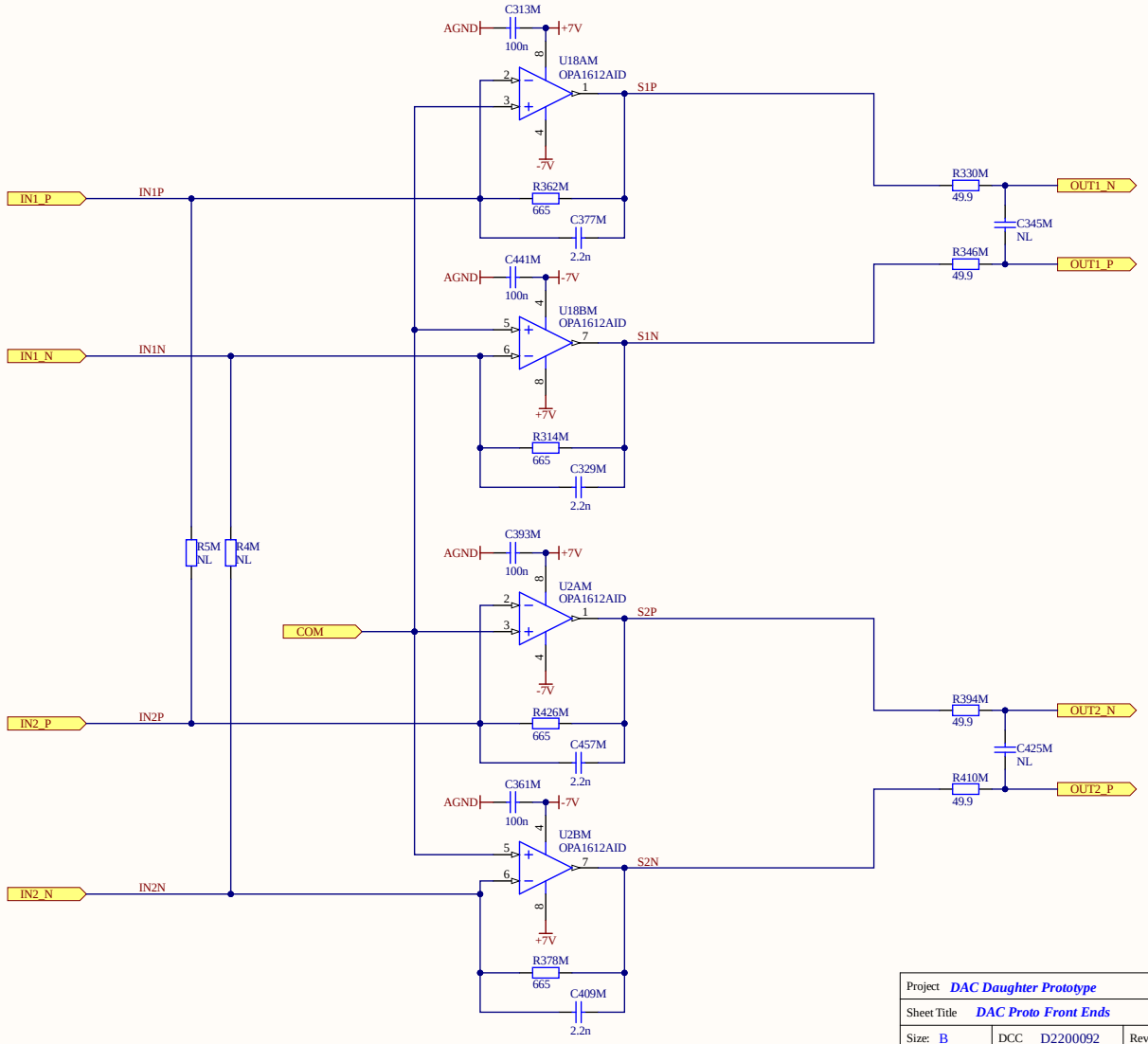
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:26 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



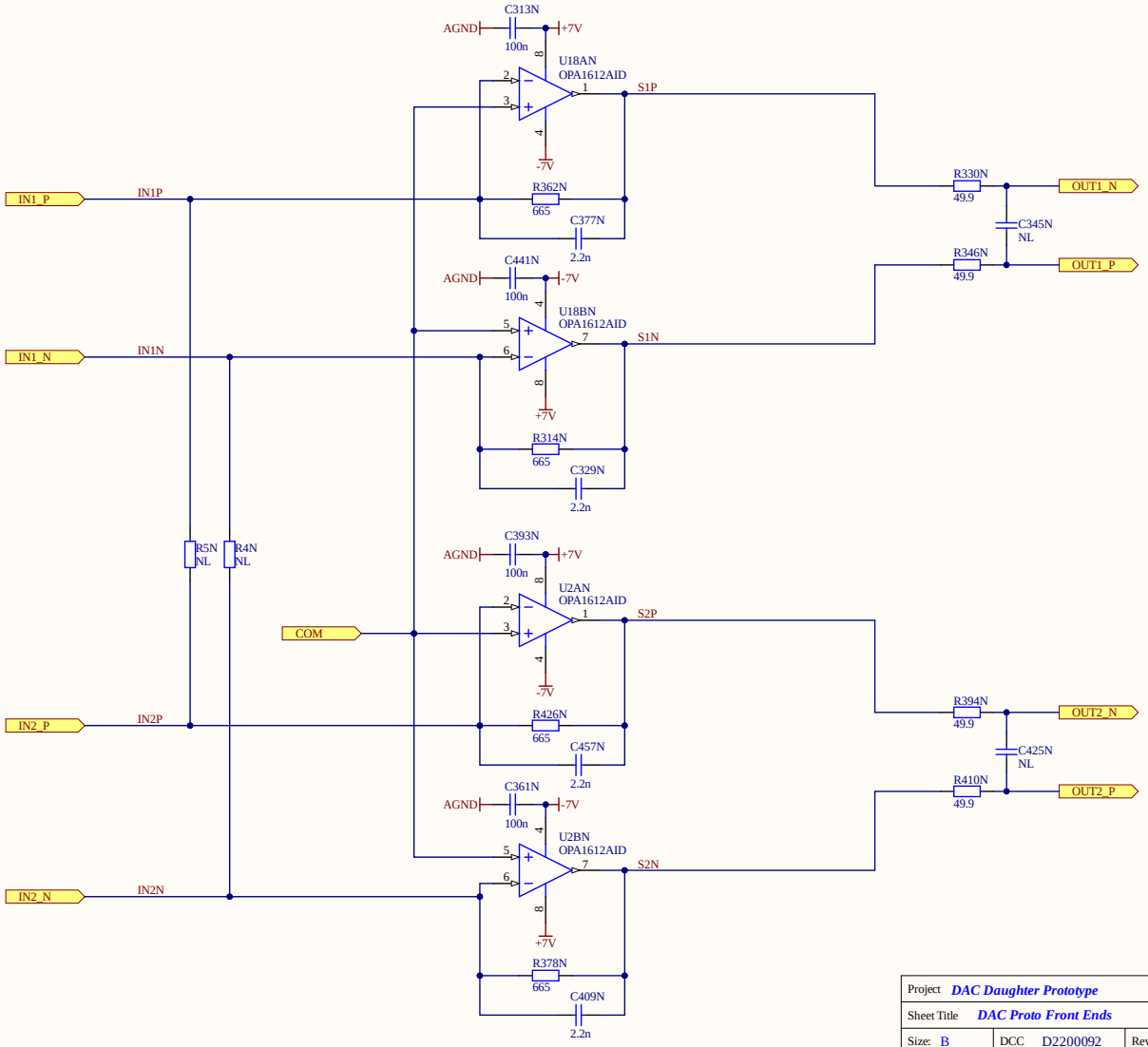
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:26 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



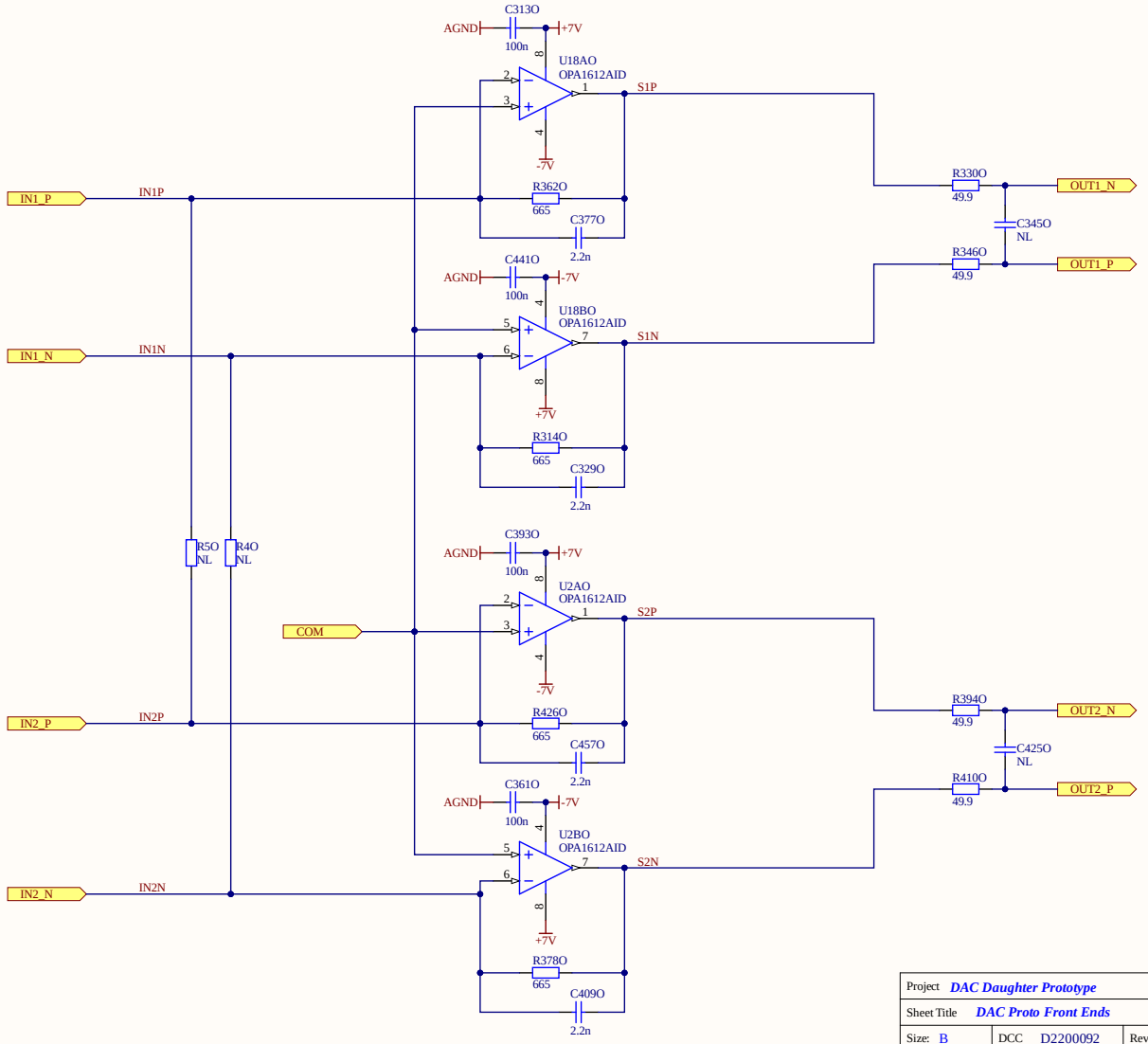
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:27 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



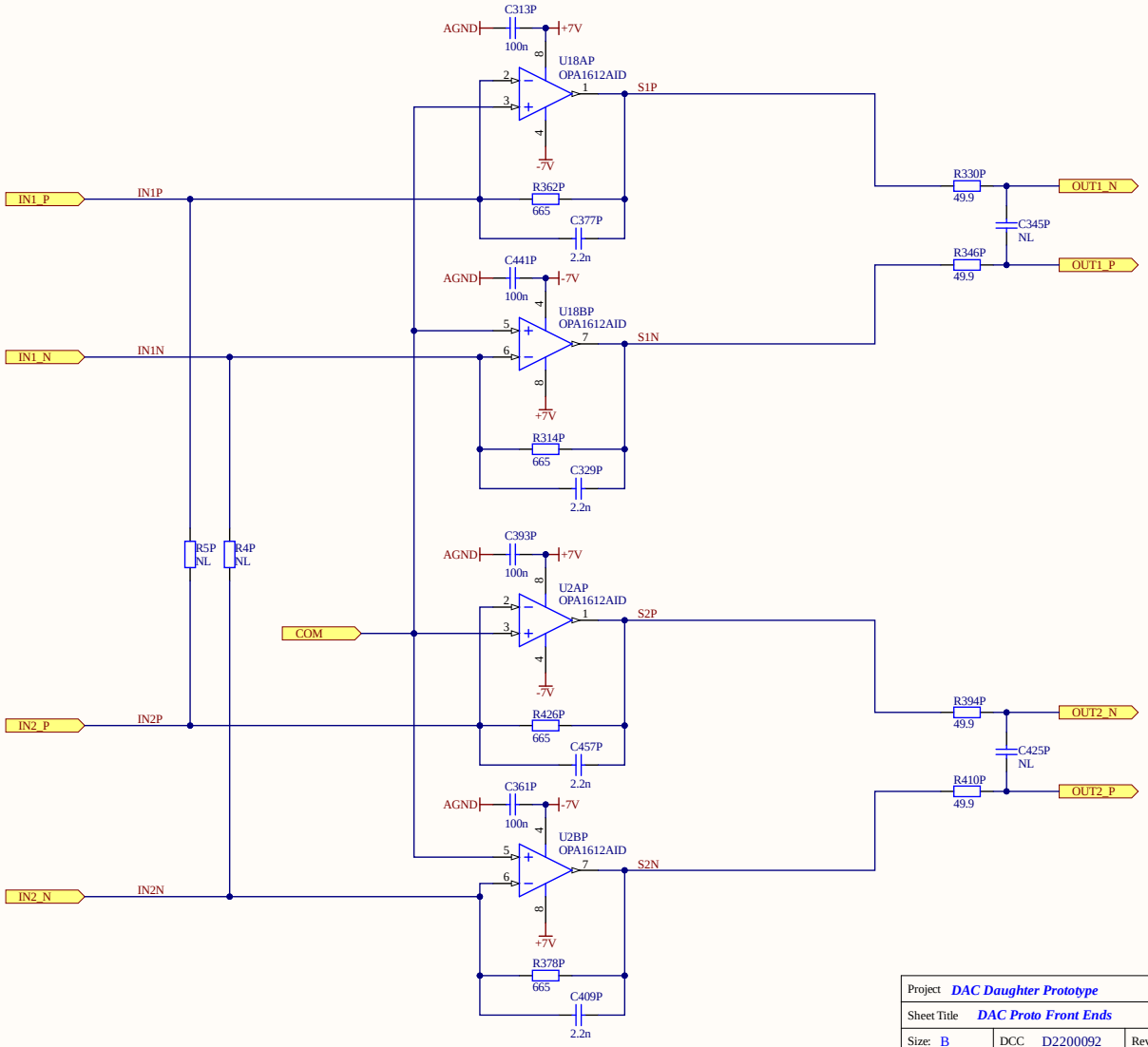
Parts Checked for Value and Consistency

Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:27 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			



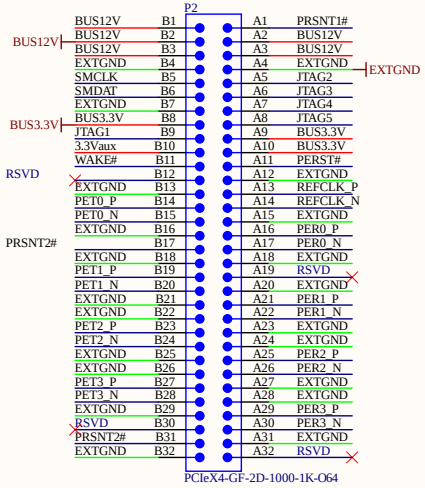
Parts Checked for Value and Consistency

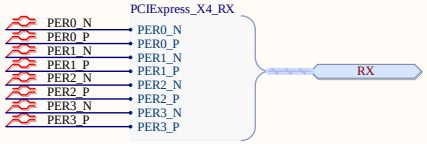
Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Proto Front Ends***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:28 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			

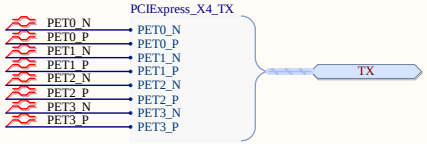


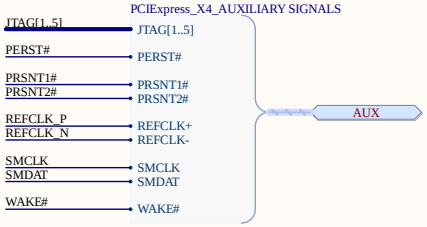
Parts Checked for Value and Consistency

Project	*DAC Daughter Prototype*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*DAC Proto Front Ends*		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:28 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello*
File: LD32_FrontEnd.SchDoc			

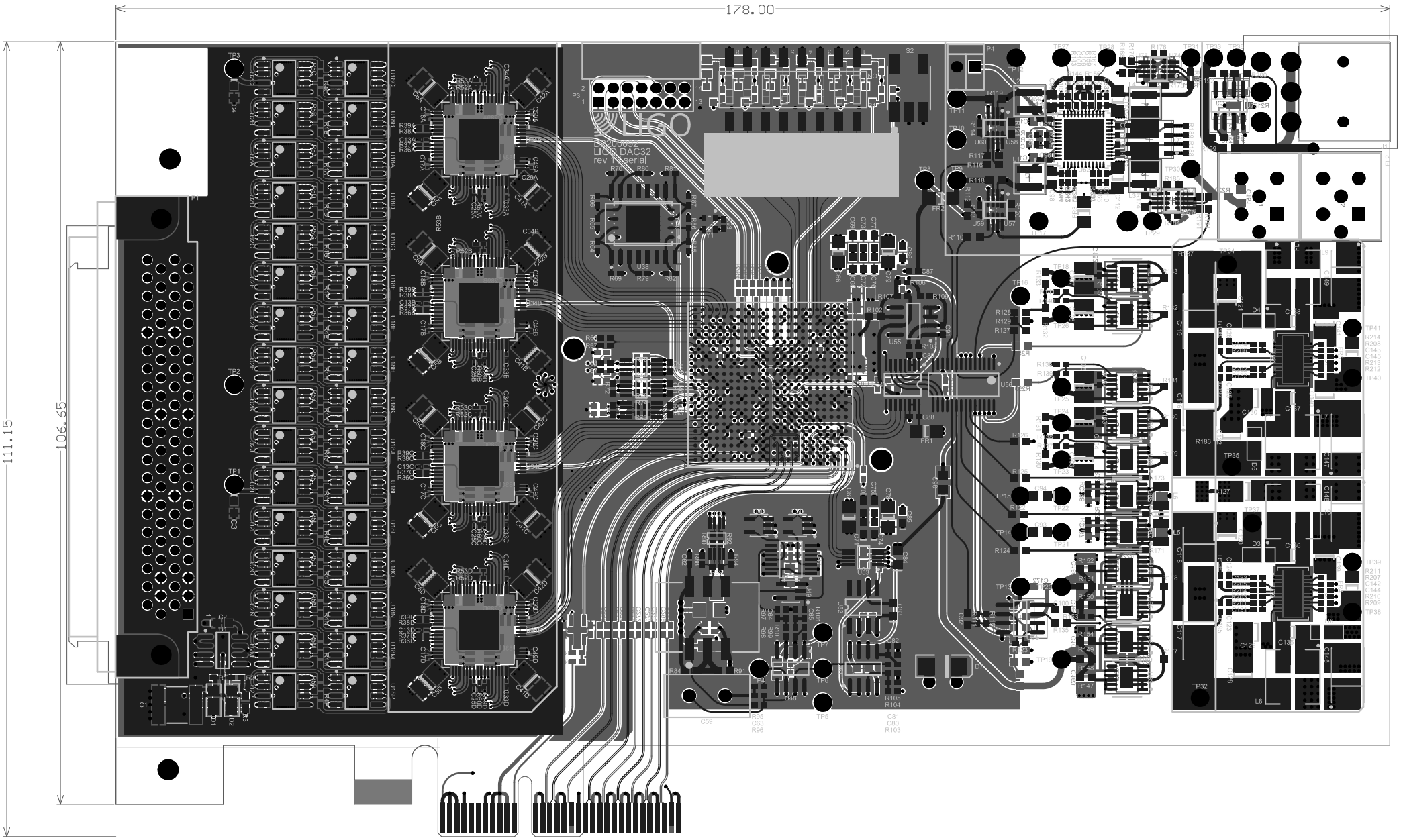








Project	***DAC Daughter Prototype***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***PCIe***		
Size: B	DCC D2200092	Rev: 2	
Date: 11/1/2022	Time: 1:23:28 PM	Sheet: 12 of 12	*DrawnBy: M. Pirello*
File: LD32_PCIE.SchDoc			


178.00
111.15
106.65
LIGO DAC32
rev 1 serial