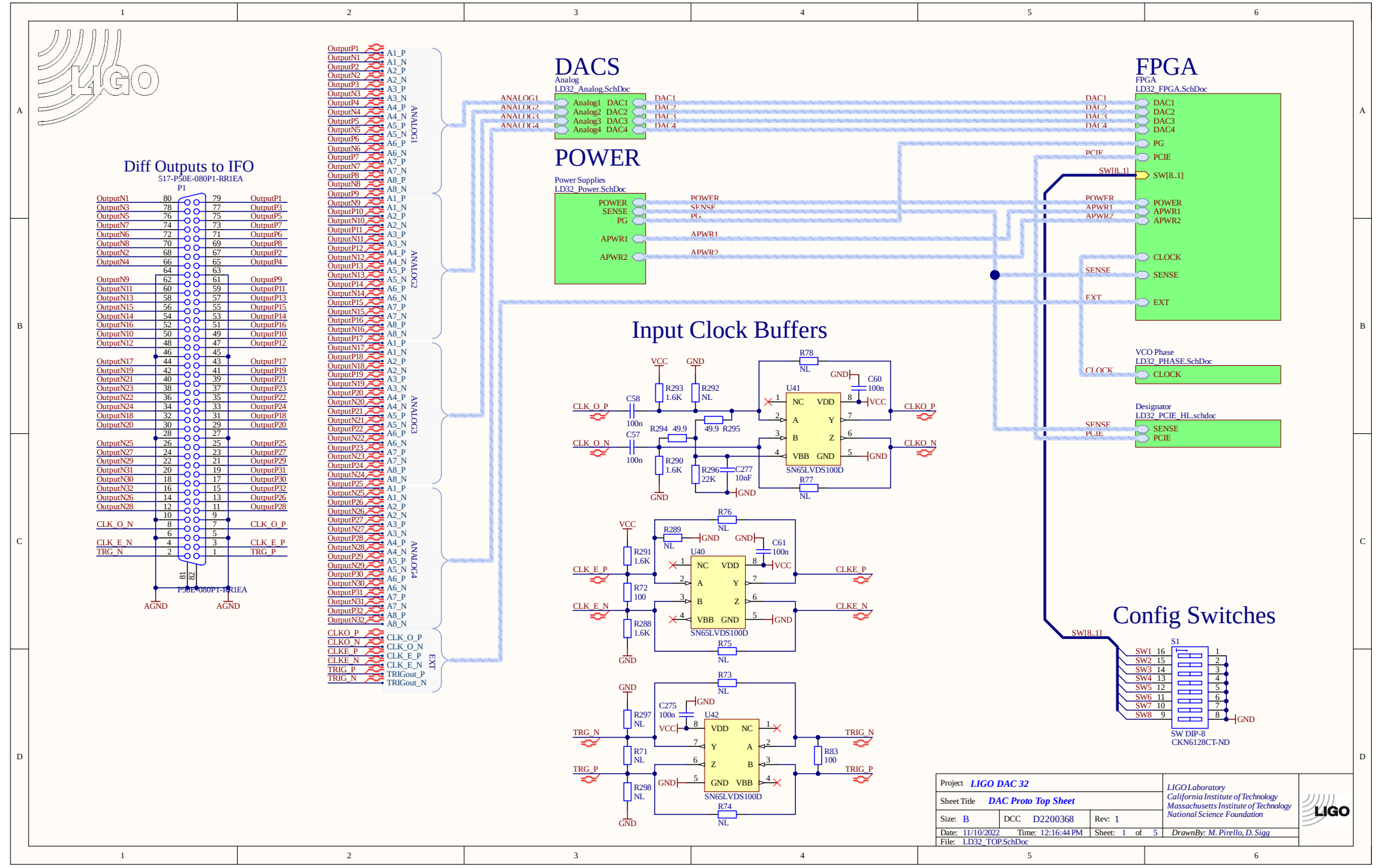
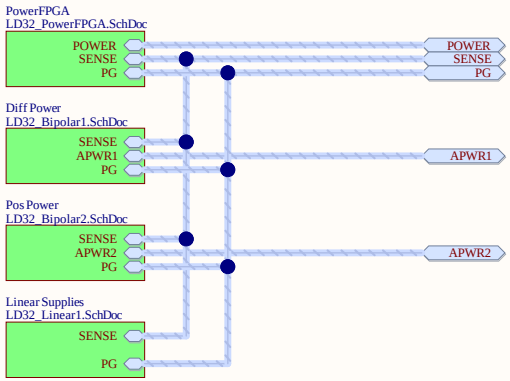

Diff Outputs to IFO
517-P50E-080P1-RR1EA
P1
DACS
Analog
LD32_Analog.SchDoc
POWER
Power Supplies
LD32_Power.SchDoc
FPGA
FPGA
LD32_FPGA.SchDoc
Input Clock Buffers
VCO Phase
LD32_PHASE.SchDoc
Designator
LD32_PCIE_HL.schdoc
Config Switches
SW DIP-8
CKN6128CT-ND
SN65LVDS100D
AGND
GND
VCC
Project LIGO DAC 32
Sheet Title DAC Proto Top Sheet
Size: B
DCC D2200368
Rev: 1
Date: 11/10/2022
Time: 12:16:44 PM
Sheet: 1 of 5
File: LD32_TOP.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

Power Top Sheet



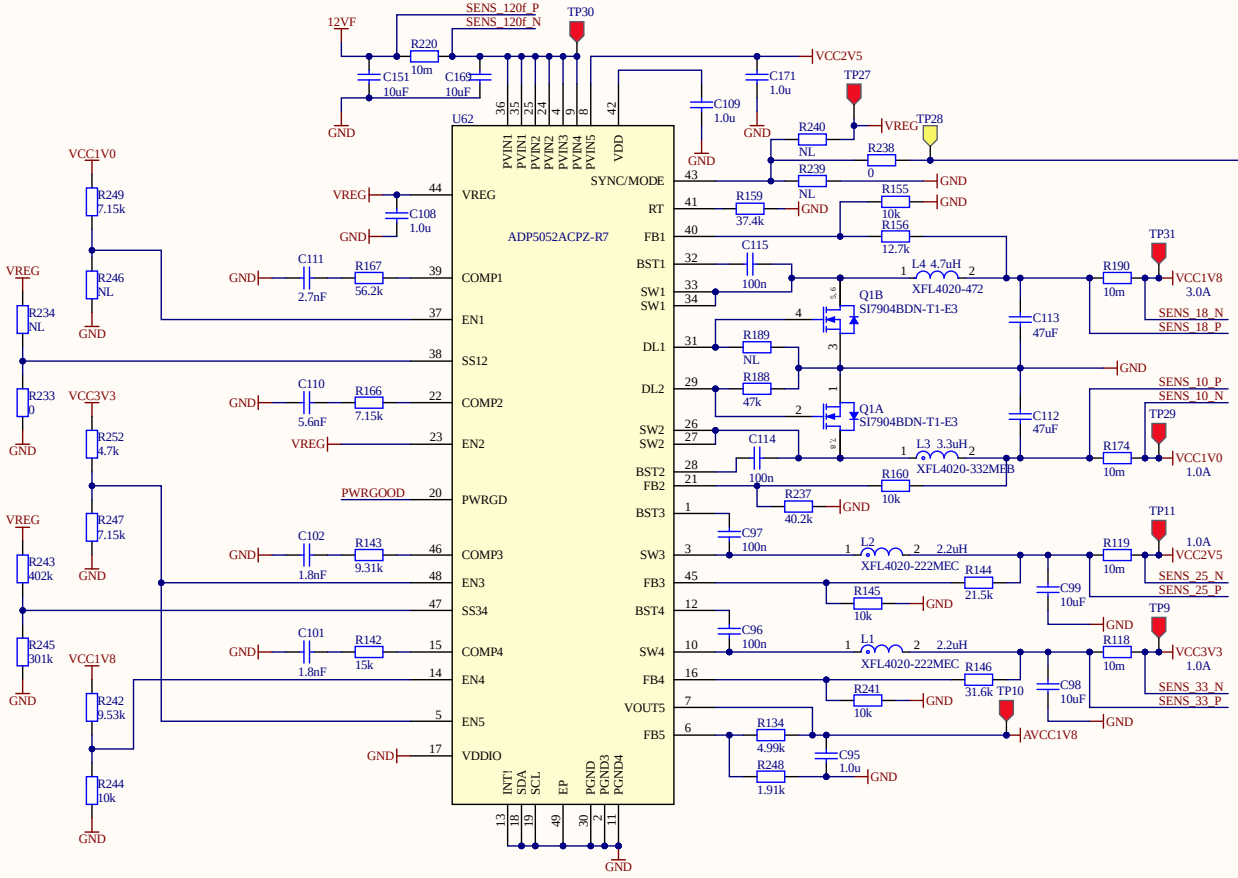
Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Power Top*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:16:45 PM		Sheet: 1 of 5	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Power.SchDoc			

Switched FPGA Power

ADP505x Configs
FB1 - 1.8V 12.7k, 10k, 4.7uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 2.5V 21.5k, 10k, 2.2uH
FB4 - 3.3V 31.6k, 10k, 2.2uH
FB5 - 1.8V 5k, 1.91k

Legend
VCC = 3.3V (digital votlage)
VDD = 1.8V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

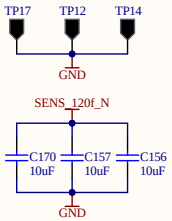
Power Up Config
1st - VCC1V0
2nd - VCC1V8
3rd - VCC3V3
4th & 5th VCC2V5 & AVCC1V8



POWER
PWRSYNC
POWER

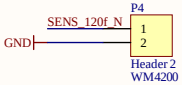
SENSE
SENS_33_P
SENS_33_N
SENS_25_P
SENS_25_N
SENS_18_P
SENS_18_N
SENS_10_P
SENS_10_N
SENS_120x_P
SENS_120x_N
SENS_120b_P
SENS_120b_N
SENS_VCCA3.3V
SENS_AVCC3.3V
SENS_DVDD1.2V
SENS_AVCC
SENS_AVTT
SENS_+7
SENS_-7
SENSE

POWER GOOD
PG_VCCAL3.3V
PG_AVCCL3.3V
PG_DVDDL1.2V
PG_SW+2V
PG_SW+4V
PWRGOOD
PG_SW+8V
PG_SW-8V
PG-7
PG+7
PG_FPGA
PG_SW+8
PG_SW-8
PG_L-7v
PG_L+7v
PG

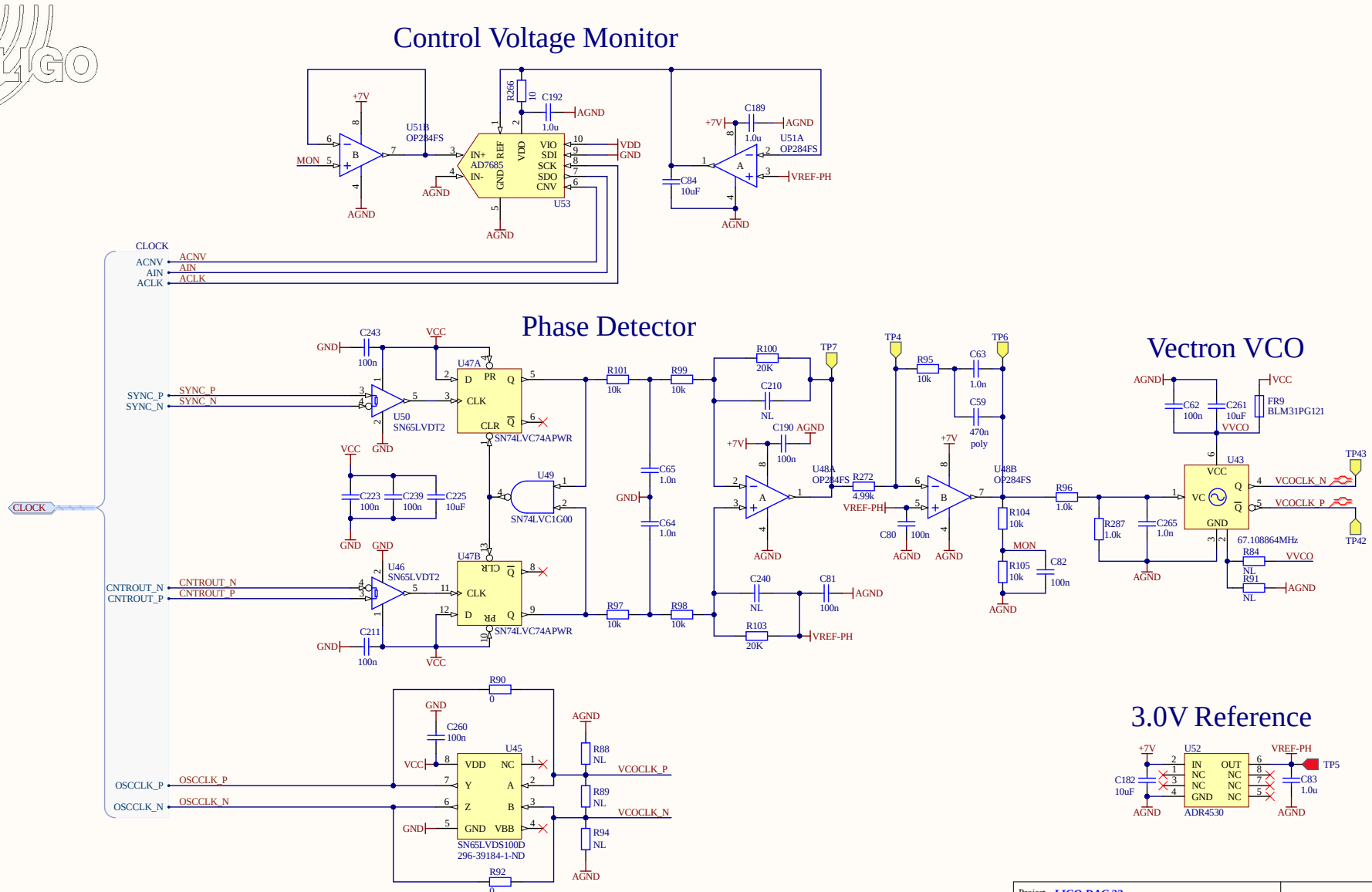


VCC Bridge

VDD Bridge

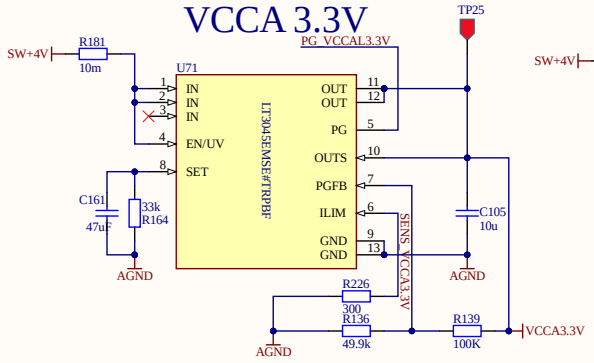


Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*FPGA Supply*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:16:47 PM	Sheet: 2 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_PowerFPGA.SchDoc			

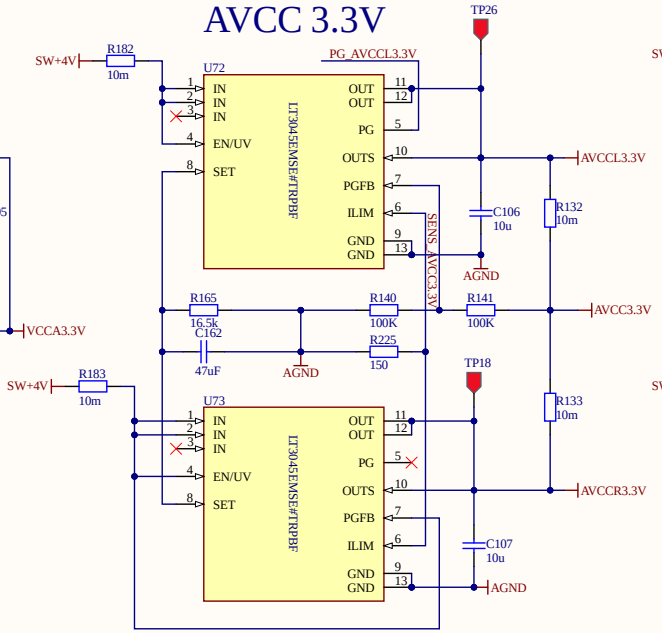

Control Voltage Monitor
Phase Detector
Vectron VCO
3.0V Reference
Optional LVPECL-LVDS Translator
U51B OP284FS
U51A OP284FS
U53 AD7685
U50 SN65LVDT2
U46 SN65LVDT2
U47A SN74LVC74APWR
U47B SN74LVC74APWR
U49 SN74LVC1G00
U48A OP284FS
U48B OP284FS
U43
U45 SN65LVDS100D
296-39184-1-ND
U52 ADR4530
MON
VREF-PH
VCOCLK_P
VCOCLK_N
OSCCLK_P
OSCCLK_N
SYNC_P
SYNC_N
CNTROUT_N
CNTROUT_P
CLOCK
ACNV
AIN
ACLK
67.108864MHz
Project LIGO DAC 32
Sheet Title VCO & Phase Detector
Size: B
DCC D2200368
Rev: 1
Date: 11/10/2022
Time: 12:16:48 PM
Sheet: 2 of 12
File: LD32_PHASE.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

DAC Linear Power Supplies

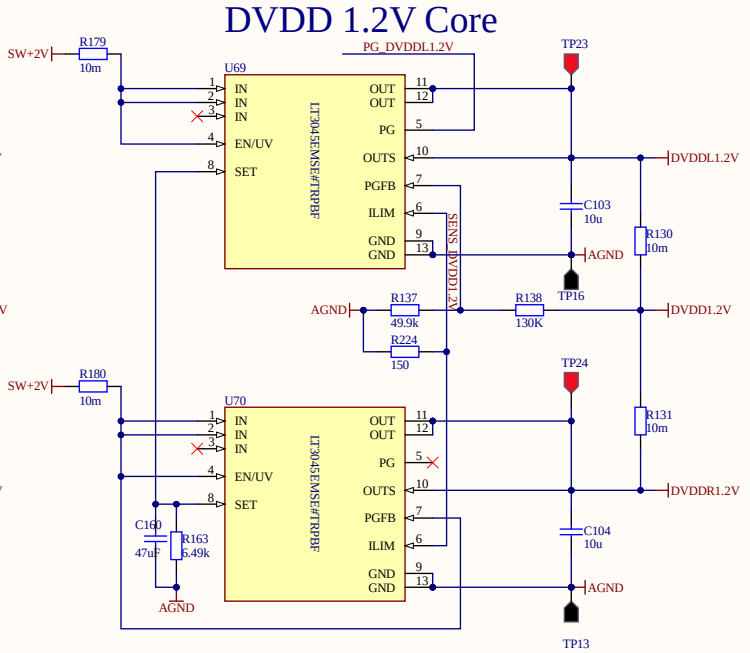
VCCA 3.3V

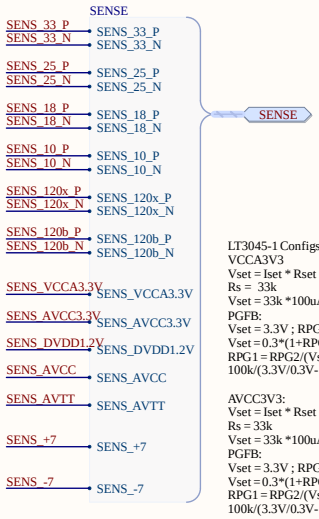


AVCC 3.3V



DVDD 1.2V Core

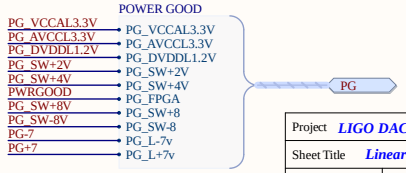




LT3045-1 Configs:
VCCA3V3
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

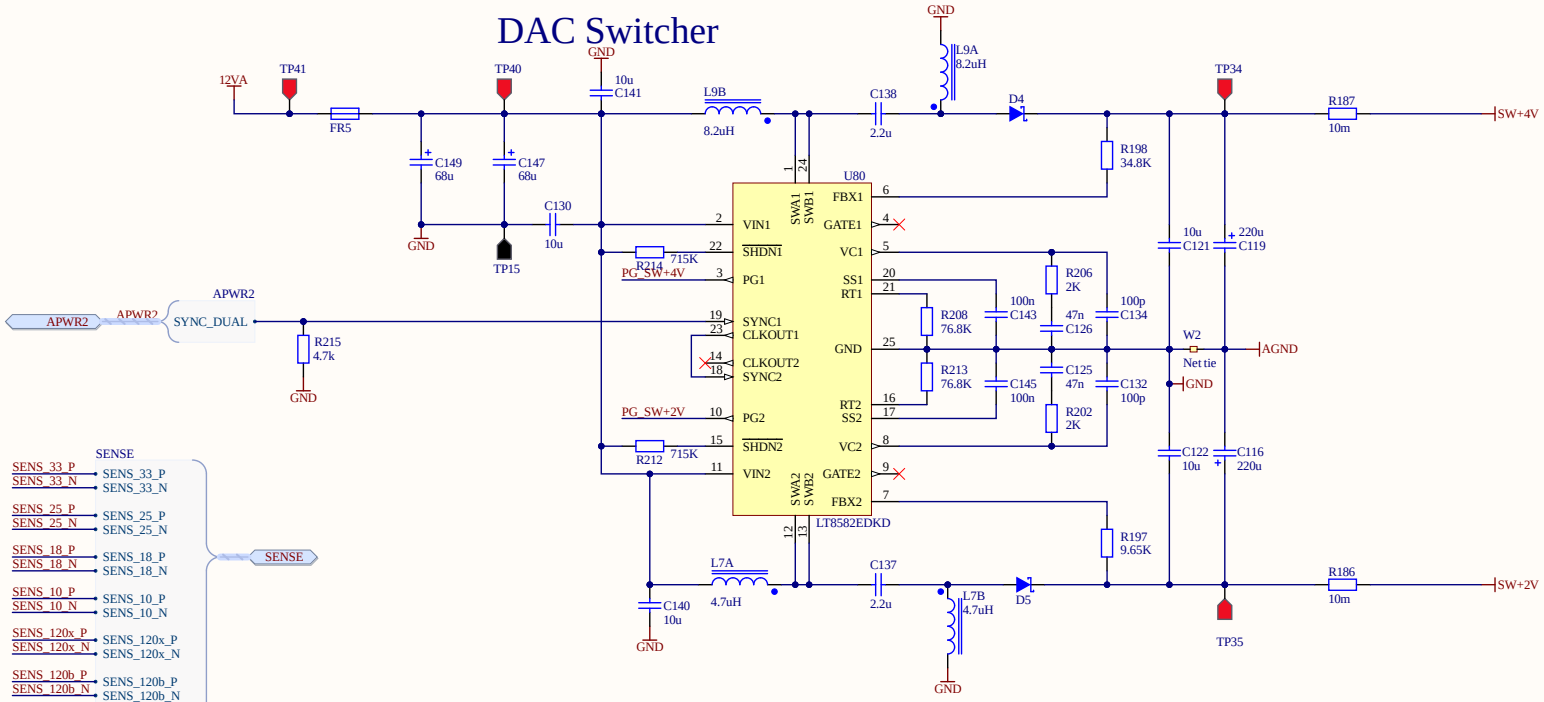
AVCC3V3:
Vset = Iset * Rset = 100uA * Rset
Rs = 33k
Vset = 33k *100uA = 3.3V
PGFB:
Vset = 3.3V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(3.3V/0.3V-1) = 10k < 11k

LT3045-1 Configs:
DVDD1V2:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k



Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Linear Supplies*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:16:49 PM	Sheet: 2 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Linear1.SchDoc			

DAC Switcher



SENSE

SENS_33_P → SENS_33_P
SENS_33_N → SENS_33_N
SENS_25_P → SENS_25_P
SENS_25_N → SENS_25_N
SENS_18_P → SENS_18_P
SENS_18_N → SENS_18_N
SENS_10_P → SENS_10_P
SENS_10_N → SENS_10_N
SENS_120x_P → SENS_120x_P
SENS_120x_N → SENS_120x_N
SENS_120b_P → SENS_120b_P
SENS_120b_N → SENS_120b_N
SENS_VCCA3.3V → SENS_VCCA3.3V
SENS_AVCC3.3V → SENS_AVCC3.3V
SENS_DVDD1.2V → SENS_DVDD1.2V
SENS_AVCC → SENS_AVCC
SENS_AVTT → SENS_AVTT
SENS_+7 → SENS_+7
SENS_-7 → SENS_-7

→ SENSE

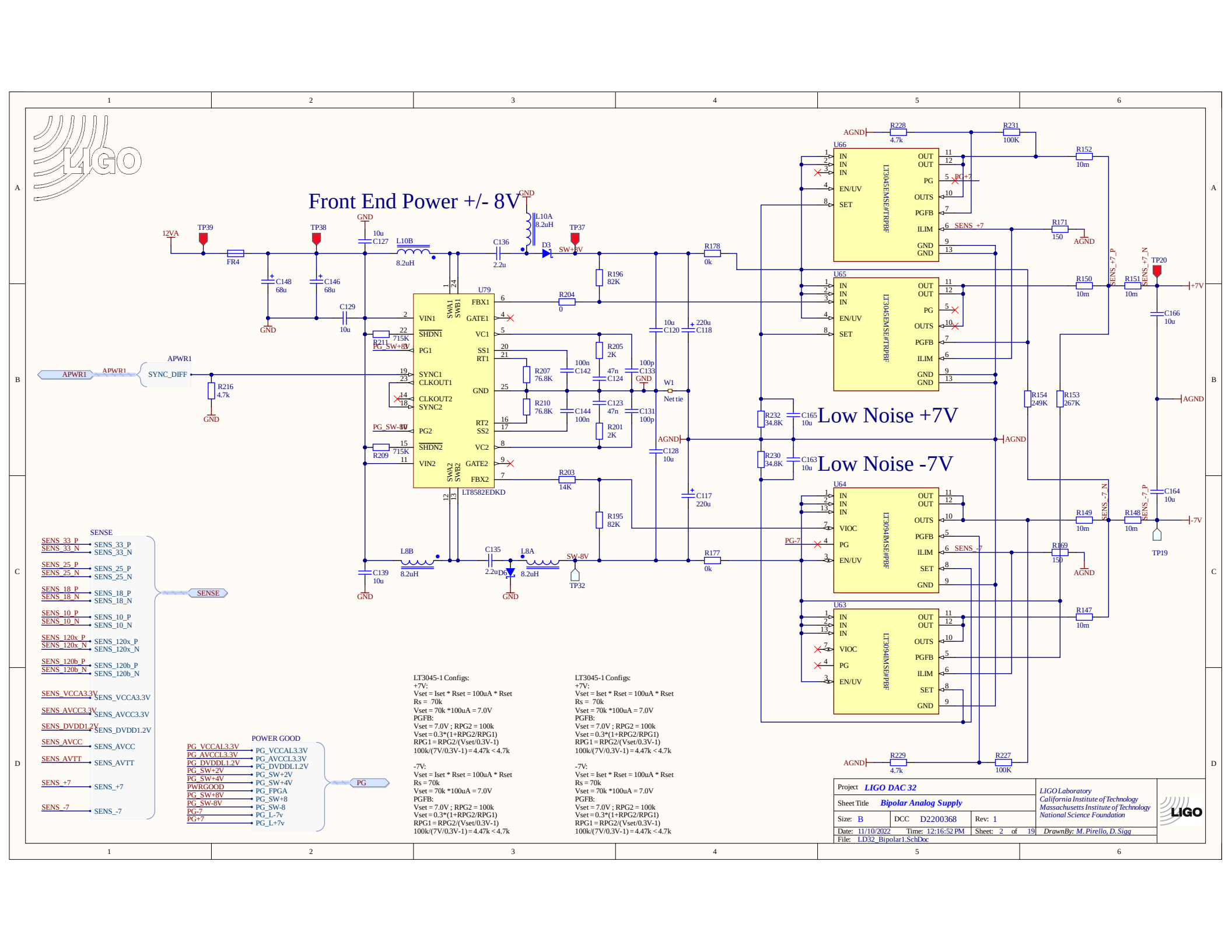
POWER GOOD

PG_VCCAL3.3V → PG_VCCAL3.3V
PG_AVCCL3.3V → PG_AVCCL3.3V
PG_DVDDL1.2V → PG_DVDDL1.2V
PG_SW+2V → PG_SW+2V
PG_SW+4V → PG_SW+4V
PWRGOOD → PG_FPGA
PG_SW+8V → PG_SW+8
PG_SW-8V → PG_SW-8
PG-7 → PG_L-7v
PG+7 → PG_L+7v

→ PG

Front End Power +/- 7V
QC per channel 5.5mA * 64 = 352mA so single supplies are sufficient
DVDD 1.2V 128 * 4 = 512mA > 500mA so two supplies
VCCA 3.3V one supply
AVDD 1.8V one suppply
AVCC_R 3.3V 90*4 = 360mA one supply
AVCC_L 3.3V 90*4 = 360mA one supply
VDD_R, VDD_L 3.3V 128 per DAC * 4 = 512mA > 500mA is two supplies

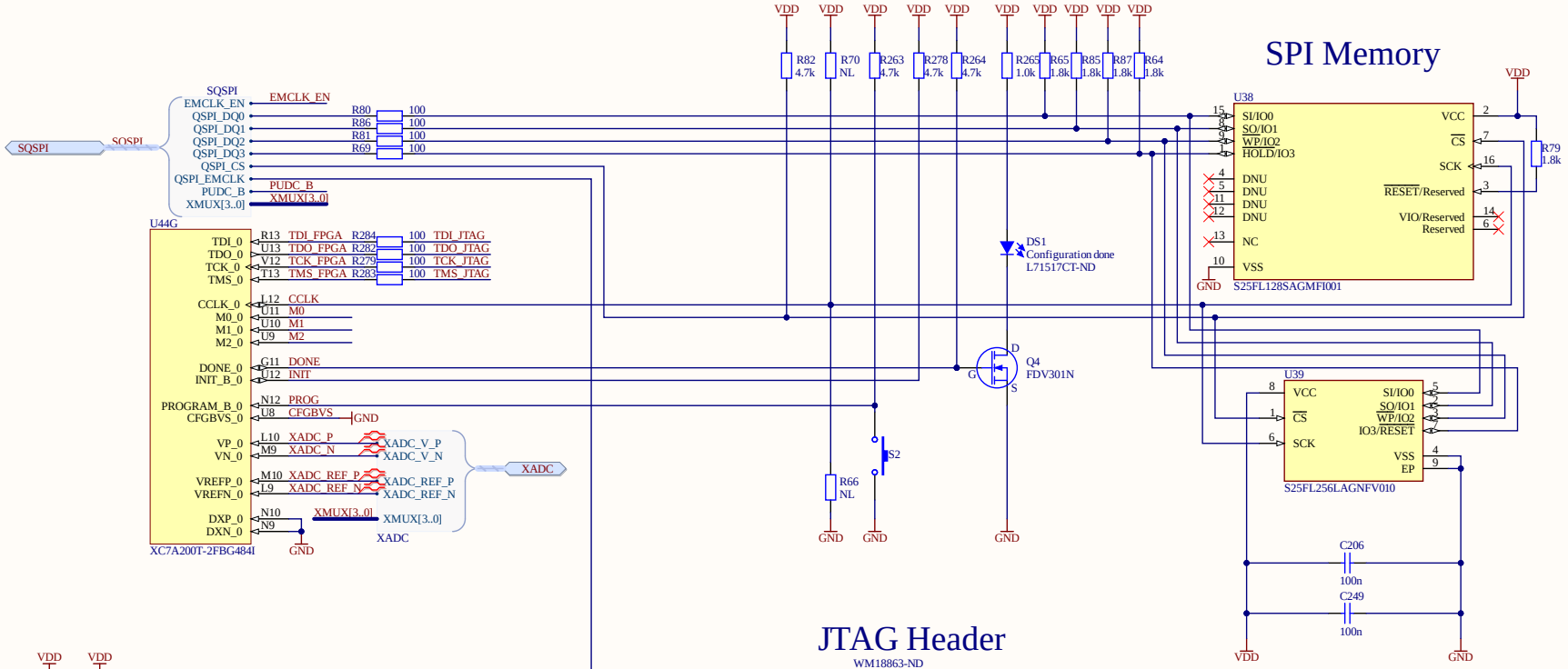
Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Dual Analog Supply*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:16:51 PM	Sheet: 2 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Bipolar2.SchDoc			


Front End Power +/- 8V
Low Noise +7V
Low Noise -7V
U79
LT8582EDKD
U66
U65
U64
U63
LT3045EMSE#TRPBF
LT3094IMSE#PBF
SENSE
POWER GOOD
PG
LT3045-1 Configs:
+7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k
-7V:
Vset = Iset * Rset = 100uA * Rset
Rs = 70k
Vset = 70k *100uA = 7.0V
PGFB:
Vset = 7.0V ; RPG2 = 100k
Vset = 0.3*(1+RPG2/RPG1)
RPG1 = RPG2/(Vset/0.3V-1)
100k/(7V/0.3V-1) = 4.47k < 4.7k
Project LIGO DAC 32
Sheet Title Bipolar Analog Supply
Size: B
DCC D2200368
Rev: 1
Date: 11/10/2022
Time: 12:16:52 PM
Sheet: 2 of 19
File: LD32_Bipolar1.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

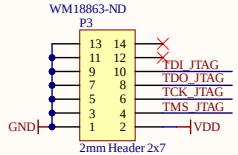
JTAG and SPI Flash

VDD is 1.8V for this design

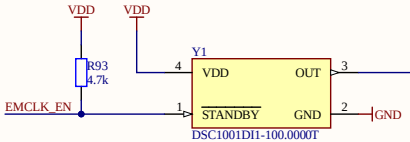
SPI Memory

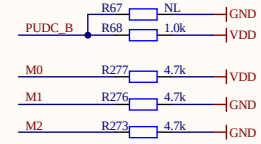


JTAG Header

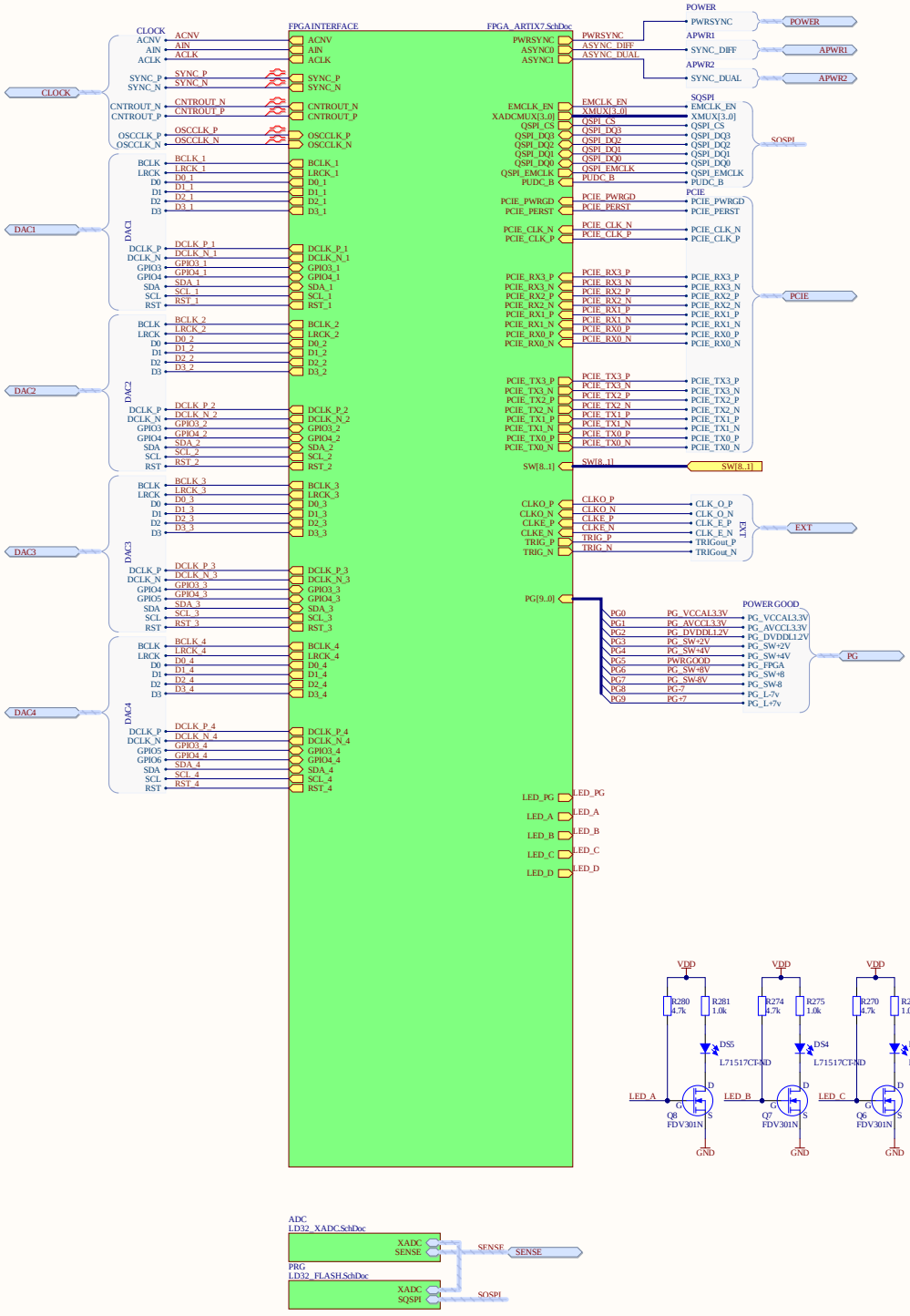


100 MHz Program Clock

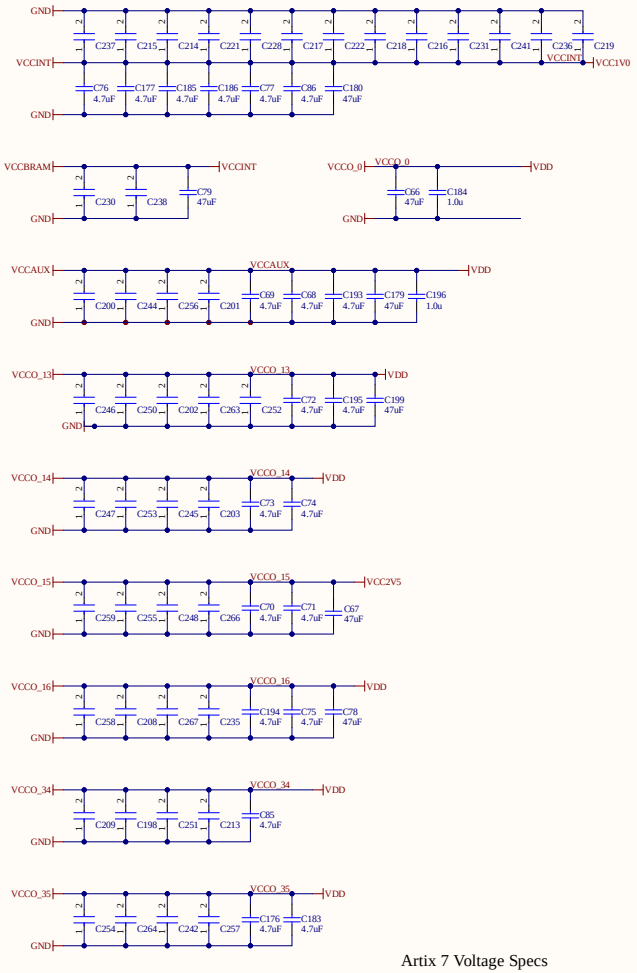




Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:16:53 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FLASH.SchDoc			



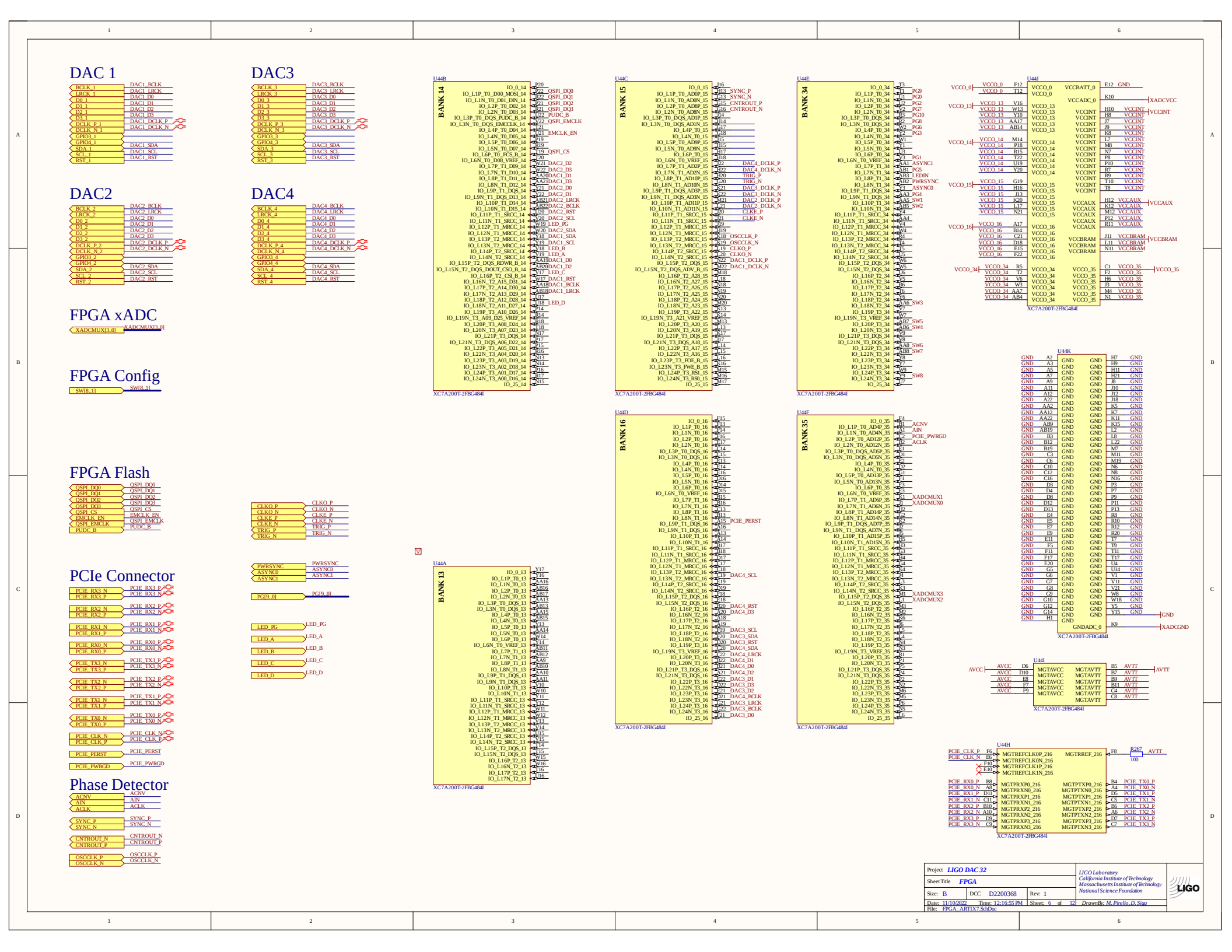
FPGA Decoupling Caps



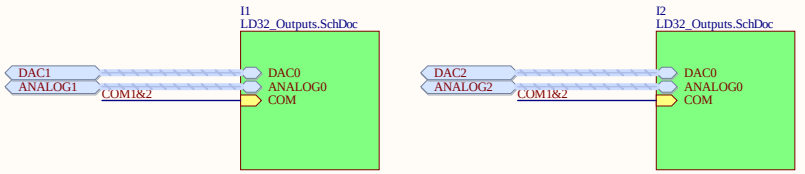
Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

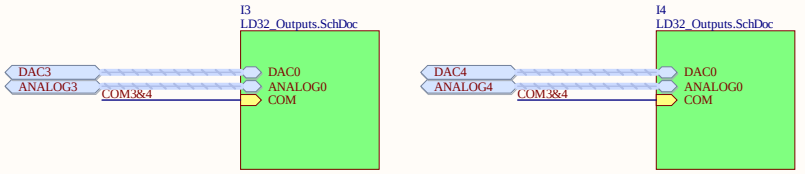
LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

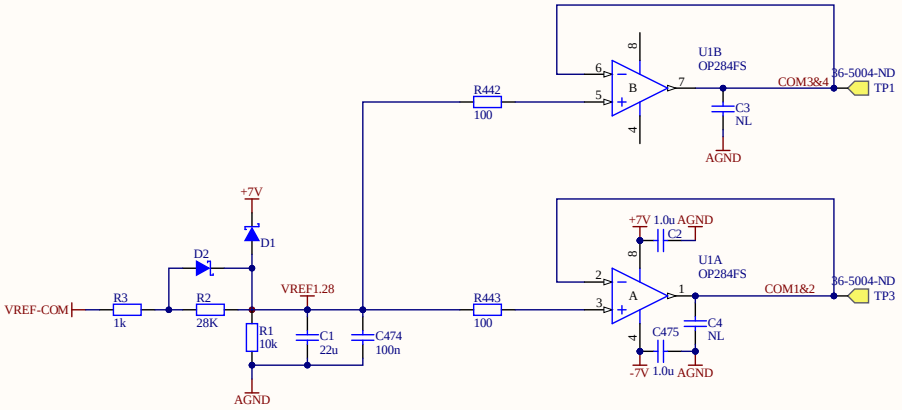
Project: *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title: *FPGA Top*			
Size: B	DCC: D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:16:54 PM	Sheet 5 of 12	*Drawn By: M. Pirello, D. Sigg*
File: LD32_FPGA.SchDoc			


DAC 1
BCLK_1
LRCK_1
D0_1
D1_1
D2_1
D3_1
DCLK_P_1
DCLK_N_1
GPIO3_1
GPIO4_1
SDA_1
SCL_1
RST_1
DAC1_BCLK
DAC1_LRCK
DAC1_D0
DAC1_D1
DAC1_D2
DAC1_D3
DAC1_DCLK_P
DAC1_DCLK_N
DAC1_SDA
DAC1_SCL
DAC1_RST
DAC3
BCLK_3
LRCK_3
D0_3
D1_3
D2_3
D3_3
DCLK_P_3
DCLK_N_3
GPIO3_3
GPIO4_3
SDA_3
SCL_3
RST_3
DAC3_BCLK
DAC3_LRCK
DAC3_D0
DAC3_D1
DAC3_D2
DAC3_D3
DAC3_DCLK_P
DAC3_DCLK_N
DAC3_SDA
DAC3_SCL
DAC3_RST
DAC2
BCLK_2
LRCK_2
D0_2
D1_2
D2_2
D3_2
DCLK_P_2
DCLK_N_2
GPIO3_2
GPIO4_2
SDA_2
SCL_2
RST_2
DAC2_BCLK
DAC2_LRCK
DAC2_D0
DAC2_D1
DAC2_D2
DAC2_D3
DAC2_DCLK_P
DAC2_DCLK_N
DAC2_SDA
DAC2_SCL
DAC2_RST
DAC4
BCLK_4
LRCK_4
D0_4
D1_4
D2_4
D3_4
DCLK_P_4
DCLK_N_4
GPIO3_4
GPIO4_4
SDA_4
SCL_4
RST_4
DAC4_BCLK
DAC4_LRCK
DAC4_D0
DAC4_D1
DAC4_D2
DAC4_D3
DAC4_DCLK_P
DAC4_DCLK_N
DAC4_SDA
DAC4_SCL
DAC4_RST
FPGA xADC
XADCMUX[3..0]
XADCMUX[3..0]
FPGA Config
SW[8..1]
SW8..1
FPGA Flash
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CS
EMCLK_EN
QSPI_EMCLK
PUDC_B
CLKO_P
CLKO_N
CLKE_P
CLKE_N
TRIG_P
TRIG_N
PWRSYNC
ASYNCD
ASYNC1
PG[9..0]
LED_PG
LED_A
LED_B
LED_C
LED_D
PCIe Connector
PCIE_RX3_P
PCIE_RX3_N
PCIE_RX2_P
PCIE_RX2_N
PCIE_RX1_P
PCIE_RX1_N
PCIE_RX0_P
PCIE_RX0_N
PCIE_TX3_P
PCIE_TX3_N
PCIE_TX2_P
PCIE_TX2_N
PCIE_TX1_P
PCIE_TX1_N
PCIE_TX0_P
PCIE_TX0_N
PCIE_CLK_N
PCIE_CLK_P
PCIE_PERST
PCIE_PWRGD
Phase Detector
ACNV
AIN
ACLK
SYNC_P
SYNC_N
CNTROUT_N
CNTROUT_P
OSCCLK_P
OSCCLK_N
U44B
BANK 14
XC7A200T-2FBG484I
U44C
BANK 15
XC7A200T-2FBG484I
U44E
BANK 34
XC7A200T-2FBG484I
U44J
XC7A200T-2FBG484I
U44K
XC7A200T-2FBG484I
U44D
BANK 16
XC7A200T-2FBG484I
U44F
BANK 35
XC7A200T-2FBG484I
U44A
BANK 13
XC7A200T-2FBG484I
U44I
XC7A200T-2FBG484I
U44H
XC7A200T-2FBG484I
Project LIGO DAC 32
Sheet Title FPGA
Size: B
DCC D2200368
Rev: 1
Date: 11/10/2022
Time: 12:16:55 PM
Sheet 6 of 12
File: FPGA_ARTIX7.SchDoc
Drawn By: M.Pirello, D.Sigg
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
LIGO

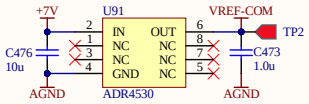
Multiple DAC's COM Distro







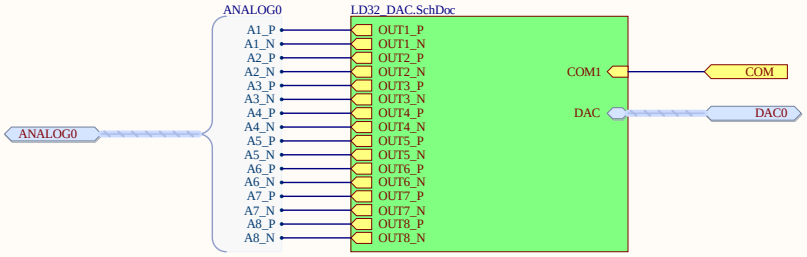
3.0V COM Reference



Parts Checked for Value and Consistency

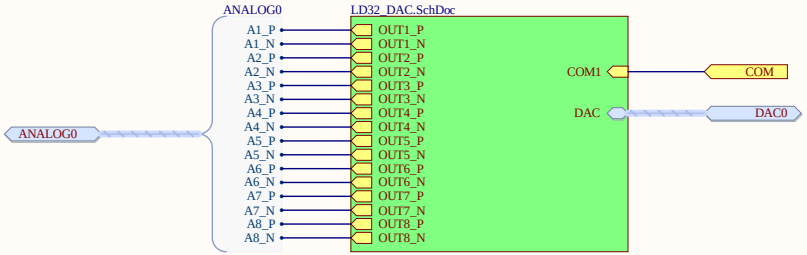
Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Top*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:16:56 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Analog.SchDoc			

DAC Overview



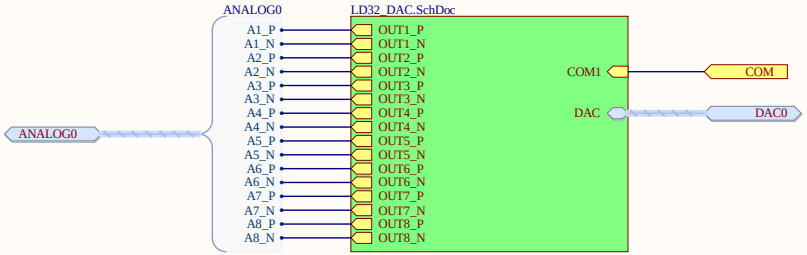
Project	***LIGO DAC 32***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Overview***		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:16:56 PM	Sheet: 9 of 19		*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Outputs.SchDoc			

DAC Overview



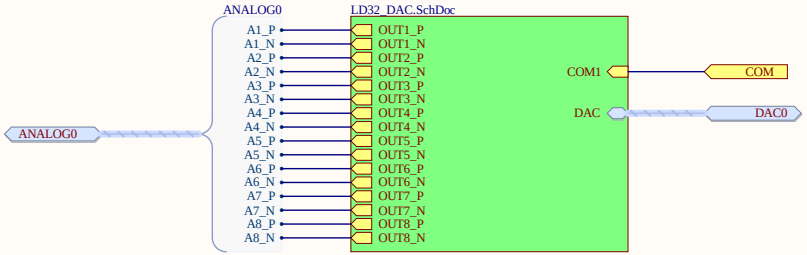
Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Overview*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:16:57 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Outputs.SchDoc			

DAC Overview

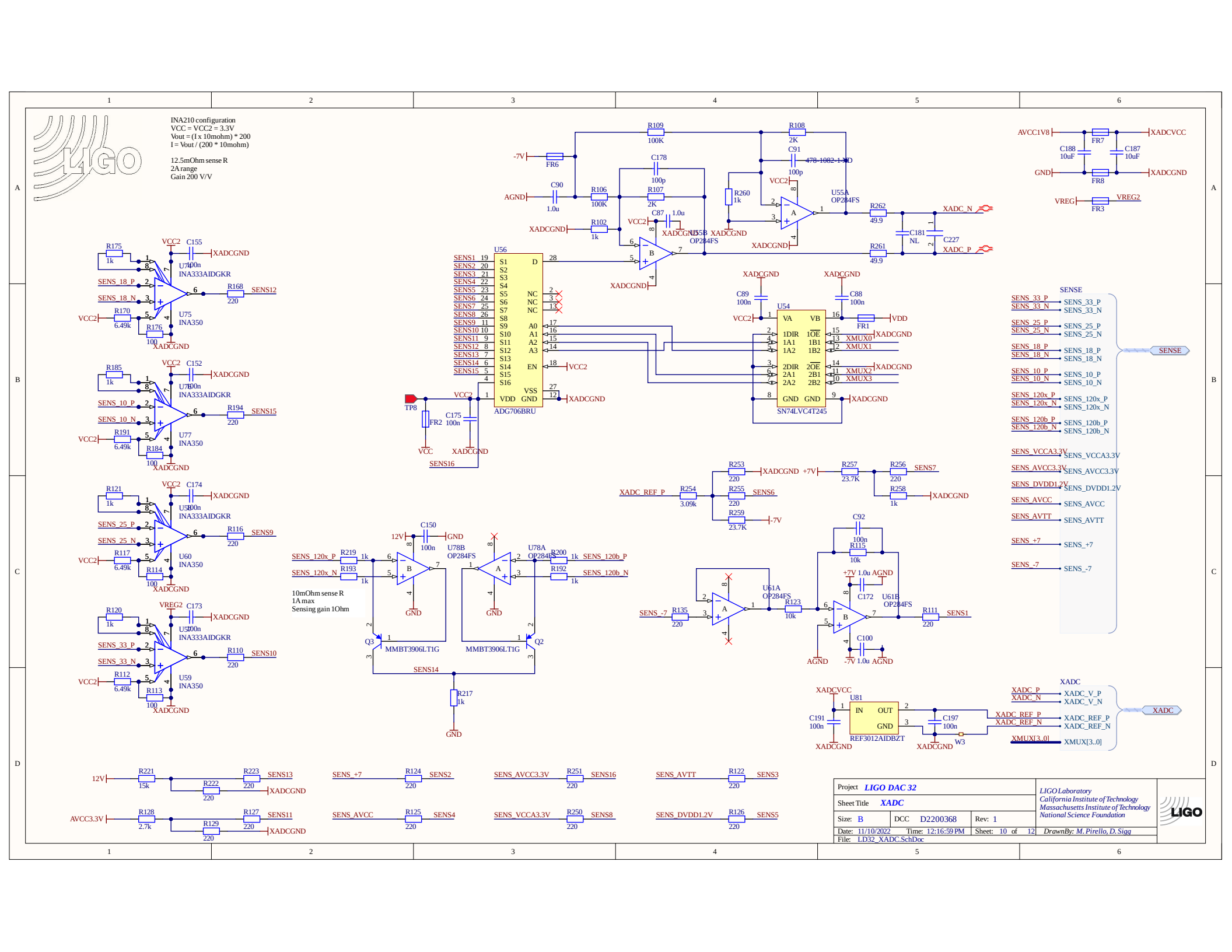


Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *DAC Overview*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:16:57 PM		Sheet: 9 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_Outputs.SchDoc			

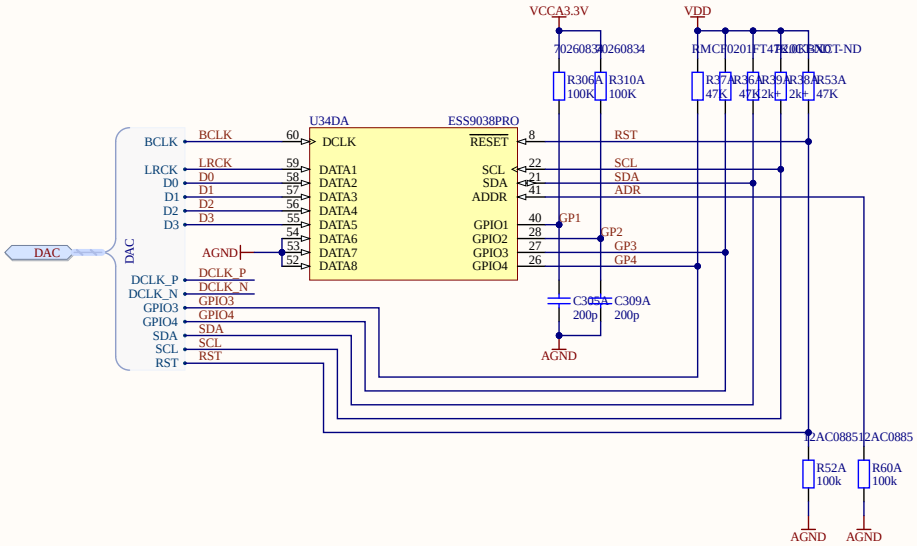
DAC Overview



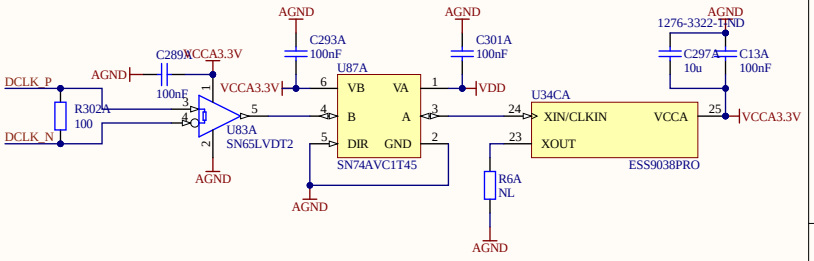
Project	***LIGO DAC 32***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***DAC Overview***		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:16:58 PM	Sheet: 9 of 19	*DrawnBy: M. Pirello, D. Sigg*	
File: LD32_Outputs.SchDoc			


INA210 configuration
VCC = VCC2 = 3.3V
Vout = (I x 10mohm) * 200
I = Vout / (200 * 10mohm)
12.5mOhm sense R
2A range
Gain 200 V/V
INA333AIDGKR
INA350
OP284FS
ADG706BRU
SN74LVC4T245
REF3012AIDBZT
MMBT3906LT1G
10mOhm sense R
1A max
Sensing gain 1Ohm
SENSE
XADC
Project LIGO DAC 32
Sheet Title XADC
Size: B
DCC D2200368
Rev: 1
Date: 11/10/2022
Time: 12:16:59 PM
Sheet: 10 of 12
File: LD32_XADC.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

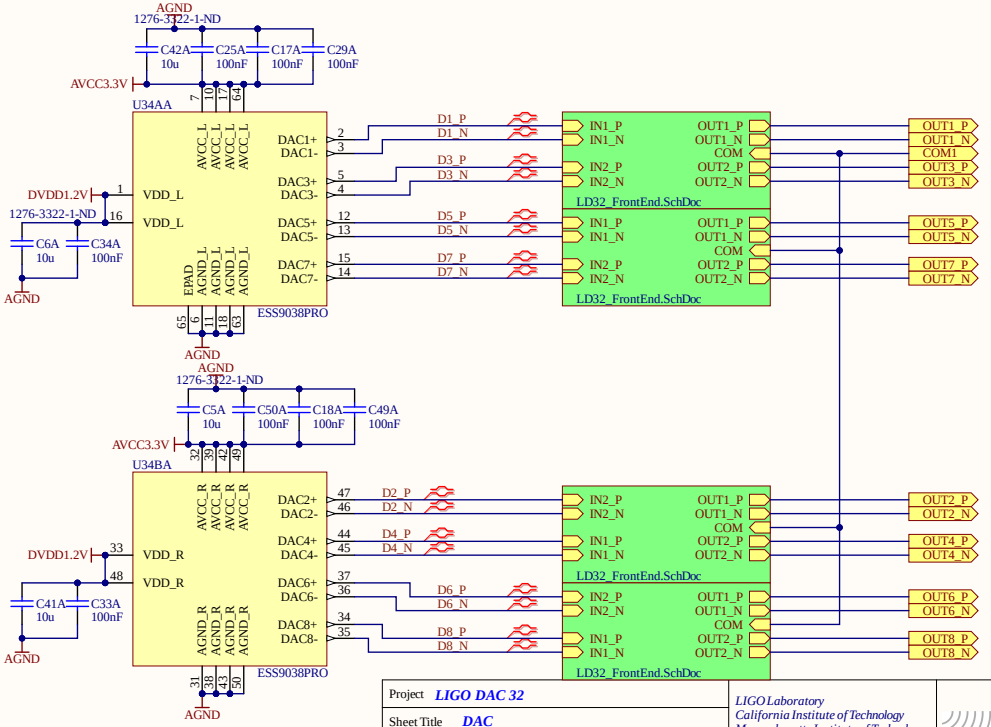
DAC Inputs



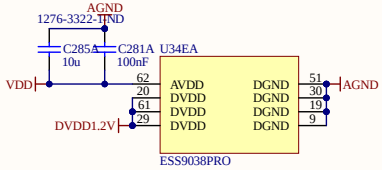
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

You also routed more lines than we really need.

1 fast clock (LVDS, SN65LVDS104 for FO)
1 BCLK
1 LRCLK
4 D lines
2 I2C lines
is needed per DAC.

There will be a difference between Artix-7 and Artix Ultrascale with later only supporting 1.8V.

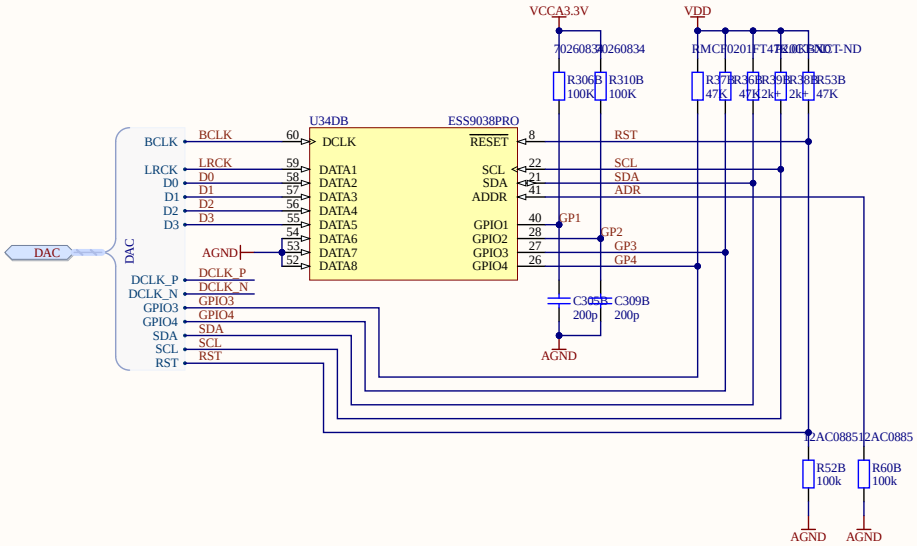
Daniel

Parts Checked for Value and Consistency

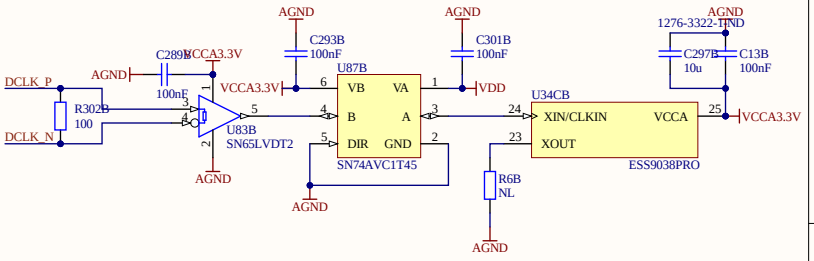
Project	*LIGO DAC 32*		
Sheet Title	*DAC*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:17:01 PM	Sheet: 10 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_DAC.SchDoc			

LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation

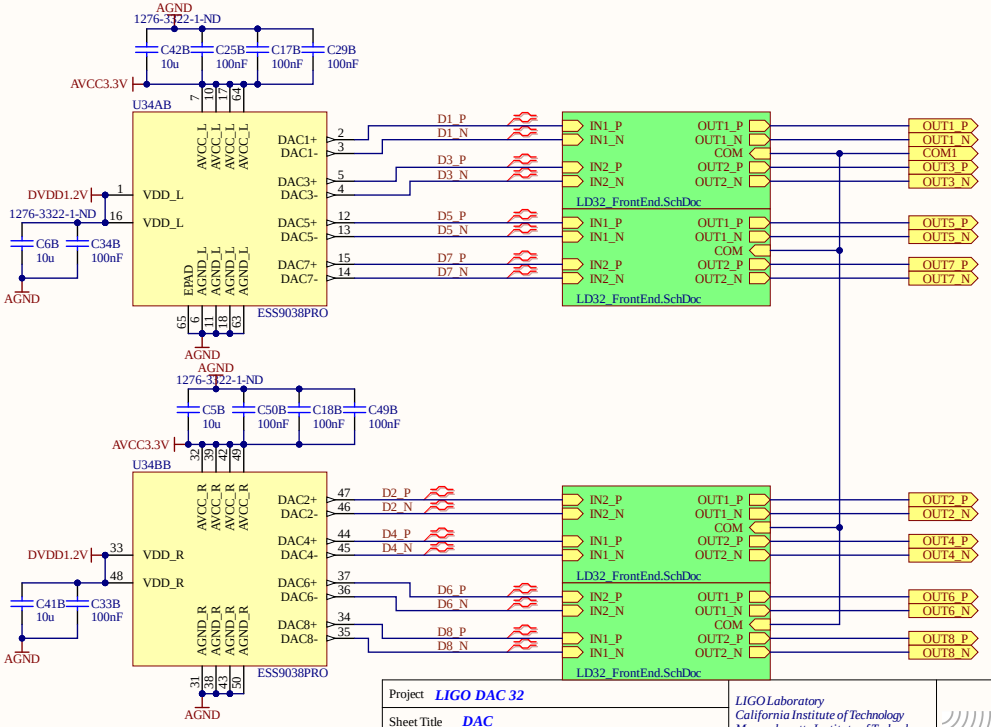
DAC Inputs



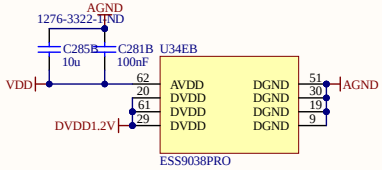
Main Clock



DAC Outputs



Core Power



Clock lines and reset could be shared in principle.

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Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		
Sheet Title	*DAC*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:17:01 PM	Sheet: 10 of 19	DrawnBy: M. Pirello, D. Sigg
File: LD32_DAC.SchDoc			

LIGO Laboratory
California Institute of Technology
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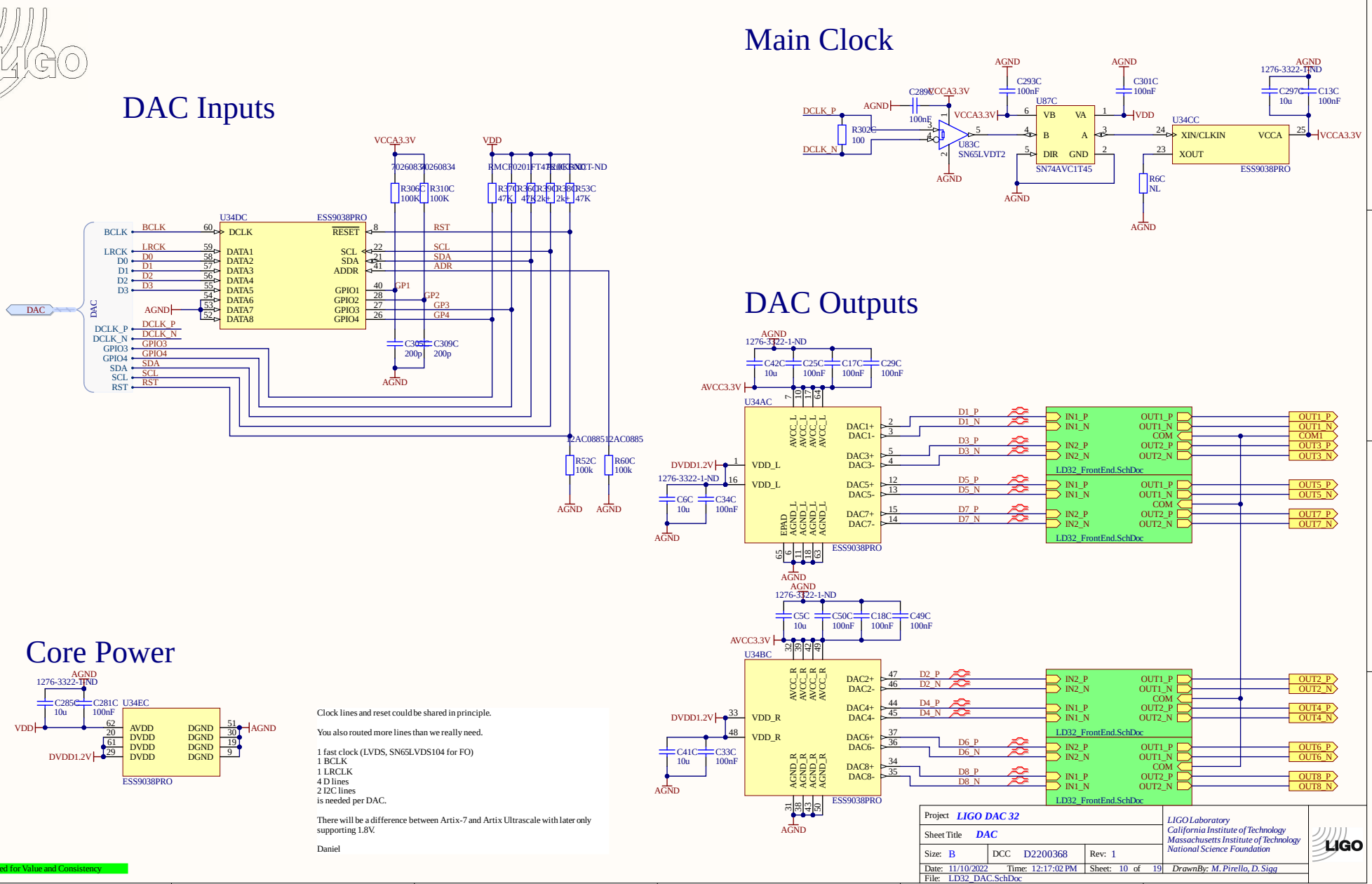
DAC Inputs
Main Clock
DAC Outputs
Core Power
U34DC
ESS9038PRO
U87C
U83C
SN65LVDT2
SN74AVC1T45
U34CC
U34AC
U34BC
U34EC
LD32_FrontEnd.SchDoc
Clock lines and reset could be shared in principle.
You also routed more lines than we really need.
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1 LRCLK
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2 I2C lines
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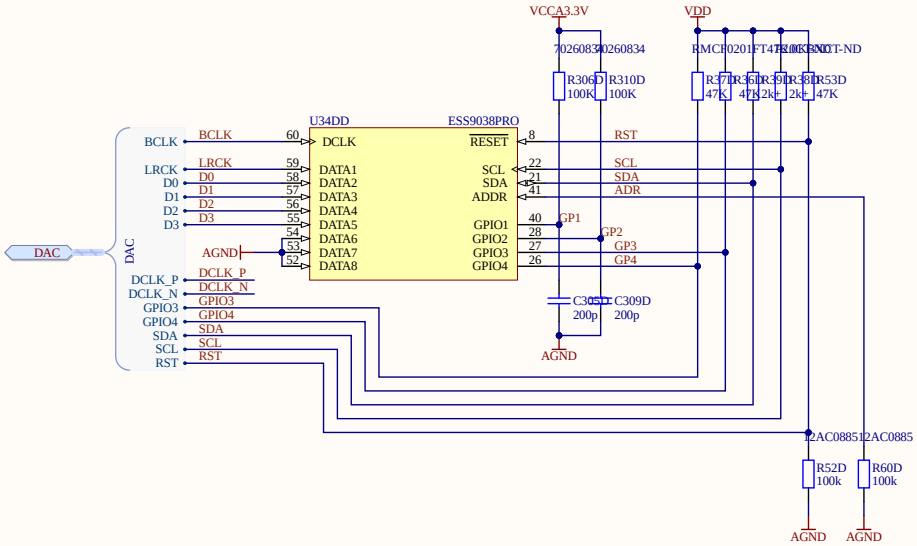
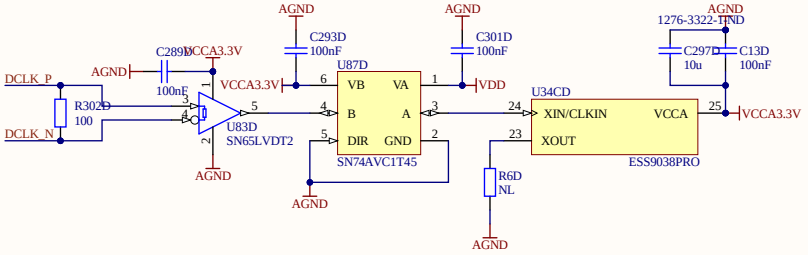
Daniel
Parts Checked for Value and Consistency
Project LIGO DAC 32
Sheet Title DAC
Size: B
DCC D2200368
Rev: 1
Date: 11/10/2022
Time: 12:17:02 PM
Sheet: 10 of 19
File: LD32_DAC.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello, D. Sigg

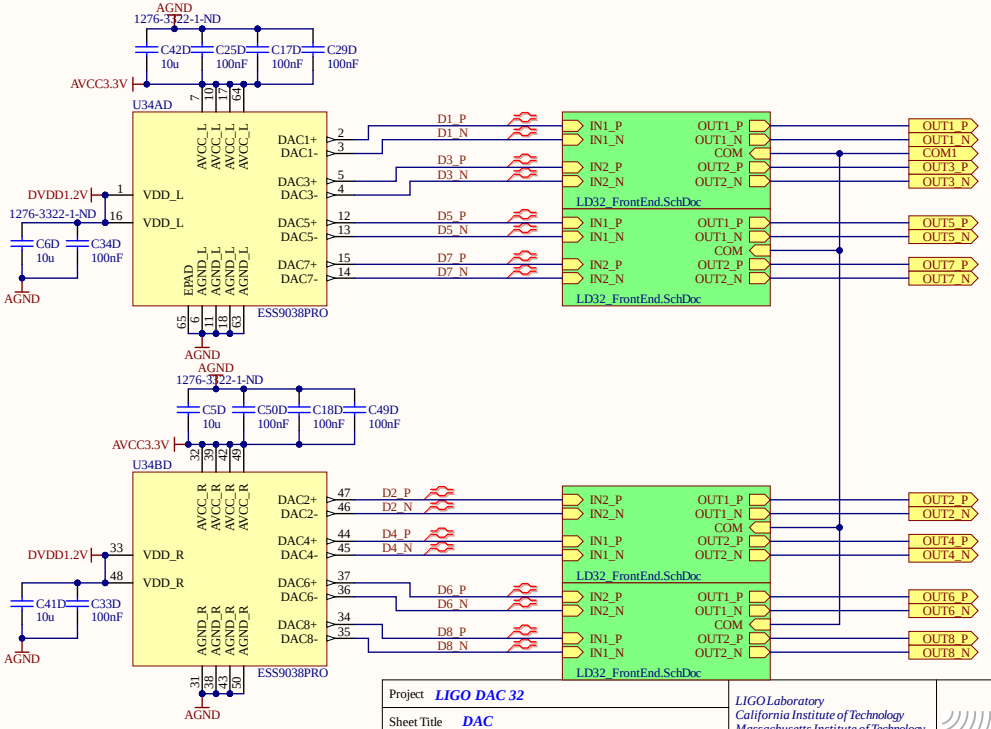
DAC Inputs



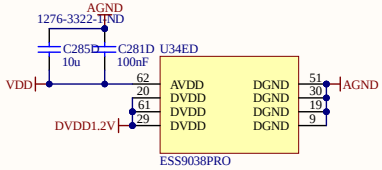
Main Clock



DAC Outputs



Core Power



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Daniel

Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		
Sheet Title	*DAC*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:17:02 PM	Sheet: 10 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_DAC.SchDoc			

LIGO Laboratory
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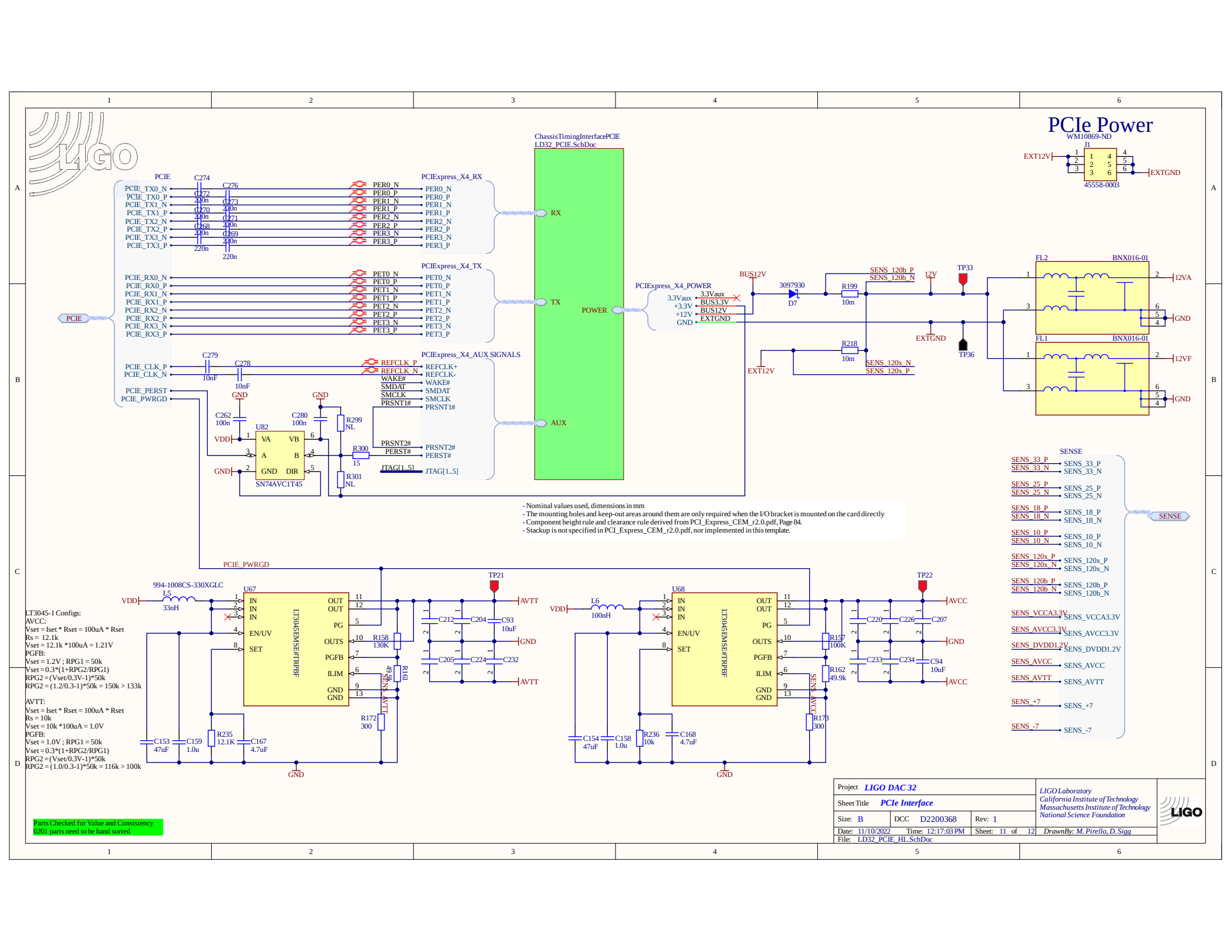
LIGO

PCIe Power



- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

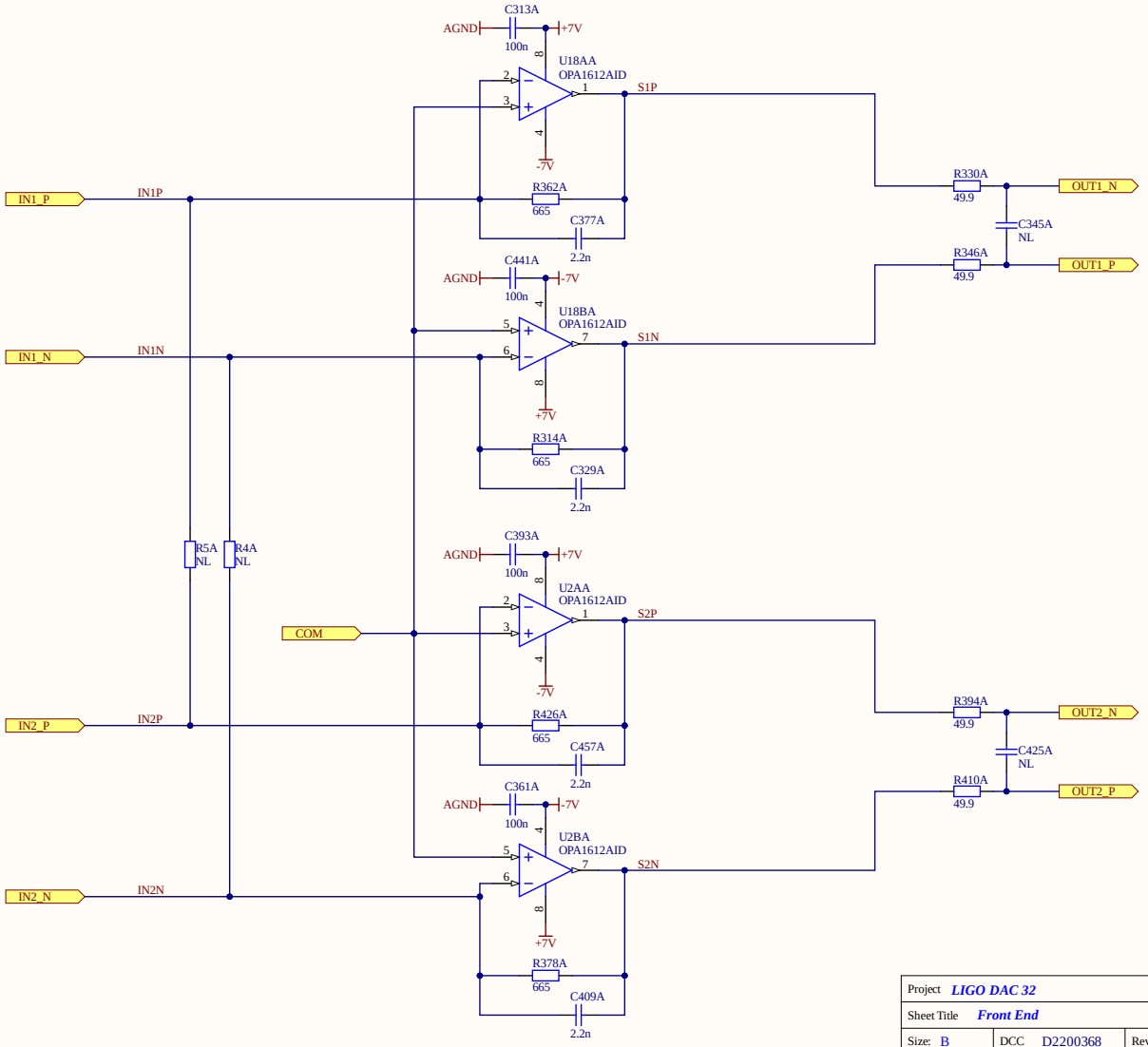
LT3045-1 Configs:
AVCC:
Vset = Iset * Rset = 100uA * Rset
Rs = 12.1k
Vset = 12.1k *100uA = 1.21V
PGFB:
Vset = 1.2V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.2/0.3-1)*50k = 150k > 133k

AVTT:
Vset = Iset * Rset = 100uA * Rset
Rs = 10k
Vset = 10k *100uA = 1.0V
PGFB:
Vset = 1.0V ; RPG1 = 50k
Vset = 0.3*(1+RPG2/RPG1)
RPG2 = (Vset/0.3V-1)*50k
RPG2 = (1.0/0.3-1)*50k = 116k > 100k

Parts Checked for Value and Consistency
0201 parts need to be hand sorted

Project	LIGO DAC 32		LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation
Sheet Title	PCIe Interface		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022	Time: 12:17:03 PM	Sheet: 11 of 12	DrawnBy: M. Pirello, D. Sigg
File: LD32_PCIE_HL.SchDoc			

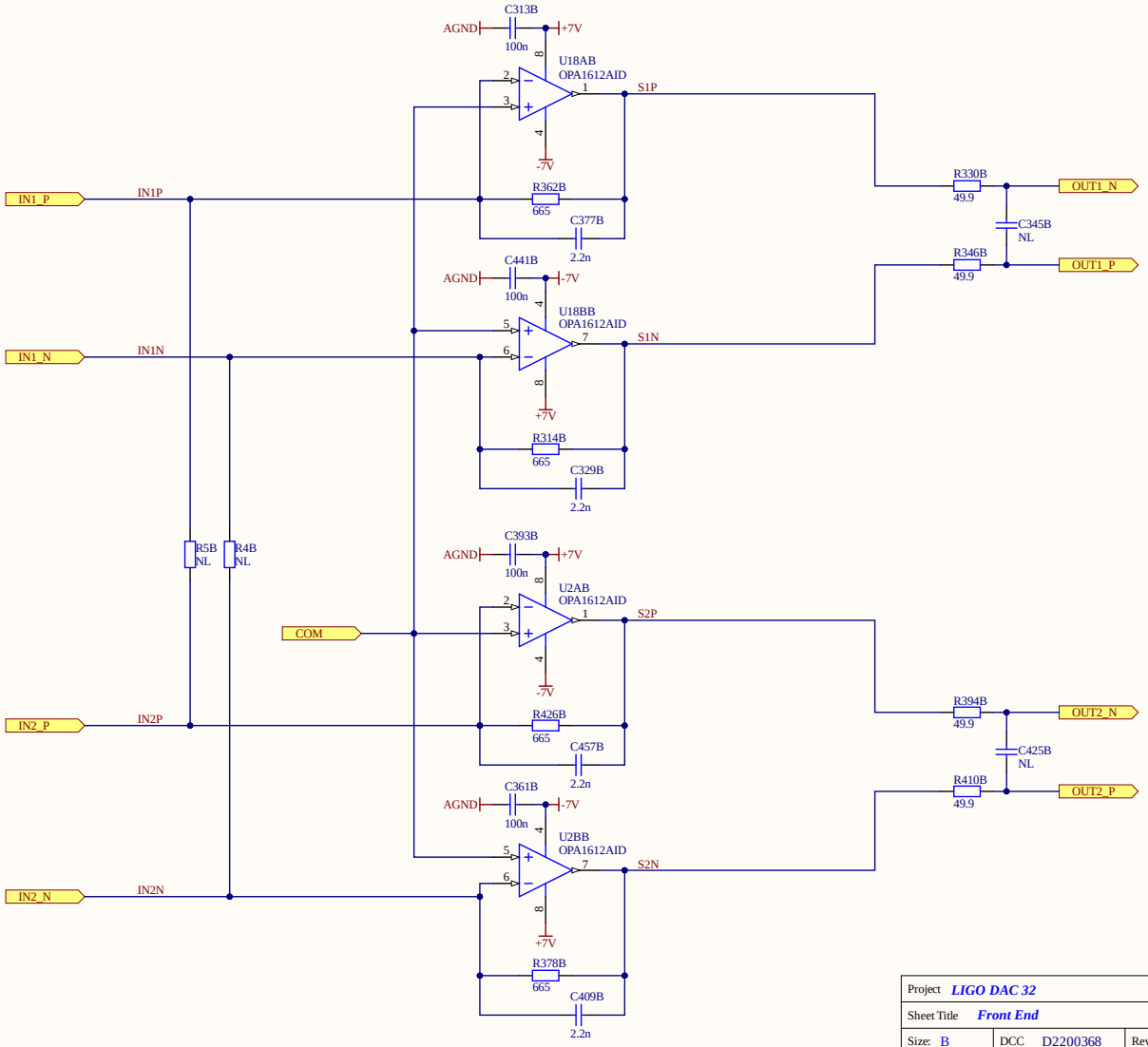
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:04 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

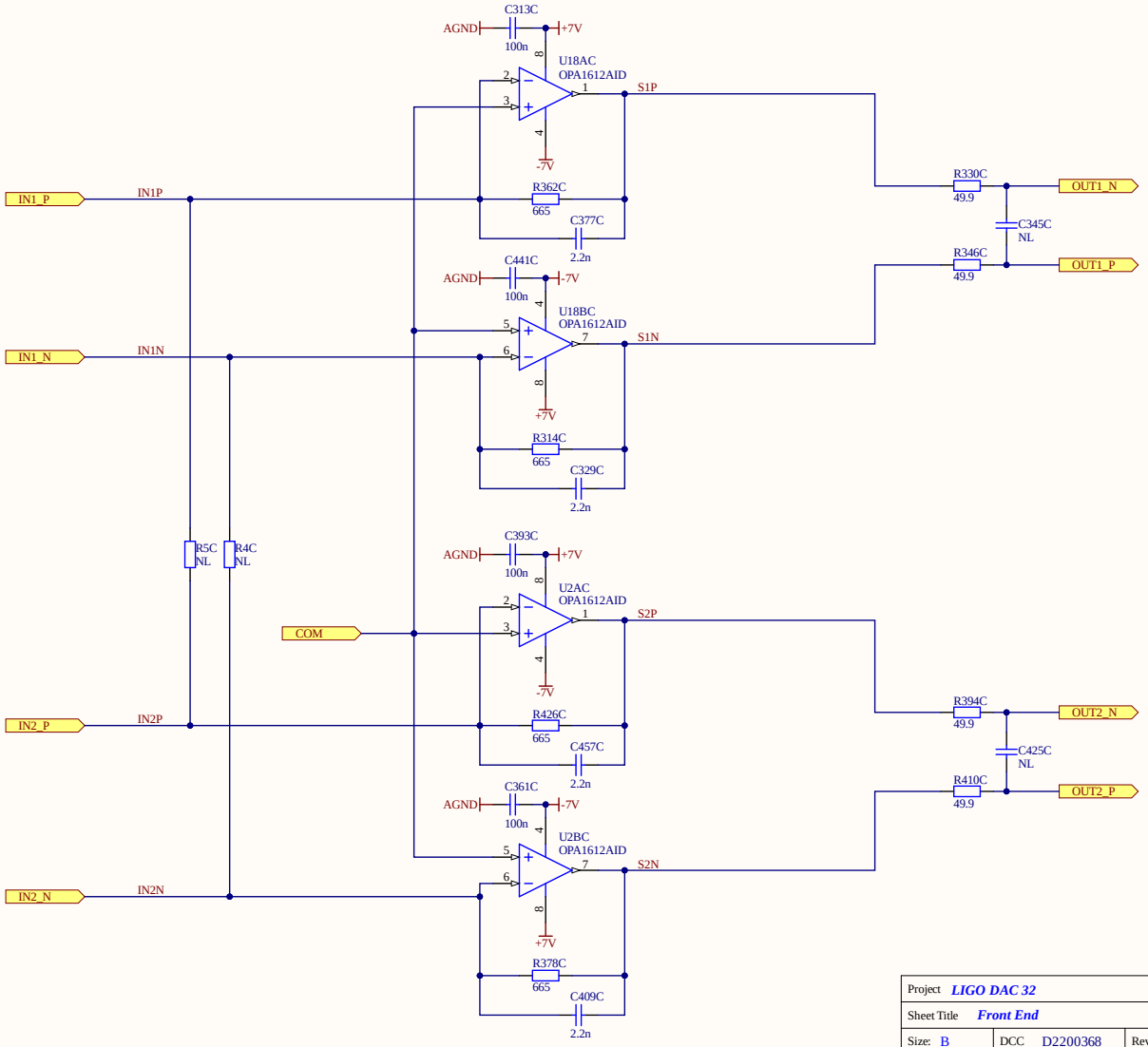
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:04 PM	Sheet: 11 of 19		*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

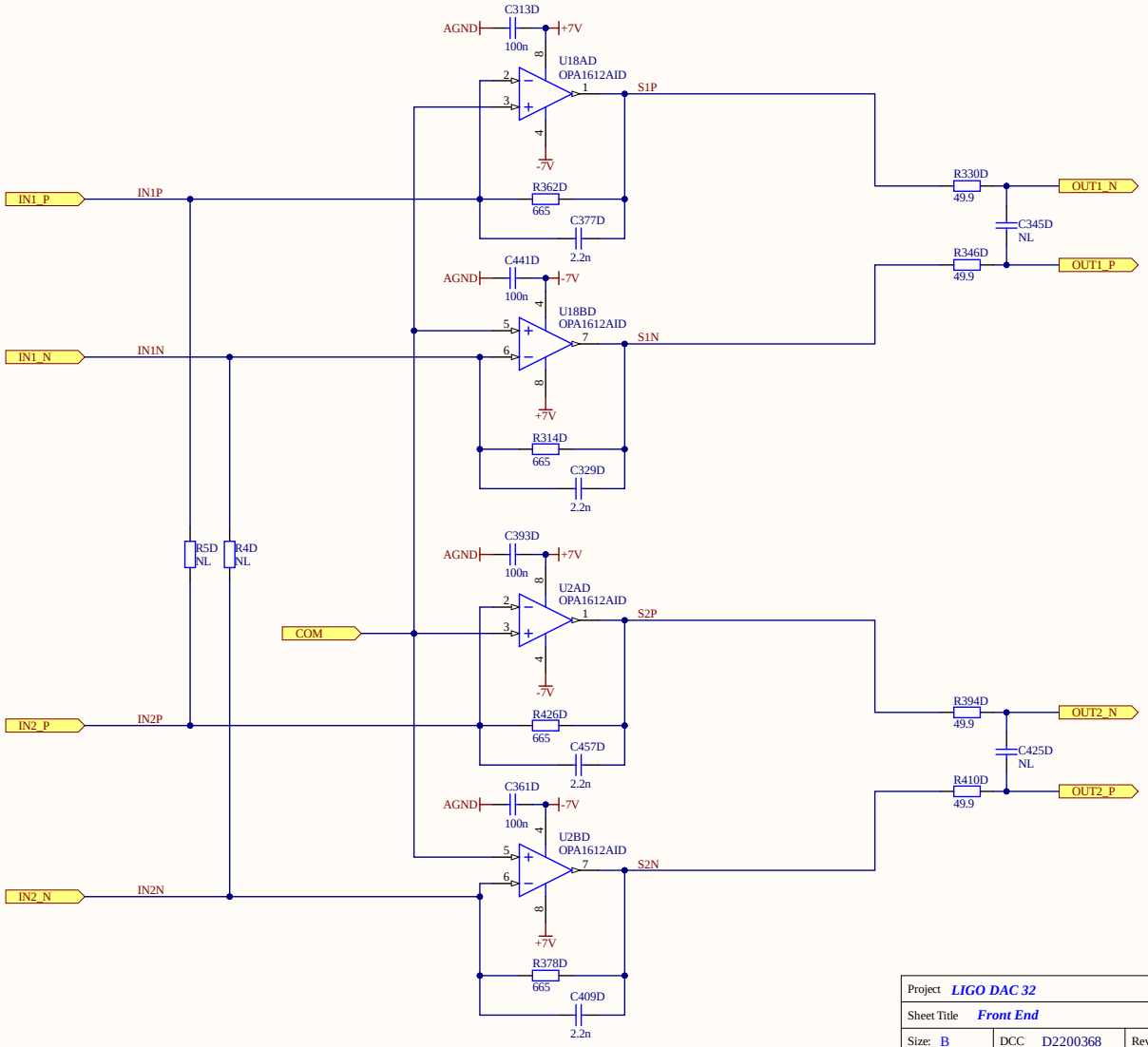
Front End Amplifiers



Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:04 PM	Sheet: 11 of 19		*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

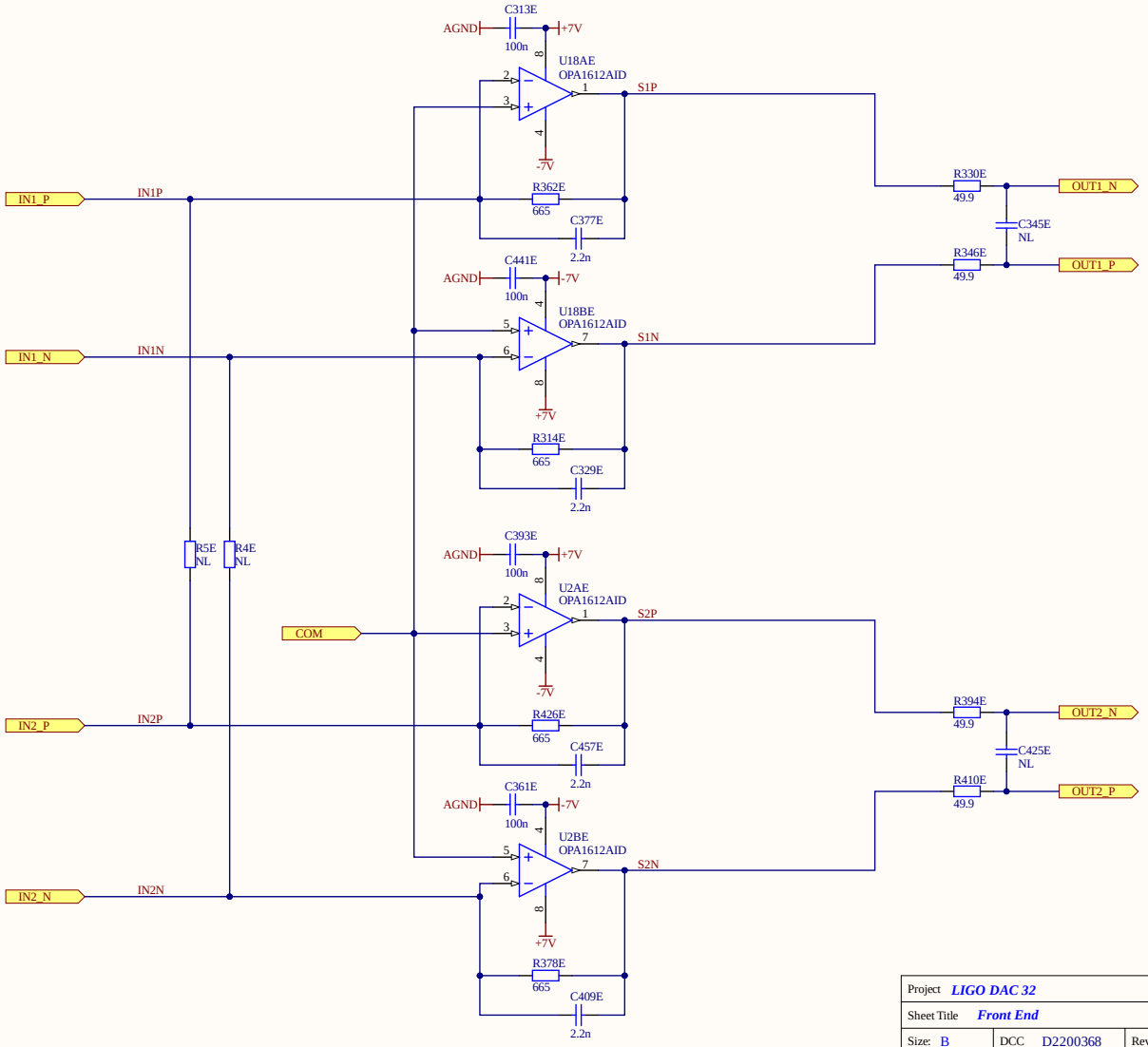
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:05 PM	Sheet: 11 of 19		*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

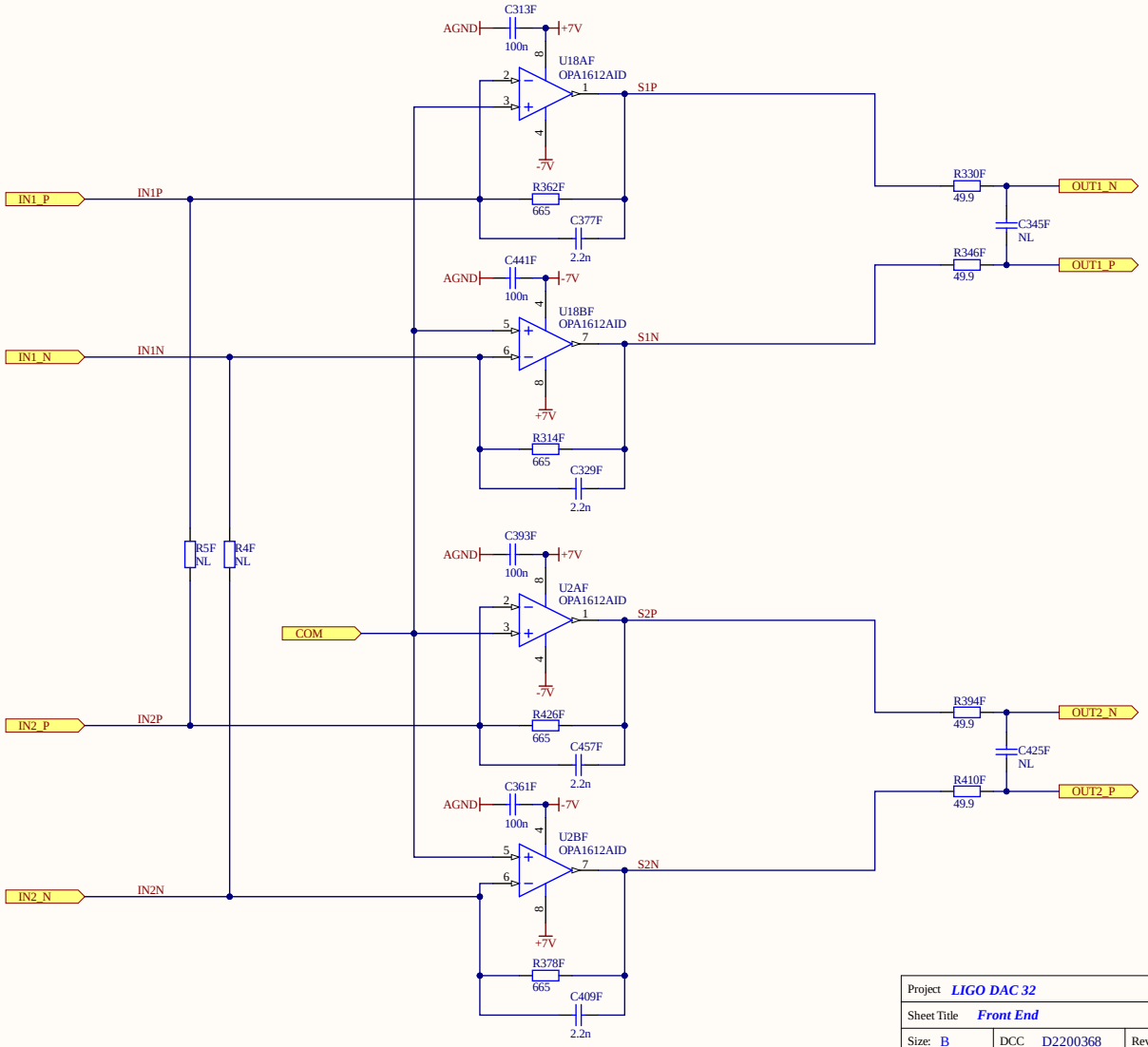
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:05 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

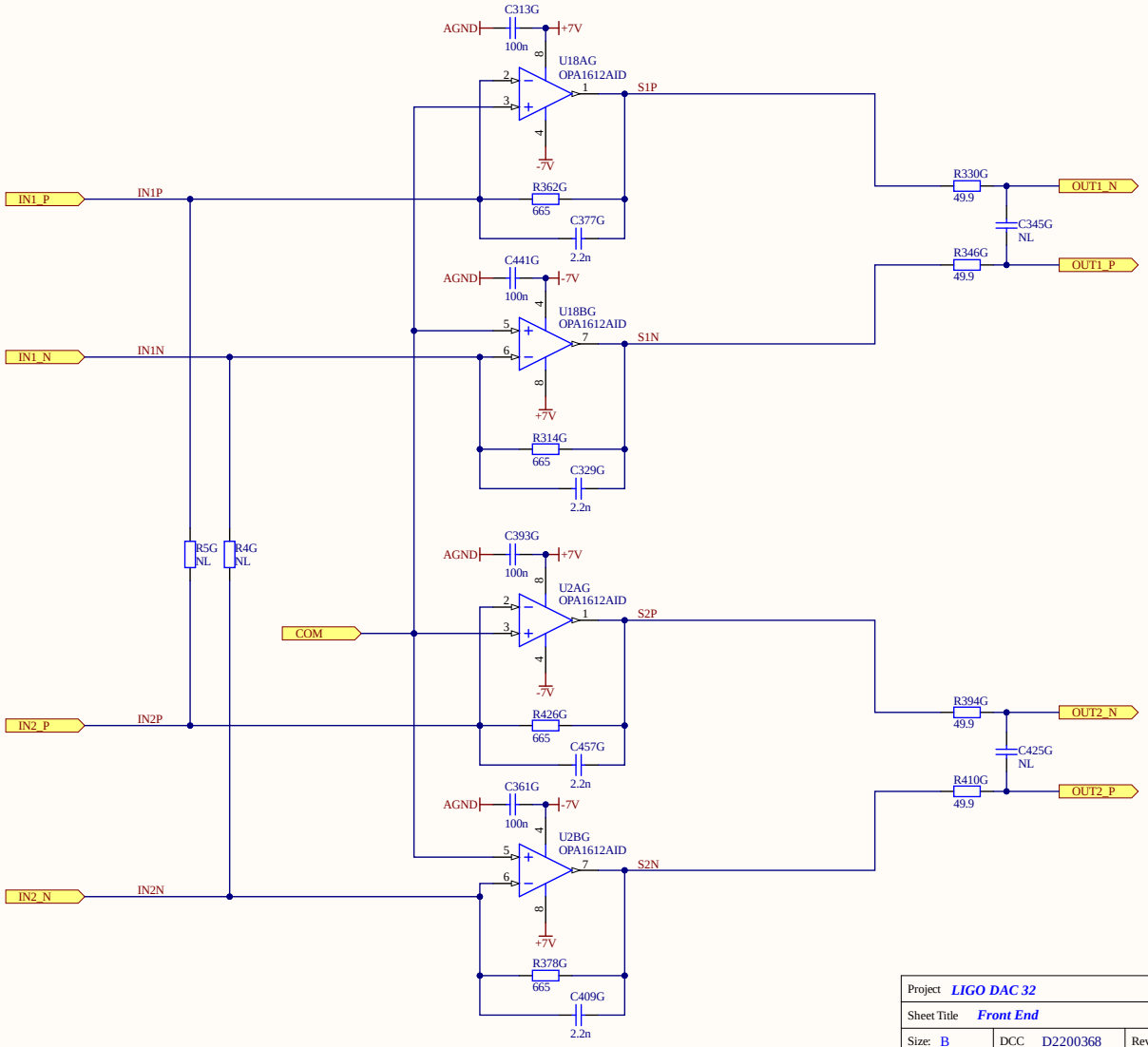
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:06 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

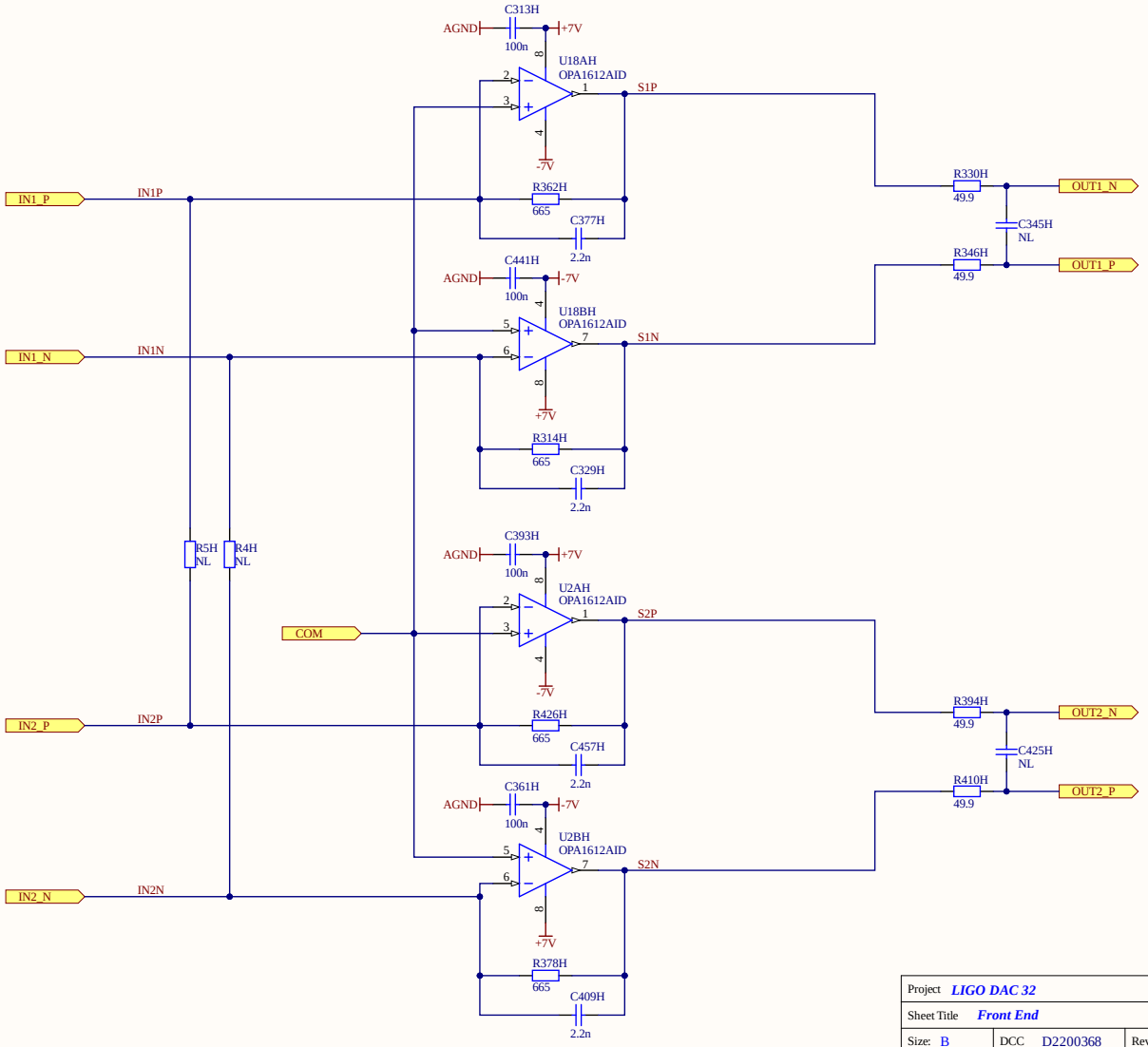
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:06 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

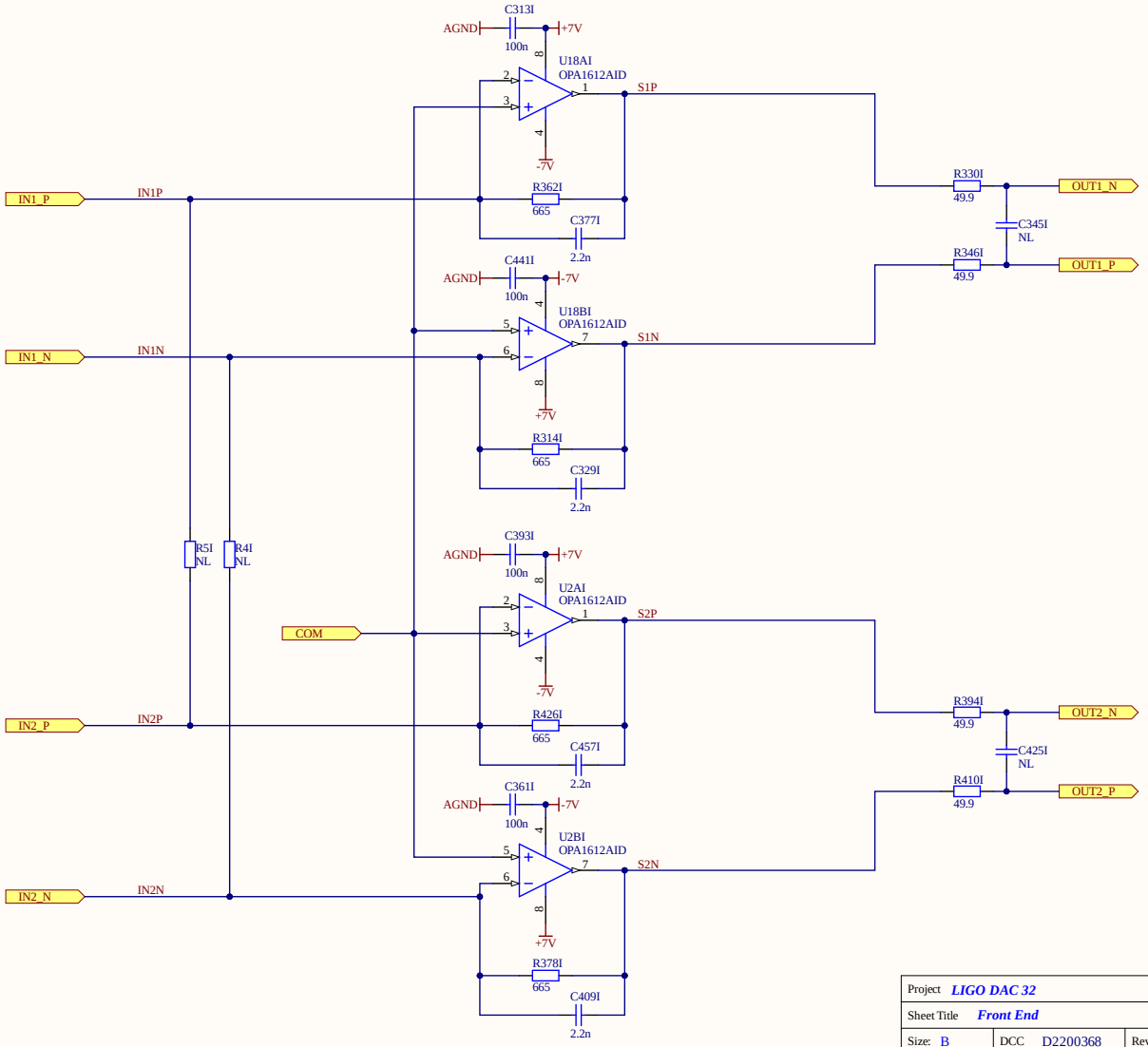
Front End Amplifiers



Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:06 PM	Sheet: 11 of 19		*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

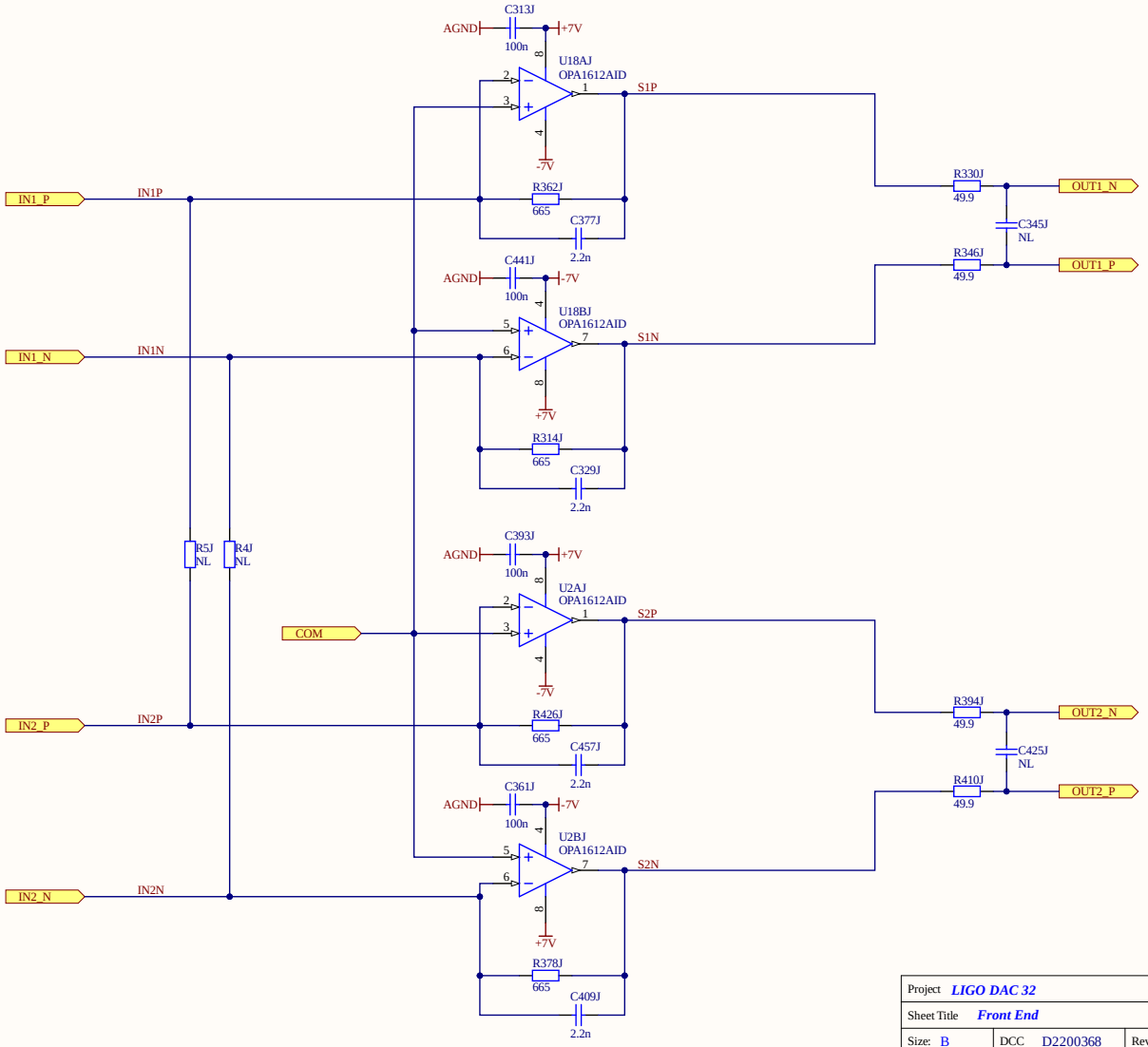
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:07 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

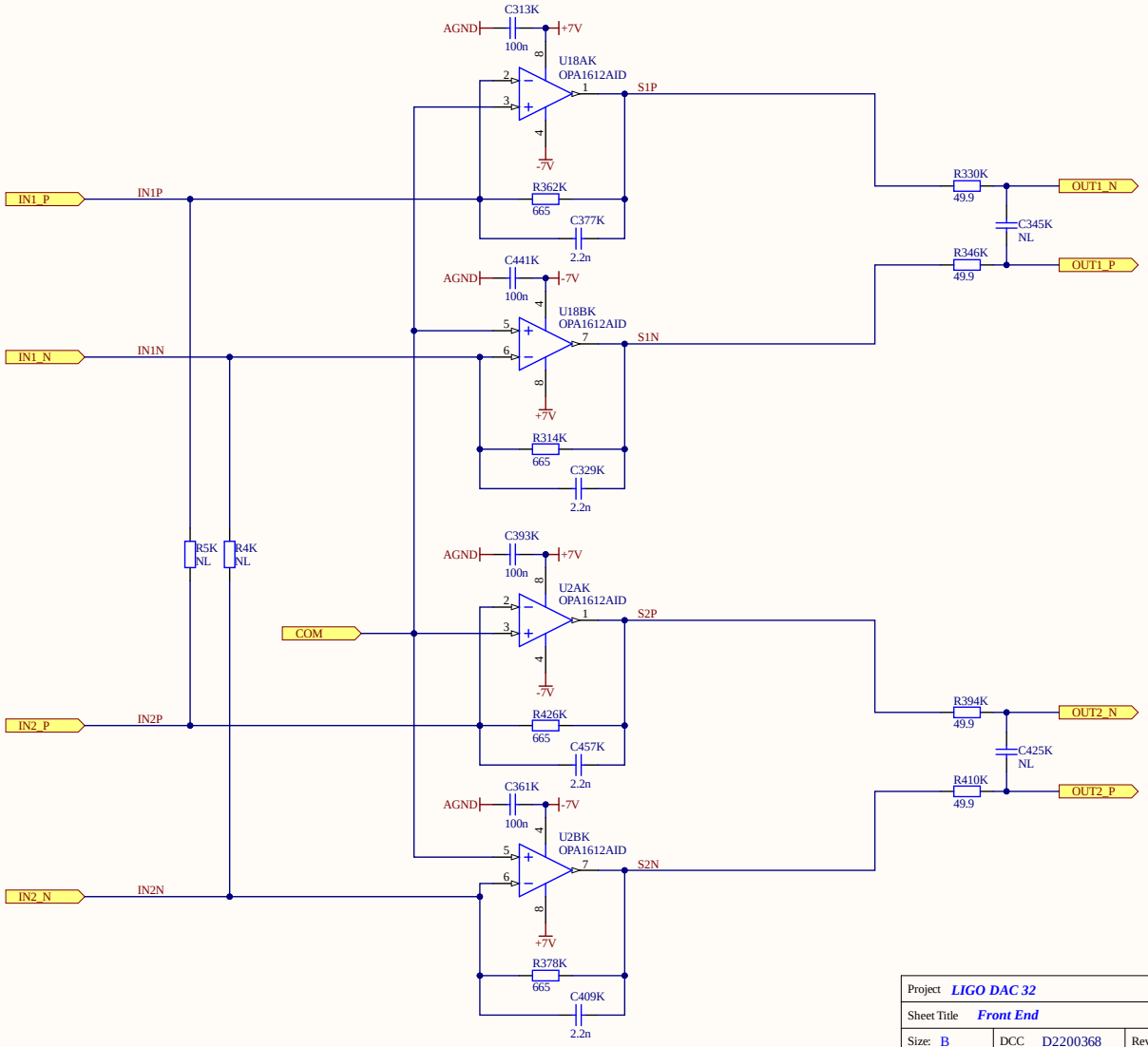
Front End Amplifiers



Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:07 PM	Sheet: 11 of 19		*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

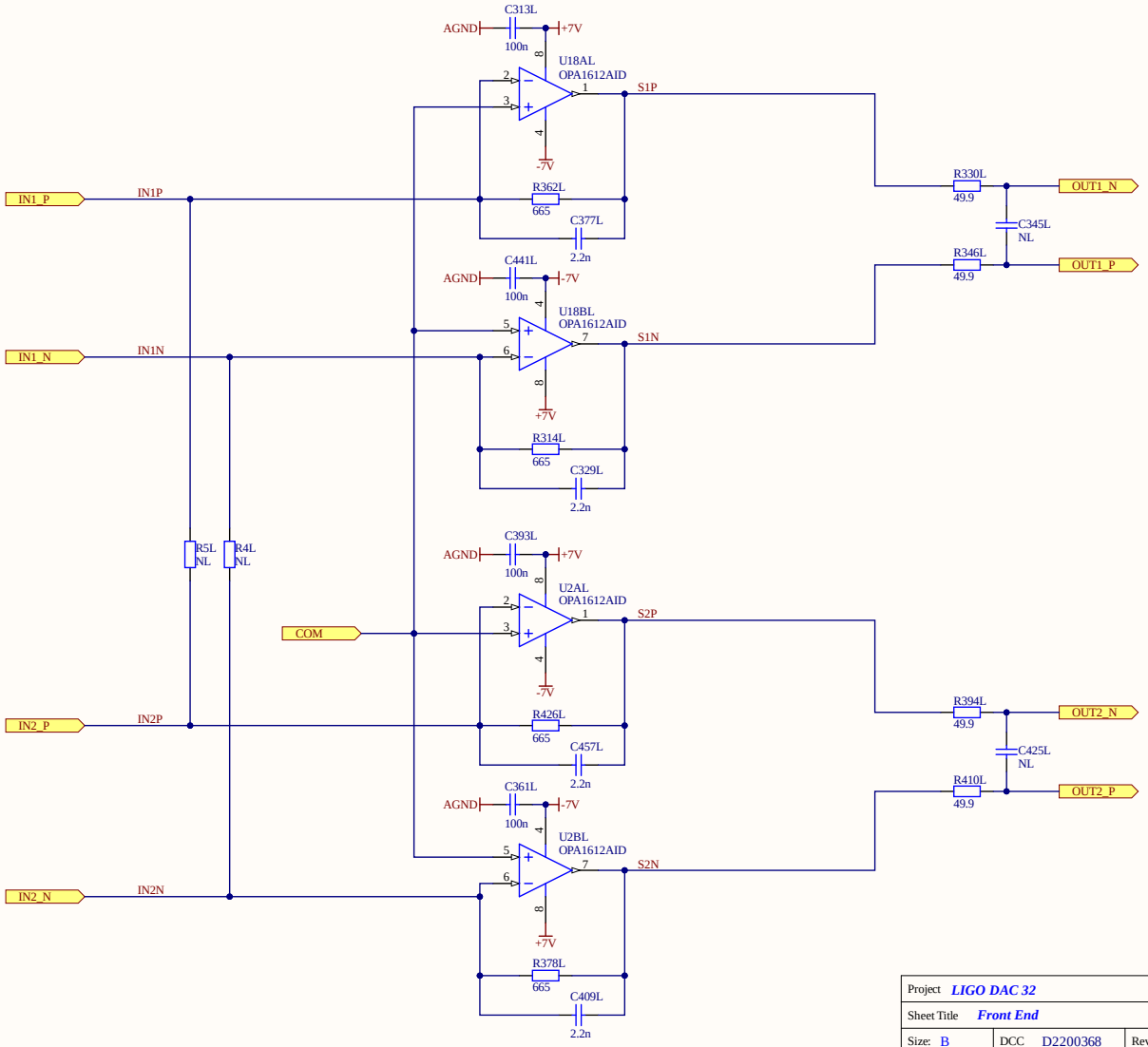
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:07 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

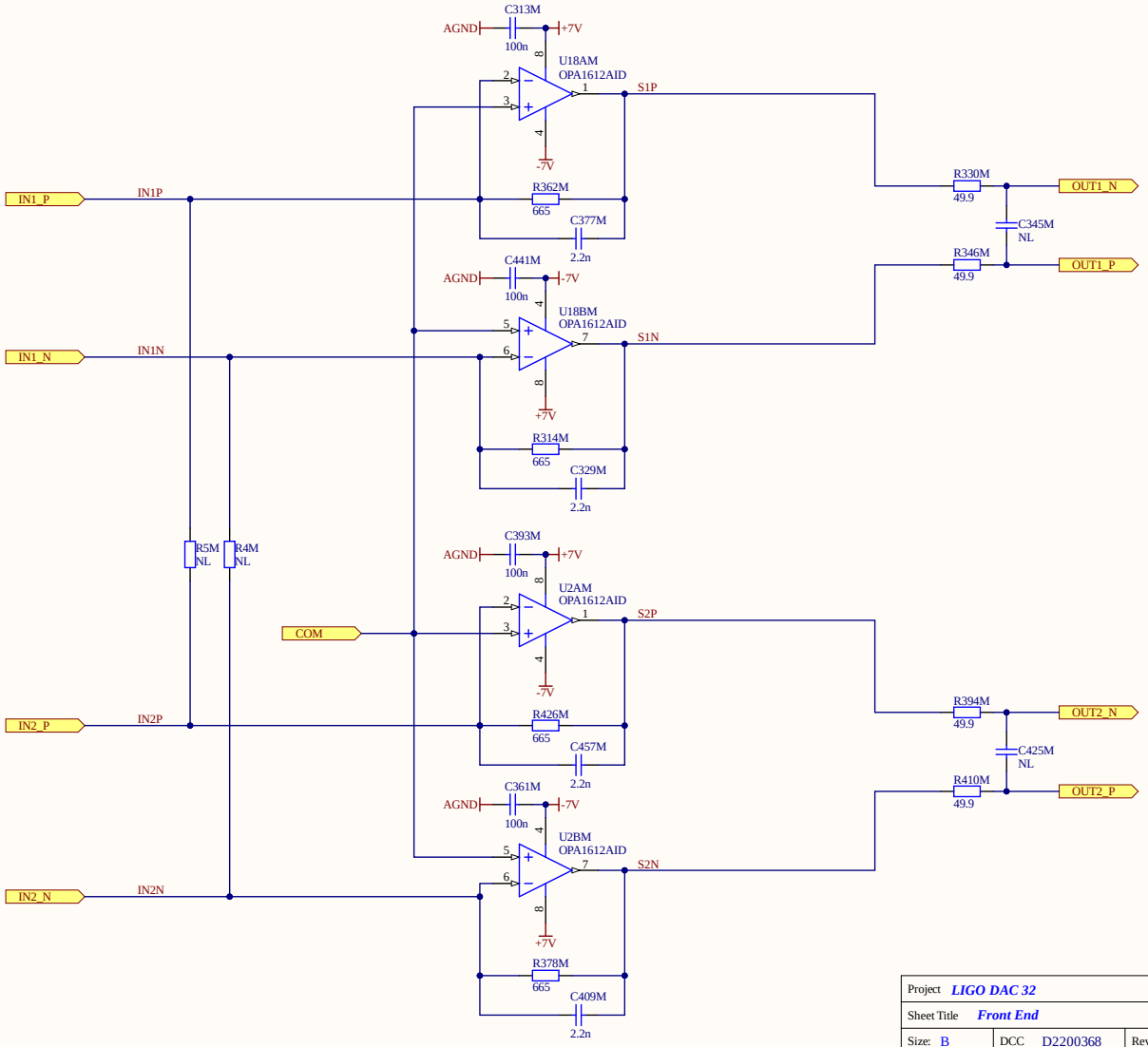
Front End Amplifiers



Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:08 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

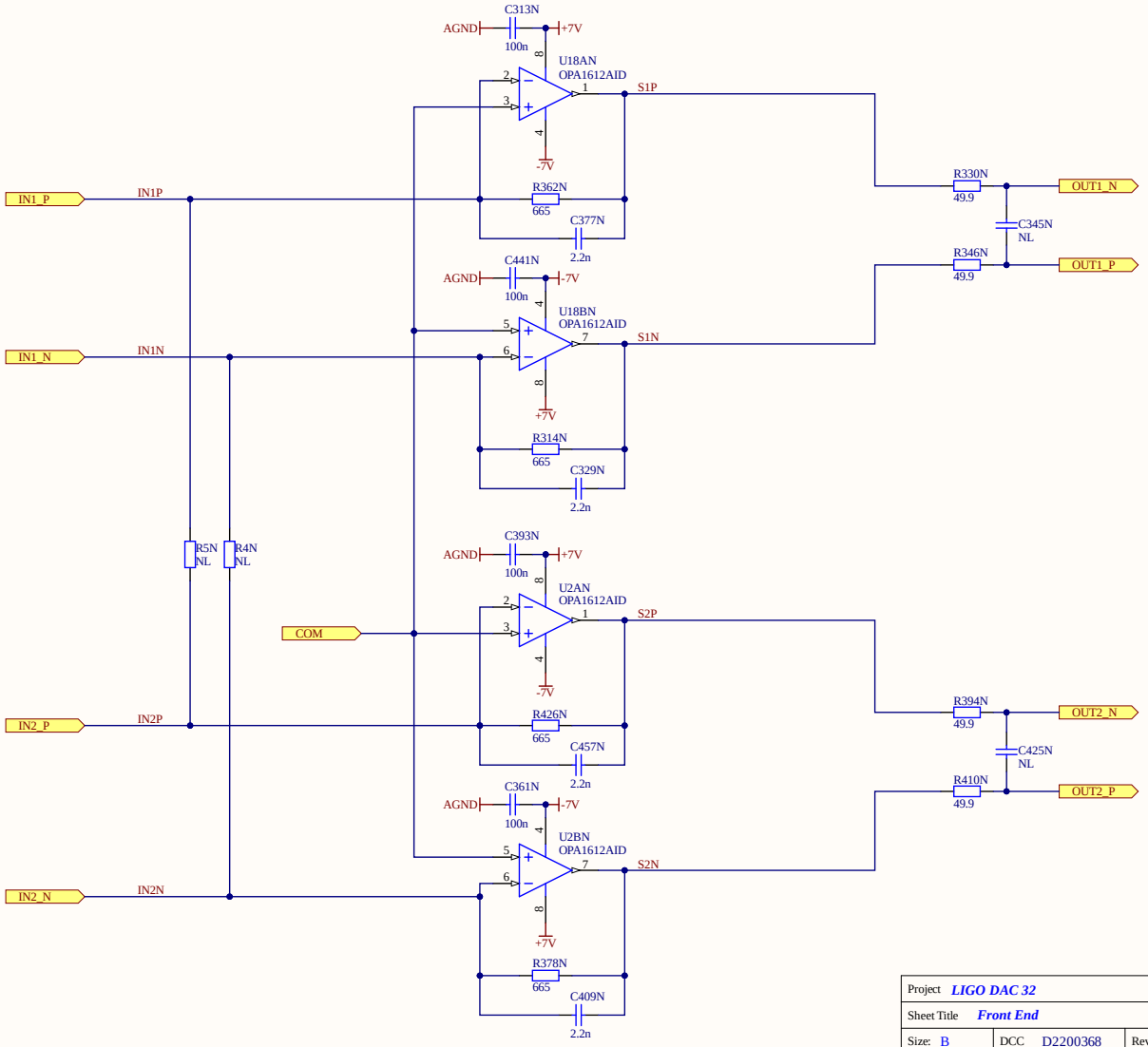
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:08 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

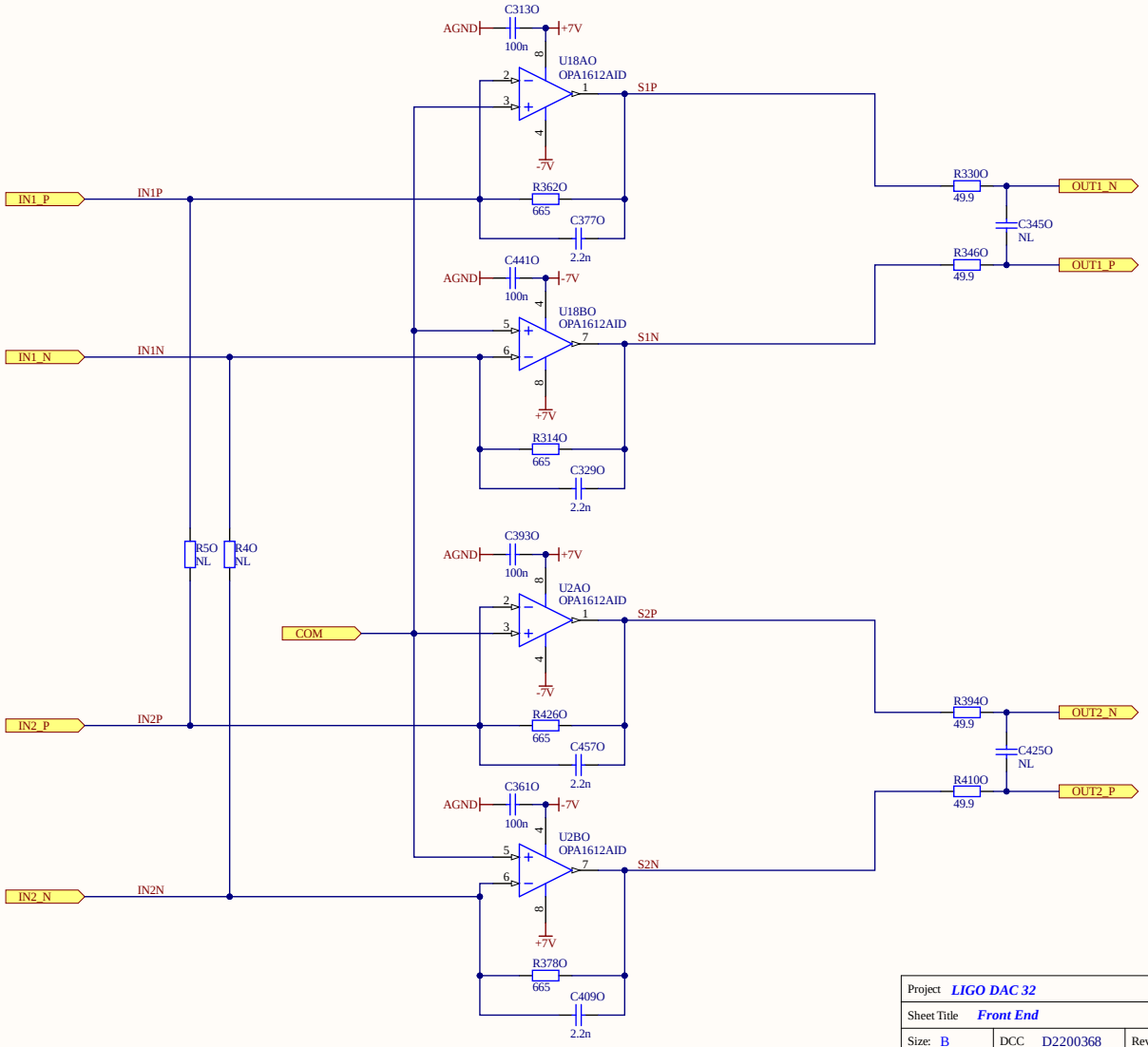
Front End Amplifiers



Parts Checked for Value and Consistency

Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *Front End*			
Size: B	DCC D2200368	Rev: 1	
Date: 11/10/2022 Time: 12:17:08 PM		Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

Front End Amplifiers



Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
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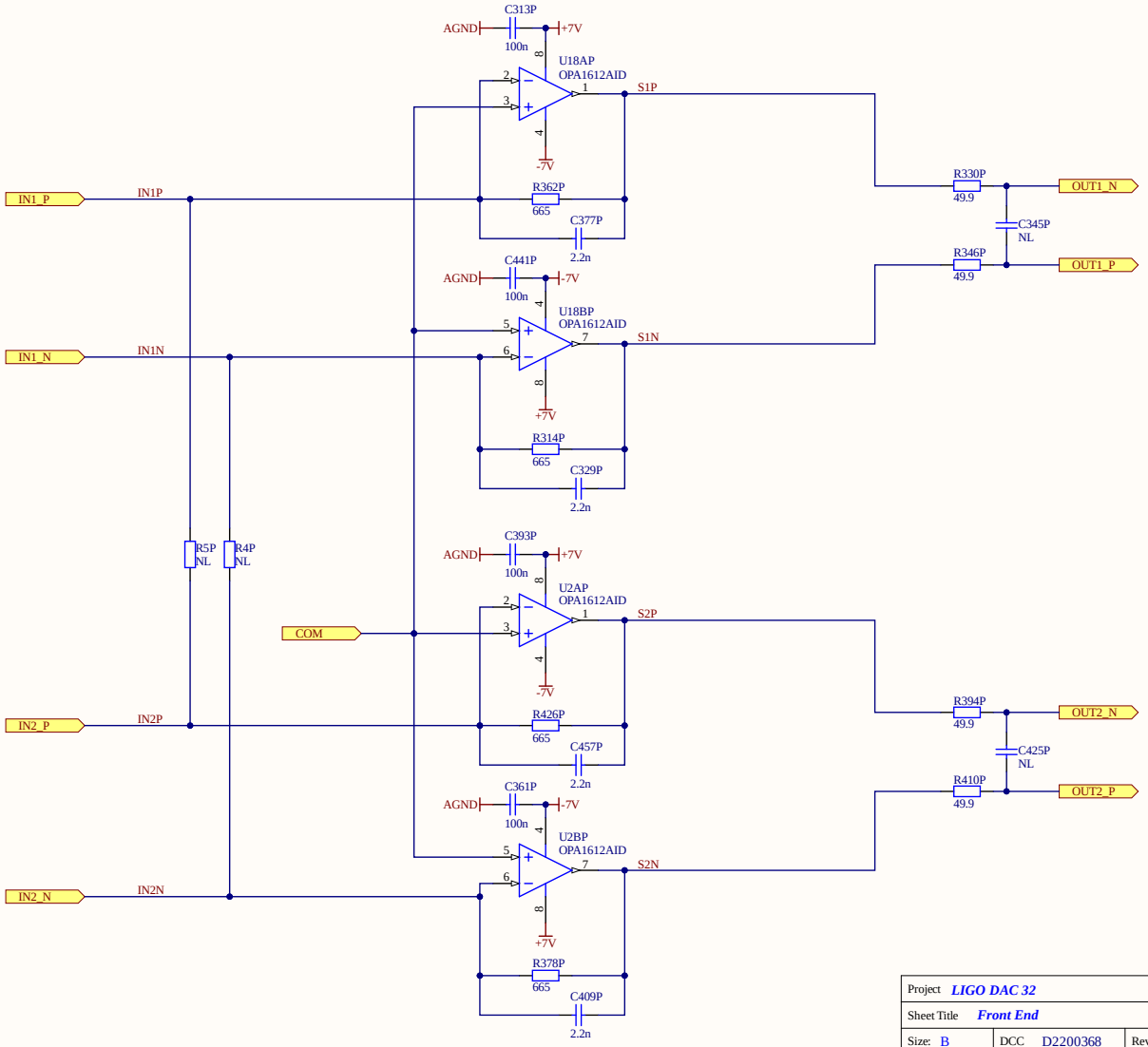
Date: 11/10/2022	Time: 12:17:09 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

Front End Amplifiers



Parts Checked for Value and Consistency

Project	*LIGO DAC 32*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Front End*		
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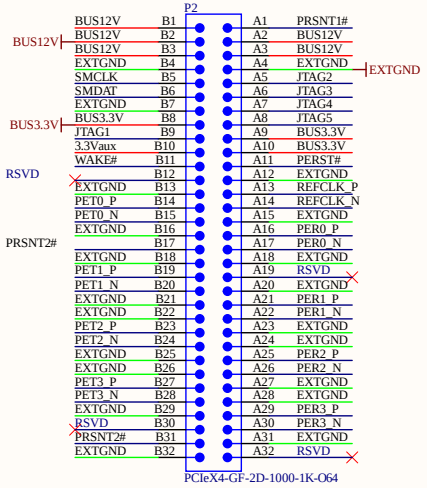
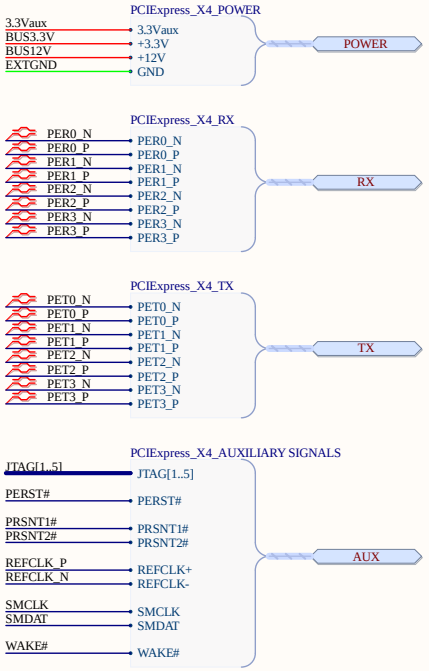
Date: 11/10/2022	Time: 12:17:09 PM	Sheet: 11 of 19	*DrawnBy: M. Pirello, D. Sigg*
File: LD32_FrontEnd.SchDoc			

PCIe 4x Slot





Project *LIGO DAC 32*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title *PCIe*			
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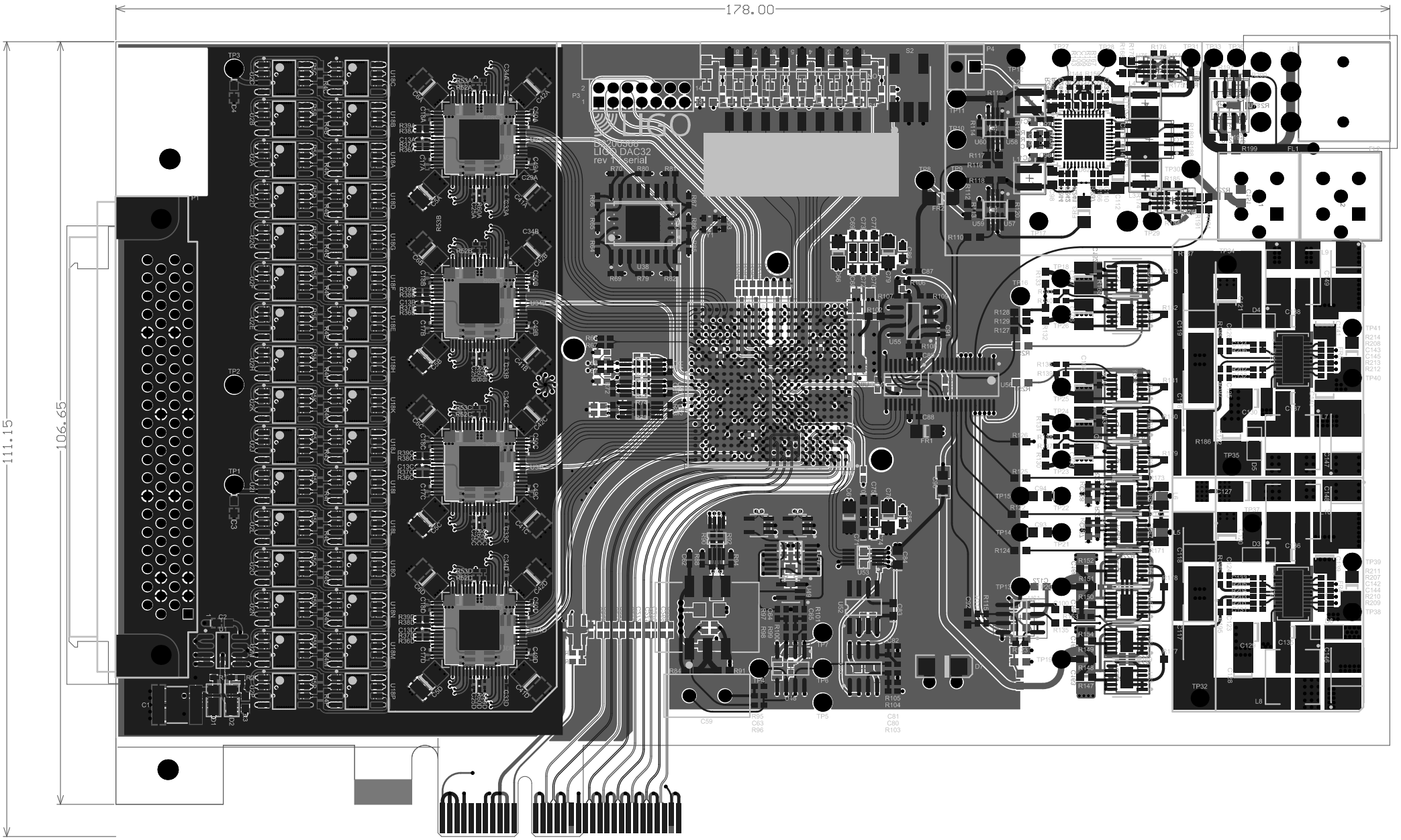
File: LD32_PCIE.SchDoc			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