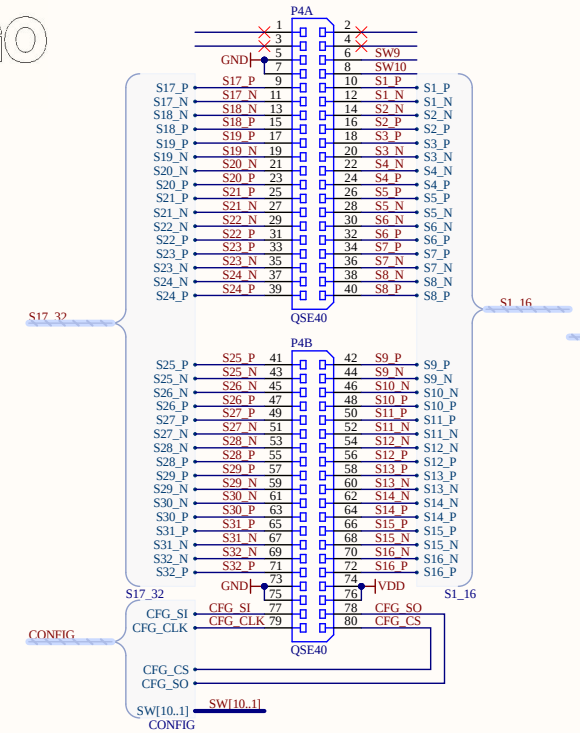
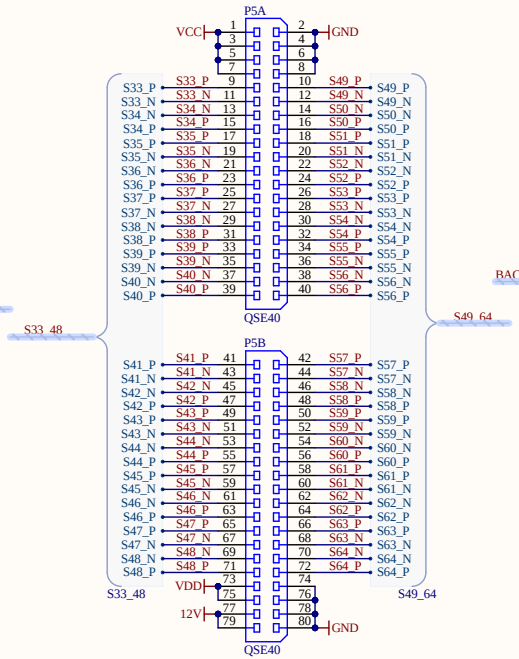
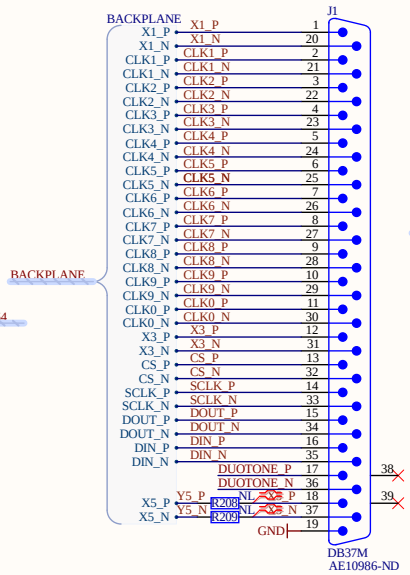
Samtec Expansion Port

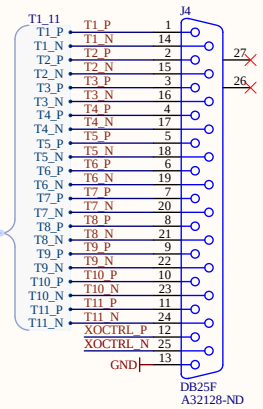


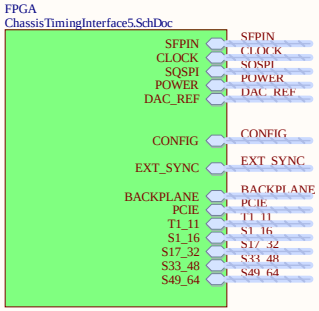


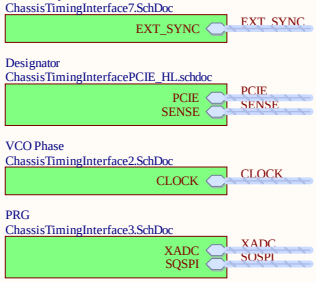
Duotone & Binary IO

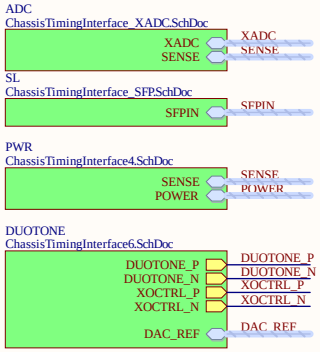


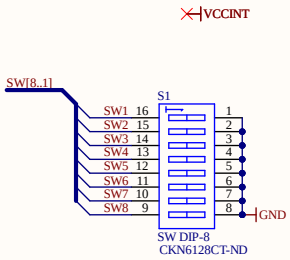
Rear DB25



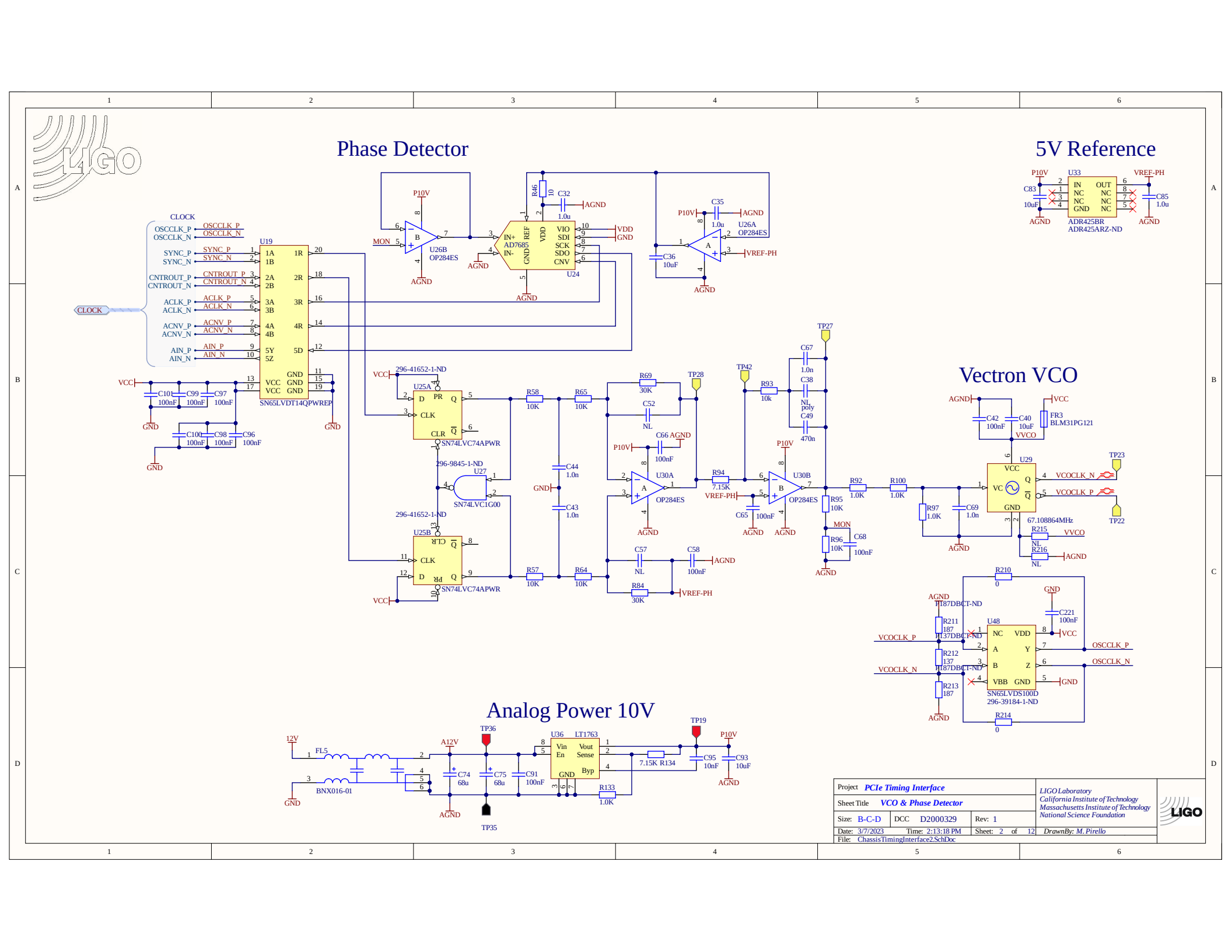




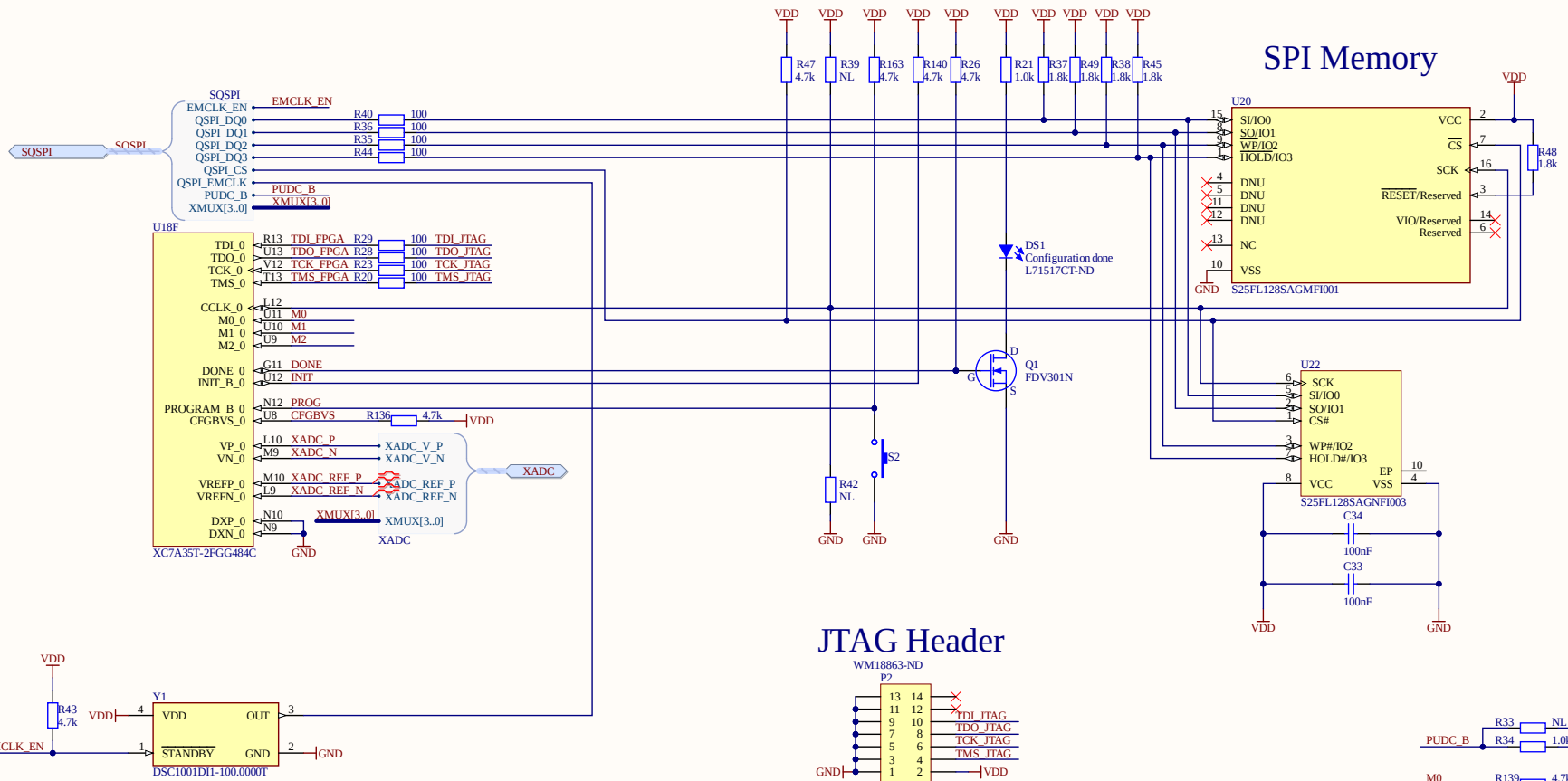




Project	*PCIe Timing Interface*		*LIGO Laboratory*
Sheet Title	*Timing Interface*		*California Institute of Technology*
Size: B-C-D	DCC D2000329	Rev: 1	*Massachusetts Institute of Technology*
Date: 3/7/2023	Time: 2:13:16 PM	Sheet: 1 of 12	*National Science Foundation*
File: ChassisTimingInterface1.SchDoc		*DrawnBy: M. Pirello*	

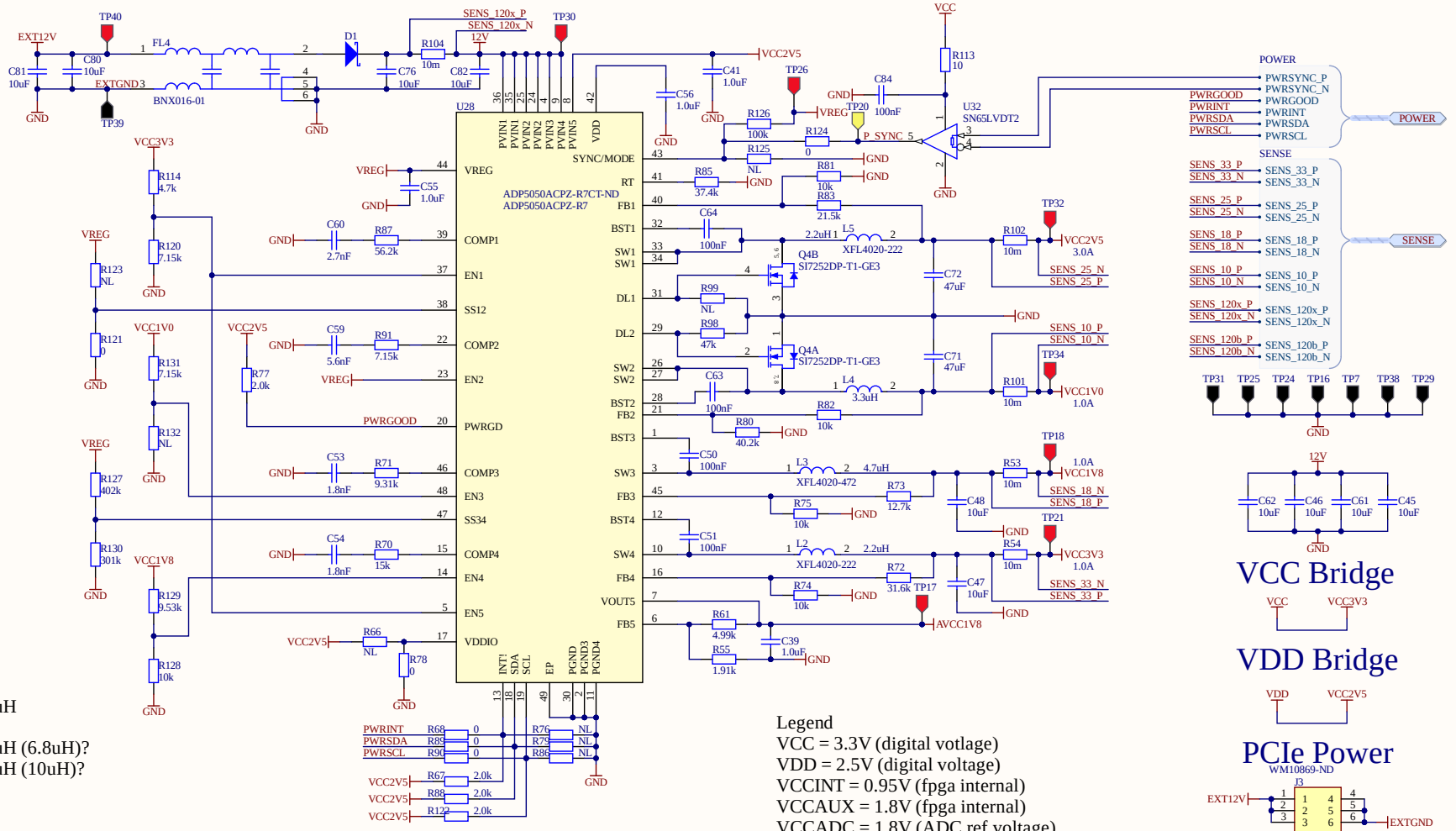

Phase Detector
5V Reference
Vectron VCO
Analog Power 10V
CLOCK
U19
SN65LVDT14QPWREP
U26B
OP284ES
U24
AD7685
U26A
OP284ES
U25A
U25B
SN74LVC74APWR
U27
SN74LVC1G00
U30A
U30B
OP284ES
U33
ADR425BR
ADR425ARZ-ND
U29
67.108864MHz
U48
SN65LVDS100D
296-39184-1-ND
U36
LT1763
FL5
BNX016-01
Project PCIe Timing Interface
Sheet Title VCO & Phase Detector
Size: B-C-D
DCC D2000329
Rev: 1
Date: 3/7/2023
Time: 2:13:18 PM
Sheet: 2 of 12
File: ChassisTimingInterface2.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello

JTAG and SPI Flash



Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*JTAG & SPI Flash*		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:19 PM	Sheet: 3 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface3.SchDoc			

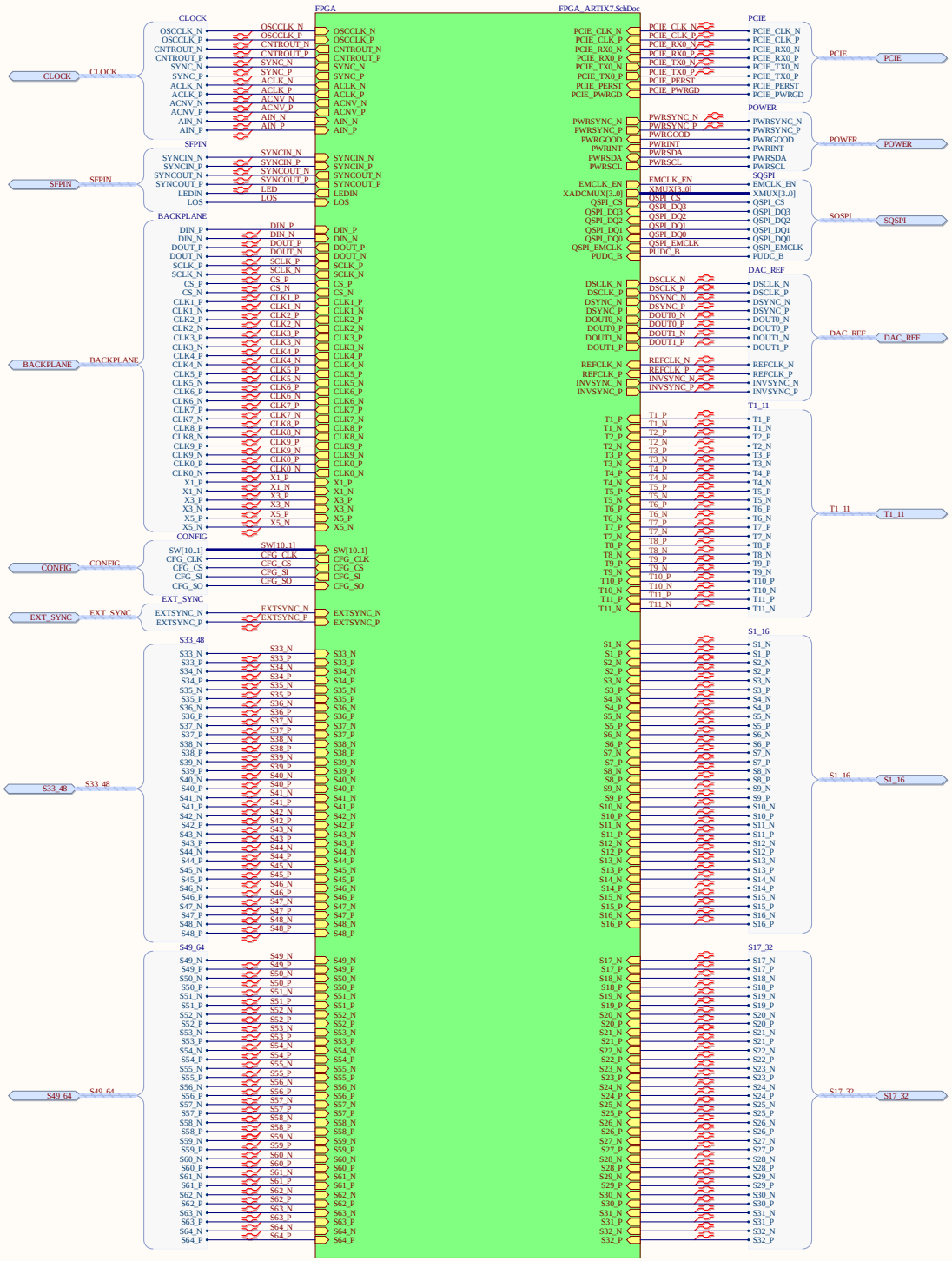
Switched FPGA Power

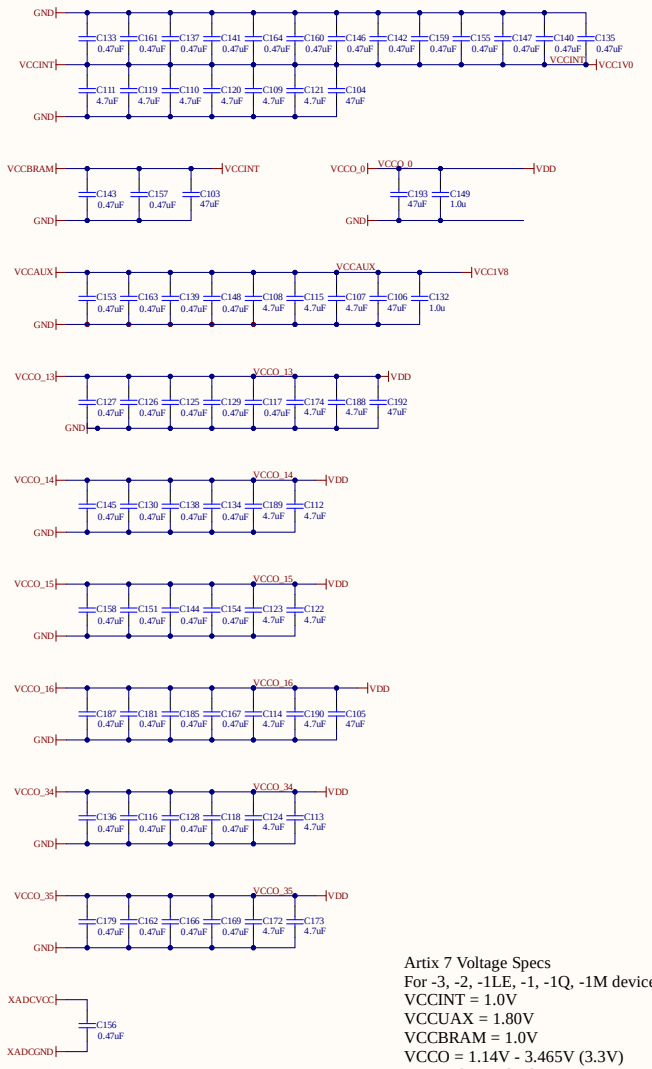


600kHz fsw?
RT Sync Calculation (R80)
FB1 - 2.5V 21.5k, 10.2k, 2.2uH
FB2 - 1.0V 10k. 40k, 3.3uH
FB3 - 1.8V 12.7k, 10.2k, 4.7uH (6.8uH)?
FB4 - 3.3V 31.6k, 10.2k, 2.2uH (10uH)?
FB5 - 1.8V 5k, 1.91k

Legend
VCC = 3.3V (digital votlage)
VDD = 2.5V (digital voltage)
VCCINT = 0.95V (fpga internal)
VCCAUX = 1.8V (fpga internal)
VCCADC = 1.8V (ADC ref voltage)
AVCC1V8

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Power Supply*		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:22 PM	Sheet: 4 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface4.SchDoc			

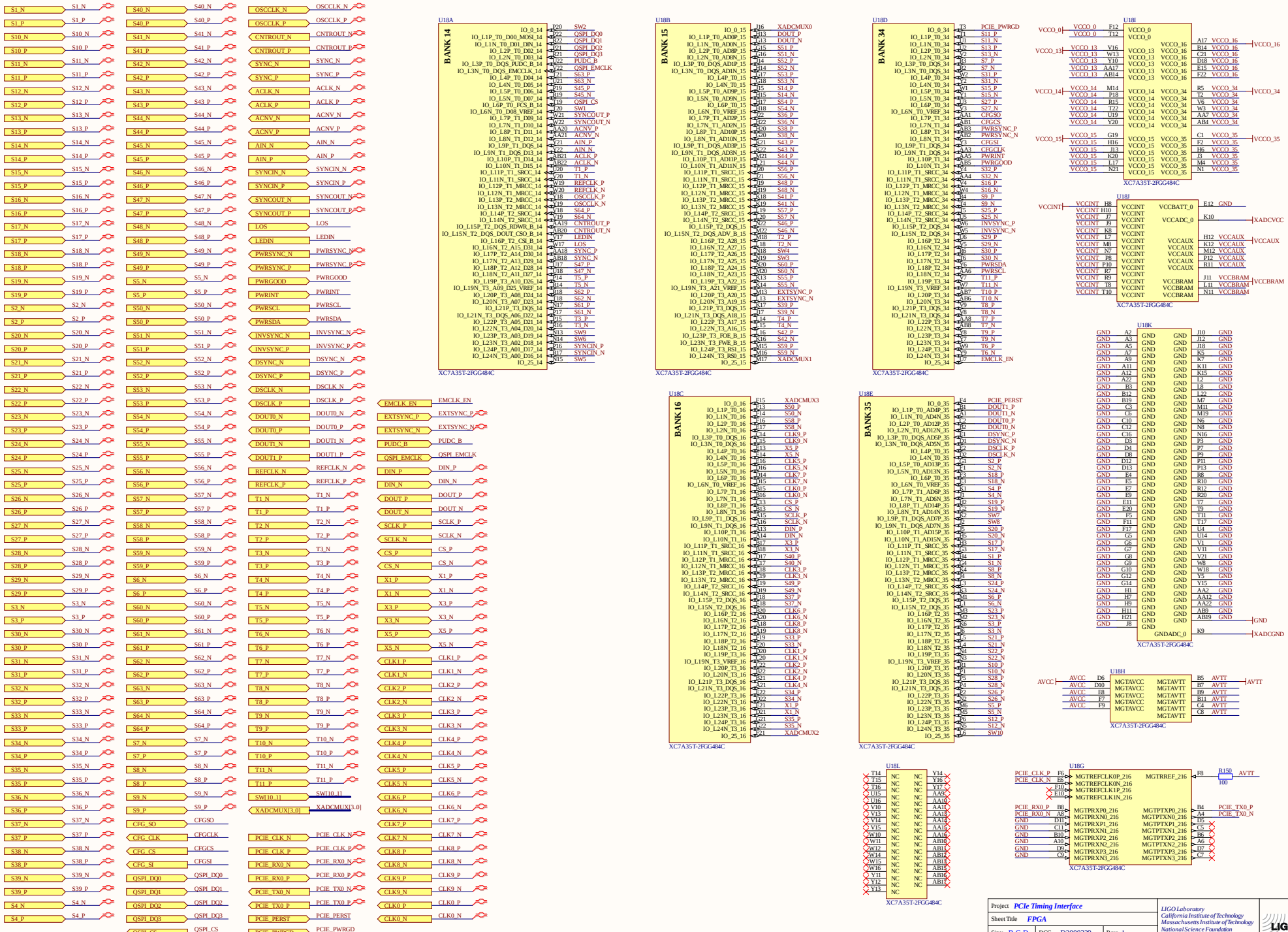




Artix 7 Voltage Specs
For -3, -2, -1LE, -1, -1Q, -1M devices
VCCINT = 1.0V
VCCUAX = 1.80V
VCCBRAM = 1.0V
VCCO = 1.14V - 3.465V (3.3V)
VIN = -0.2V - 3.465V
VCCBAT = 1.0V - 1.89V
VCCADC = 1.8V
VREFP = 1.25V
VREFN = 0V
VMGTAVCC = 1.0V
VMGTAVTT = 1.2V

LVDS DC Specification
VCCO = 2.5
VOH = 1.675V
VOL = 0.7V

Project	PCIe Timing Interface	LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology National Science Foundation	LIGO
Sheet Title	FPGA Interface		
Size: B-C-D	DCC: D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:25 PM	Sheet 5 of 12	DrawnBy: M.Pirello
File: ChassisTimingInterface5.SchDoc			

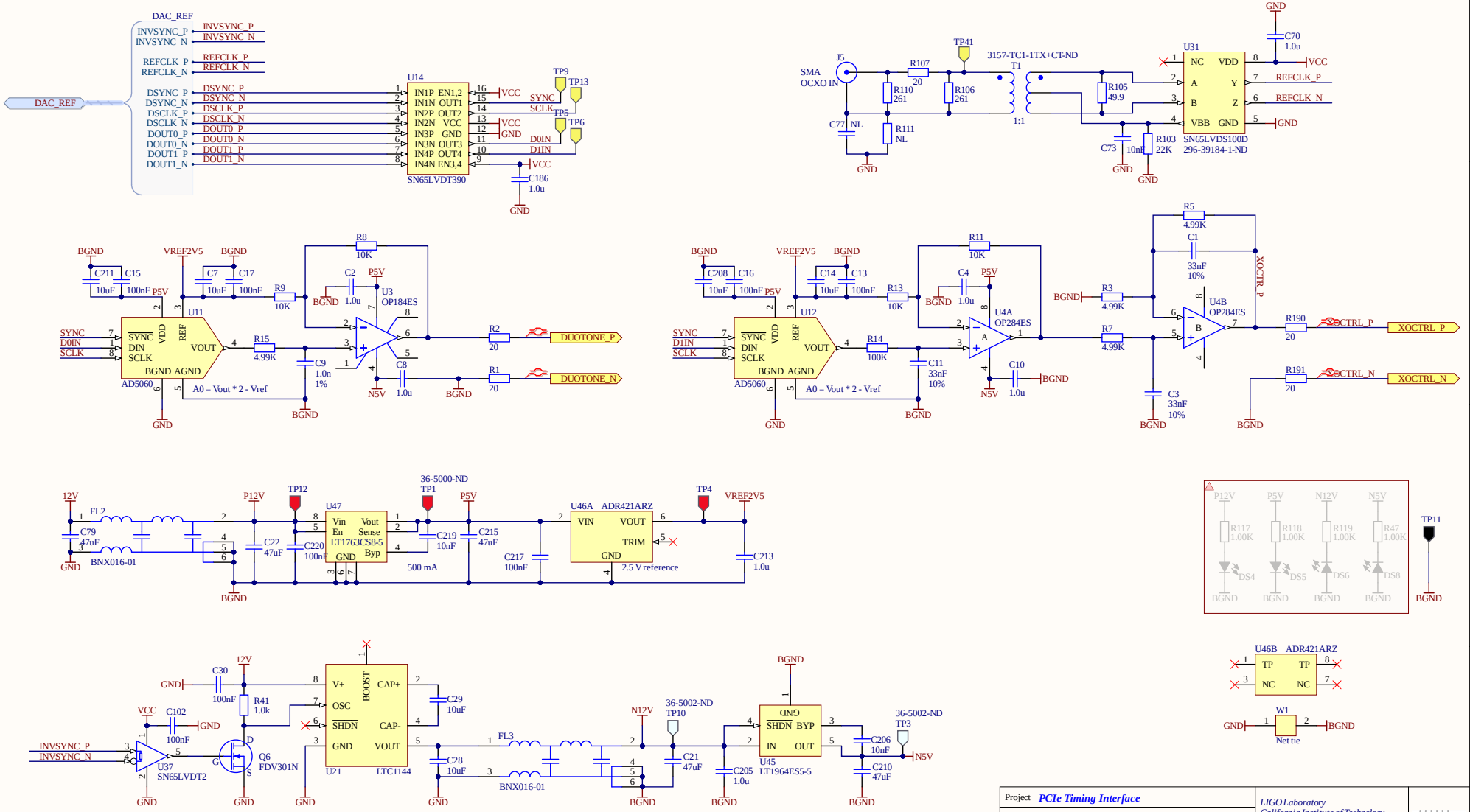


Project	PCIe Timing Interface
Sheet Title	FPGA
Size: B-C-D	DCC: D2000329 Rev: 1
Date: 3/7/2023	Time: 2:13:29 PM Sheet 6 of 12
File: FPGA_ARTIX7.SchDoc	

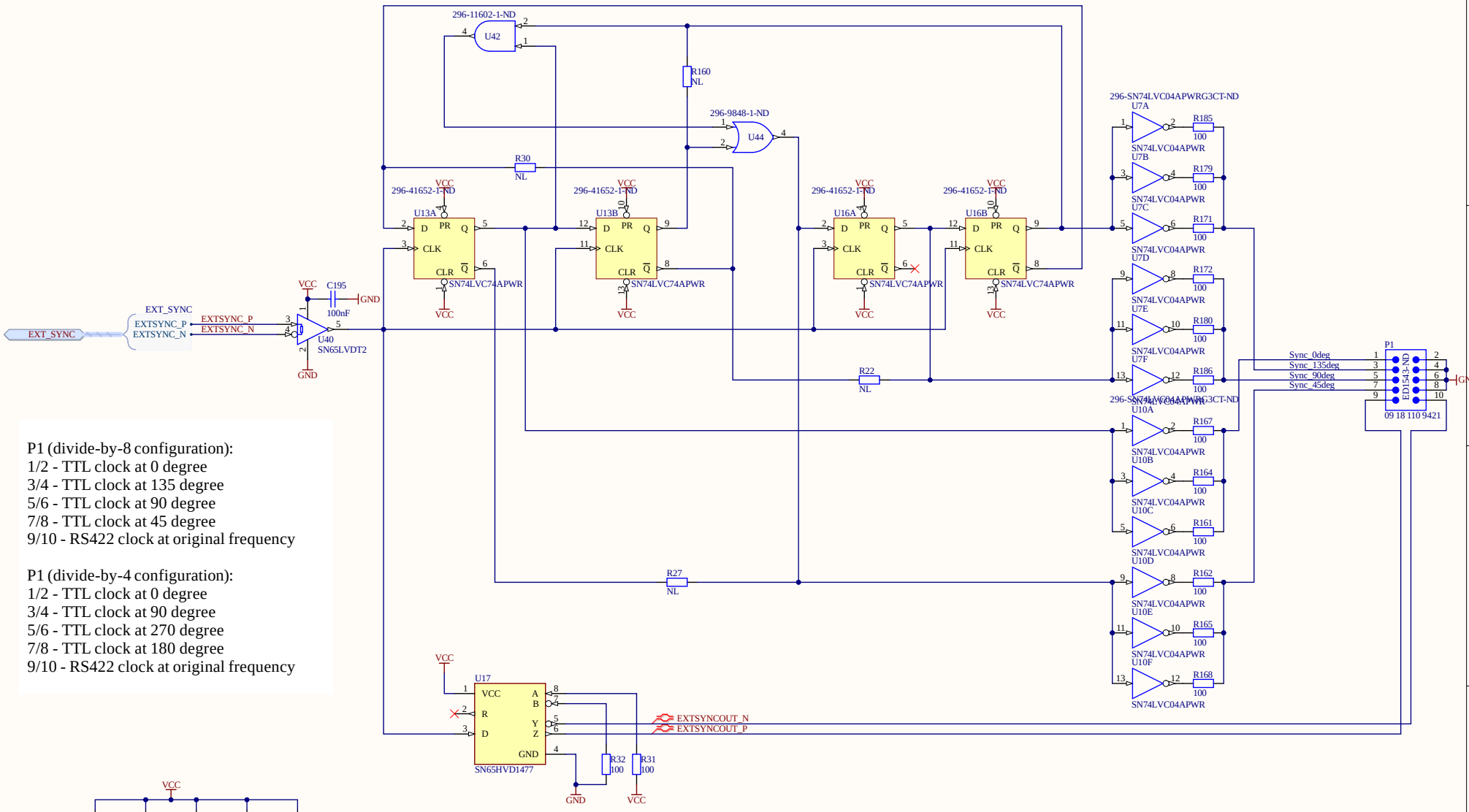
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation

LIGO

Drawn By: M. Pirello



Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*Duotone*		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:30 PM	Sheet: 7 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface6.SchDoc			

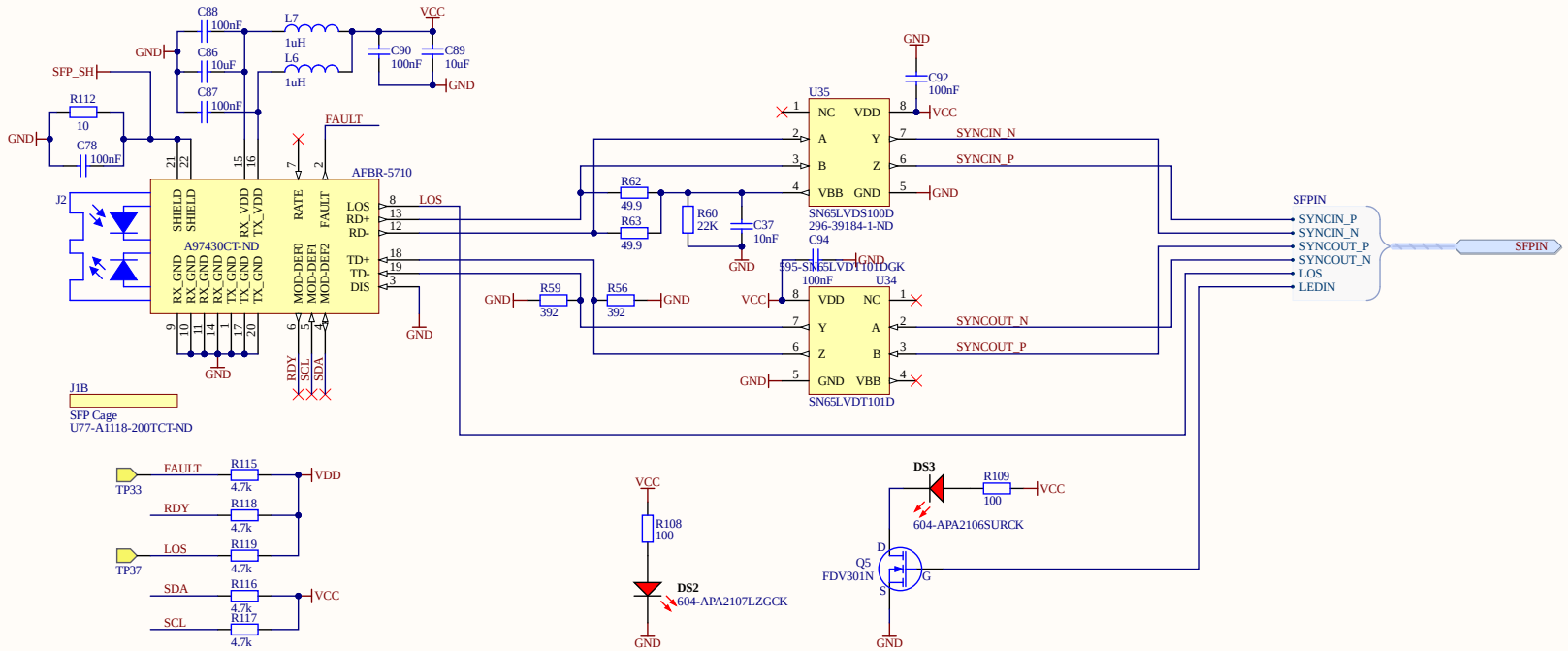


P1 (divide-by-8 configuration):
1/2 - TTL clock at 0 degree
3/4 - TTL clock at 135 degree
5/6 - TTL clock at 90 degree
7/8 - TTL clock at 45 degree
9/10 - RS422 clock at original frequency

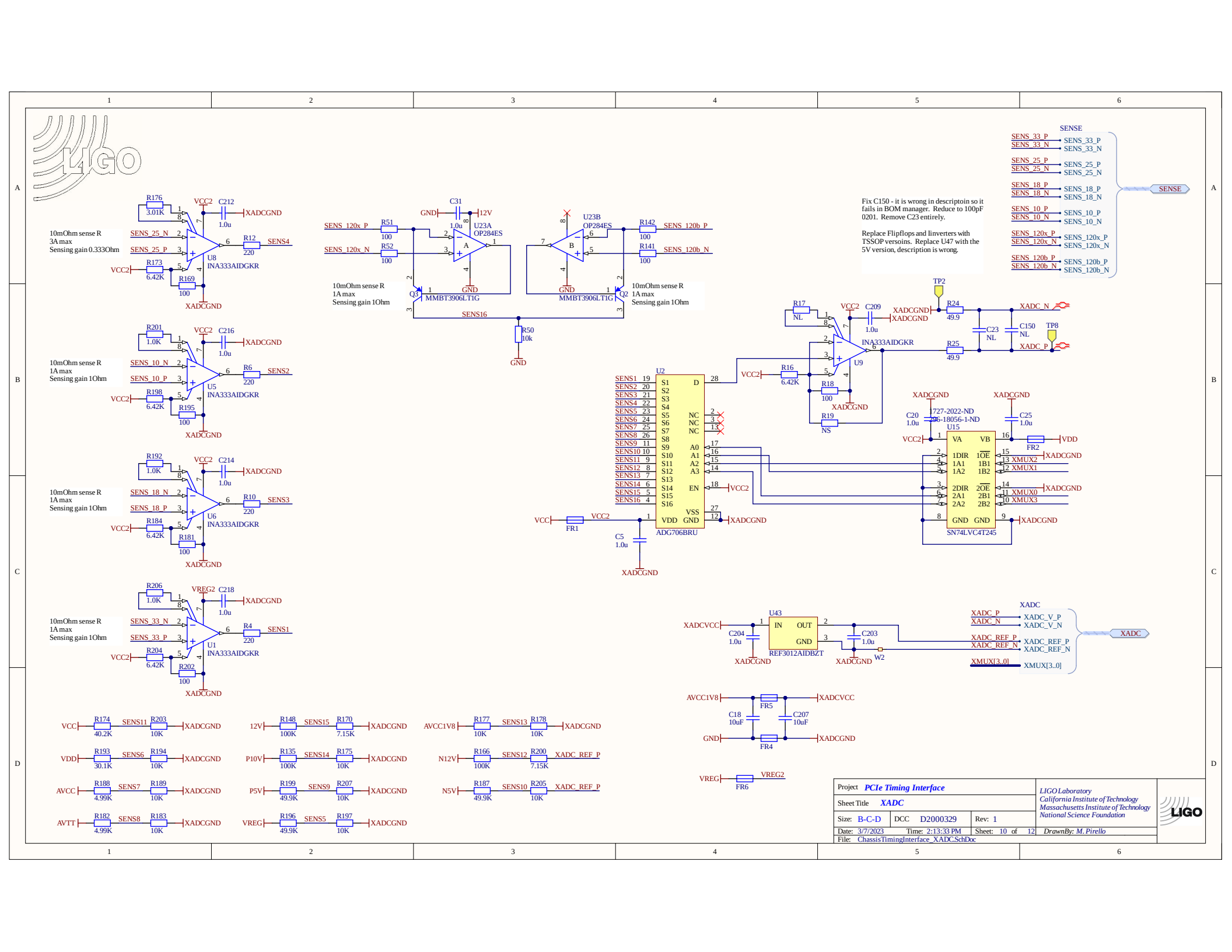
P1 (divide-by-4 configuration):
1/2 - TTL clock at 0 degree
3/4 - TTL clock at 90 degree
5/6 - TTL clock at 270 degree
7/8 - TTL clock at 180 degree
9/10 - RS422 clock at original frequency

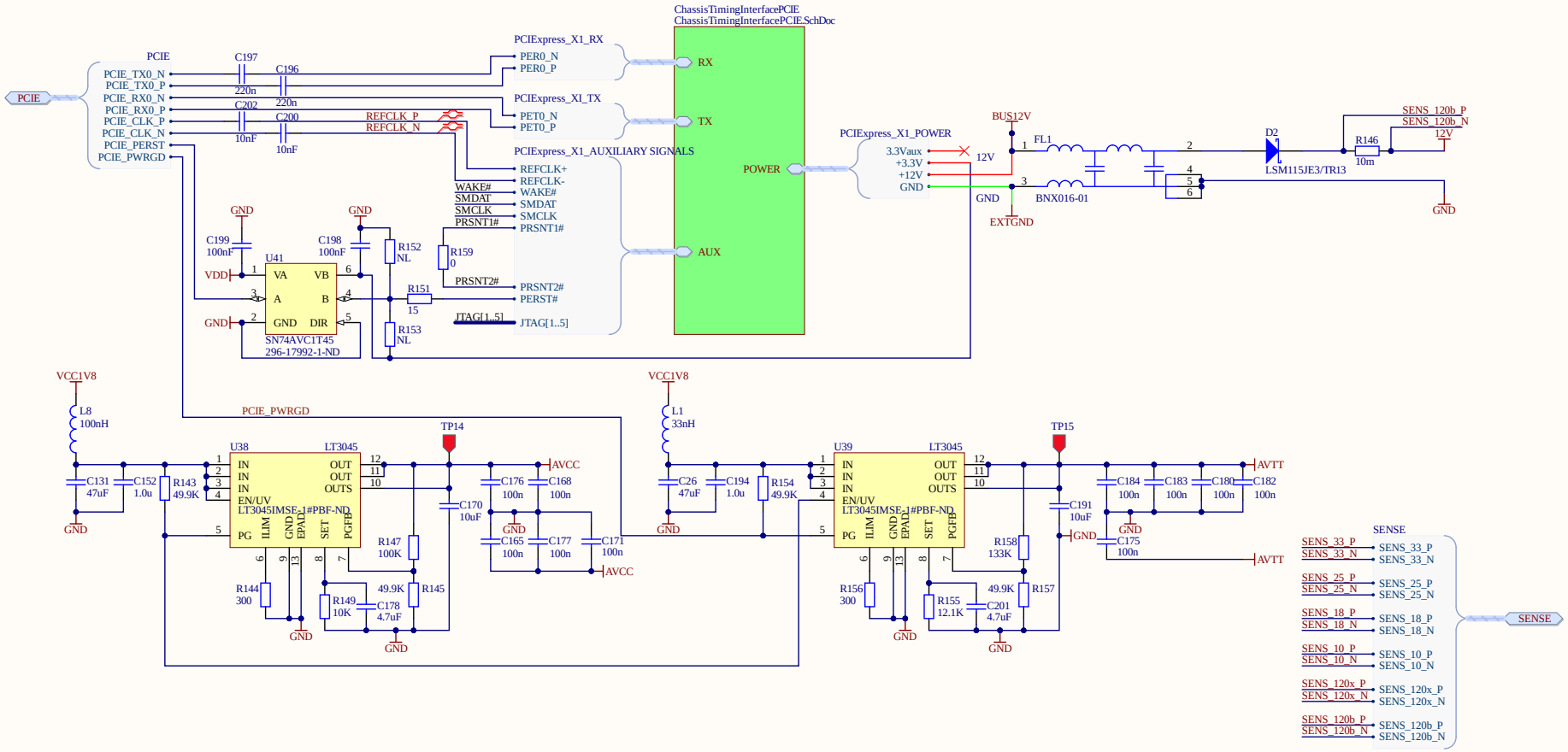
Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*External Sync*		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:31 PM	Sheet: 8 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface7.SchDoc			

SFP Port



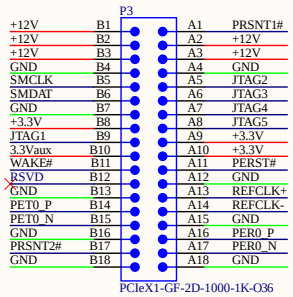
Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*SFP*		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023 Time: 2:13:32 PM		Sheet: 9 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterface_SFP.SchDoc			

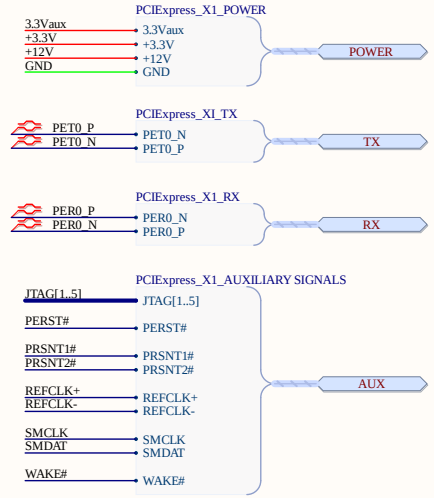

10mOhm sense R
3A max
Sensing gain 0.333Ohm
10mOhm sense R
1A max
Sensing gain 1Ohm
Fix C150 - it is wrong in descriptoin so it fails in BOM manager. Reduce to 100pF 0201. Remove C23 entirely.
Replace Flipflops and linverters with TSSOP versoins. Replace U47 with the 5V version, description is wrong.
INA333AIDGKR
OP284ES
MMBT3906LT1G
ADG706BRU
SN74LVC4T245
REF3012AIDBZT
SENSE
XADC
Project PCIe Timing Interface
Sheet Title XADC
Size: B-C-D
DCC D2000329
Rev: 1
Date: 3/7/2023
Time: 2:13:33 PM
Sheet: 10 of 12
File: ChassisTimingInterface_XADC.SchDoc
LIGO Laboratory
California Institute of Technology
Massachusetts Institute of Technology
National Science Foundation
DrawnBy: M. Pirello



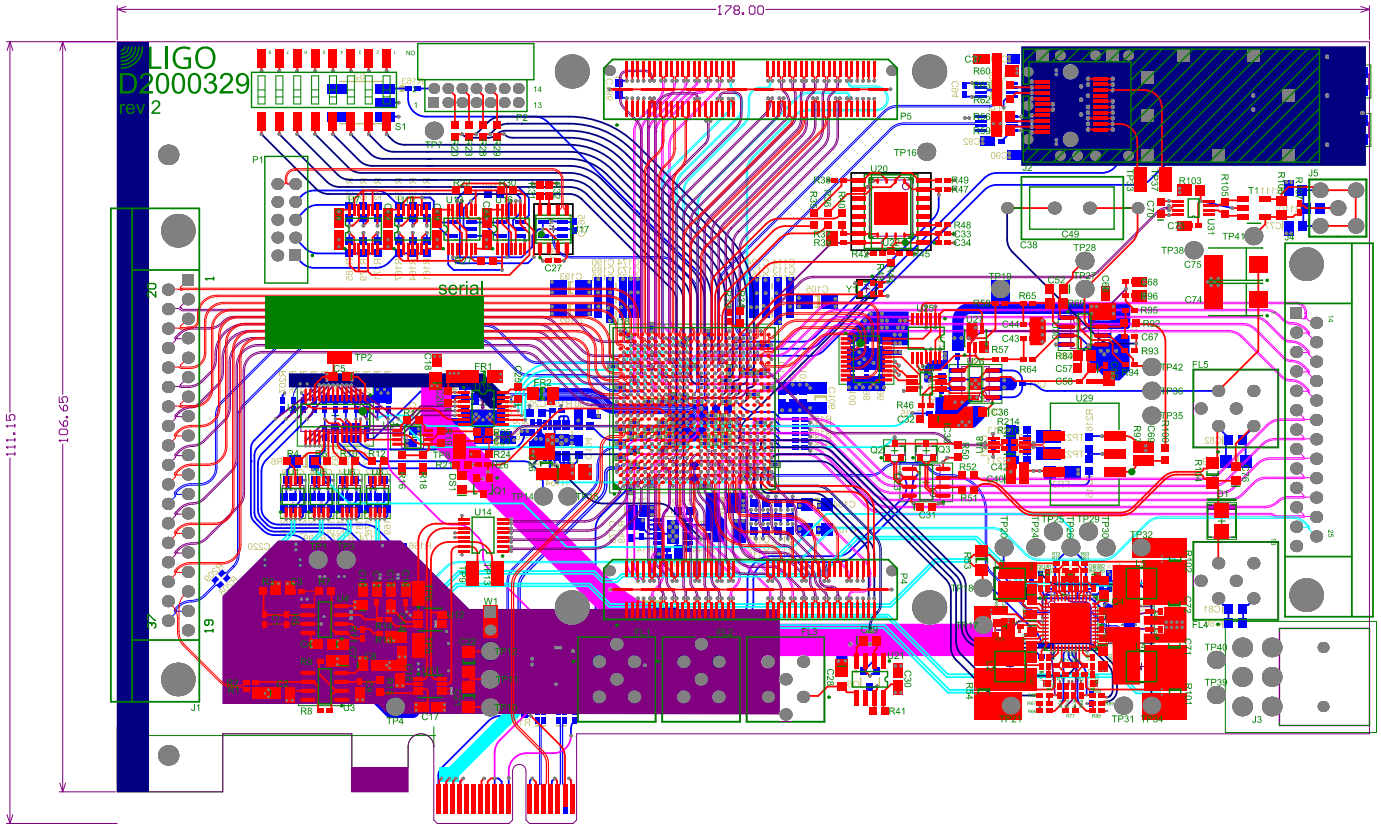
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.

Project	*PCIe Timing Interface*		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	*PCIe Interface*		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:34 PM	Sheet: 11 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterfacePCIE_HL.SchDoc			





Project	***PCIe Timing Interface***		*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology* *National Science Foundation*
Sheet Title	***PCIe***		
Size: B-C-D	DCC D2000329	Rev: 1	
Date: 3/7/2023	Time: 2:13:34 PM	Sheet: 12 of 12	*DrawnBy: M. Pirello*
File: ChassisTimingInterfacePCIE.SchDoc			



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	1.00mil	4
	Top Surface Finish	PbSn	0.79mil	
1	Top Layer	CF-004	1.38mil	
	Dielectric 1	PP-006	3.00mil	3.87
	Dielectric 2	PP-006	3.00mil	3.87
2	Int1 (GND)	CF-004	0.69mil	
	Dielectric 3	Core-016	5.00mil	4.1
3	Int2 (Sign)	CF-004	0.69mil	
	Dielectric 4	PP-006	3.50mil	4.1
	Dielectric 5	PP-006	3.50mil	4.1
4	Int3 (Sign)	CF-004	0.69mil	
	Dielectric 6	Core-016	4.00mil	4.1
5	Int4 (PWR)	CF-004	0.69mil	
	Dielectric 7	PP-006	2.85mil	3.87
	Dielectric 8	PP-006	2.85mil	3.87
6	Int5 (GND)	CF-004	0.69mil	
	Dielectric 9	Core-016	4.00mil	4.1
7	Int6 (Sign)	CF-004	0.69mil	
	Dielectric 10	PP-006	3.50mil	4.1
	Dielectric 11	PP-006	3.50mil	4.1
8	Int7 (Sign)	CF-004	0.69mil	
	Dielectric 12	Core-016	5.00mil	4.1
9	Int8 (GND)	CF-004	0.69mil	
	Dielectric 13	PP-006	3.00mil	3.87
	Dielectric 14	PP-006	3.00mil	3.87
10	Bottom Layer	CF-004	1.38mil	
	Bottom Surface Finish	PbSn	0.79mil	
	Bottom Solder	SM-001	1.00mil	4
	Bottom Overlay			
Total board thickness:			61.54mil	