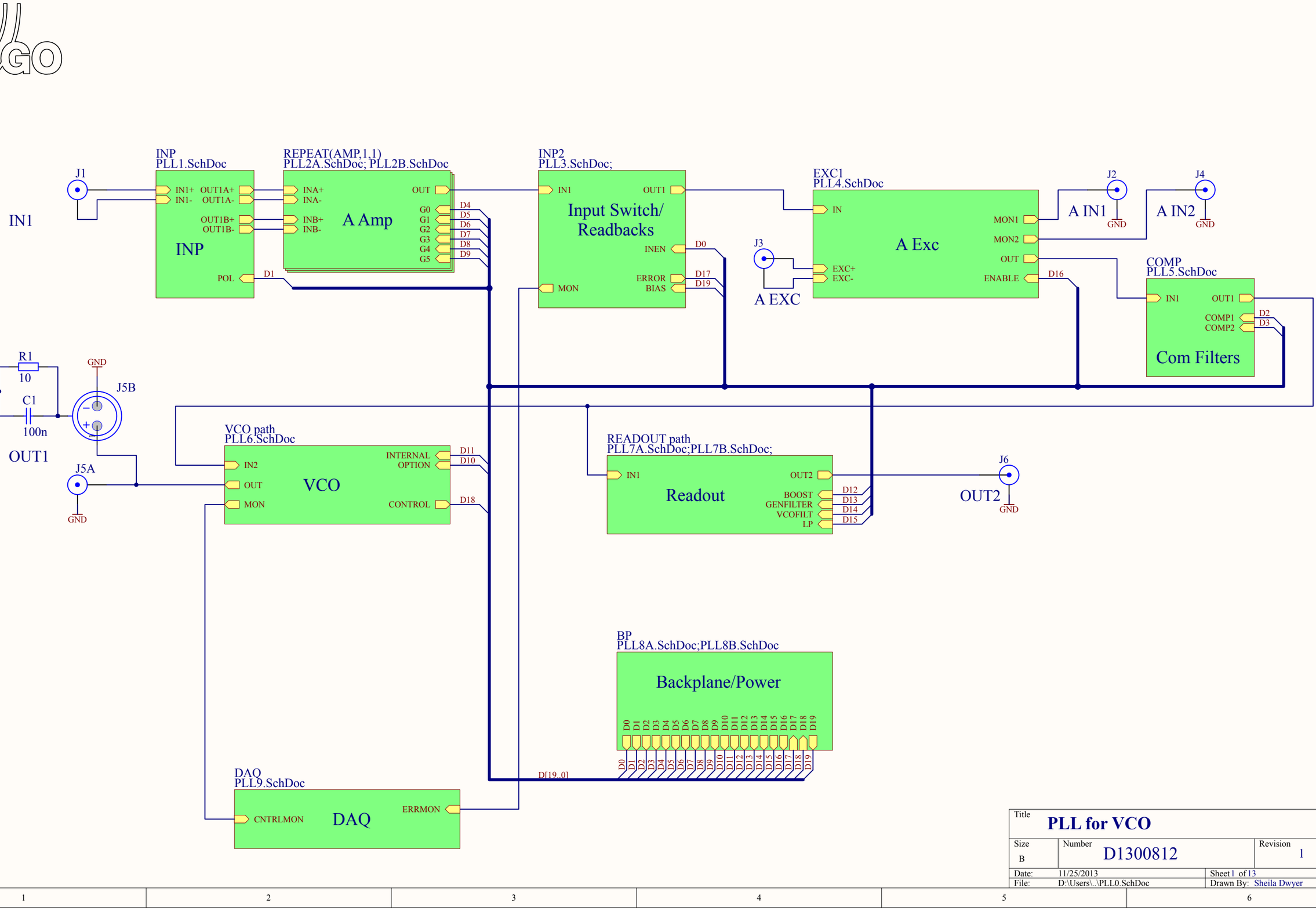
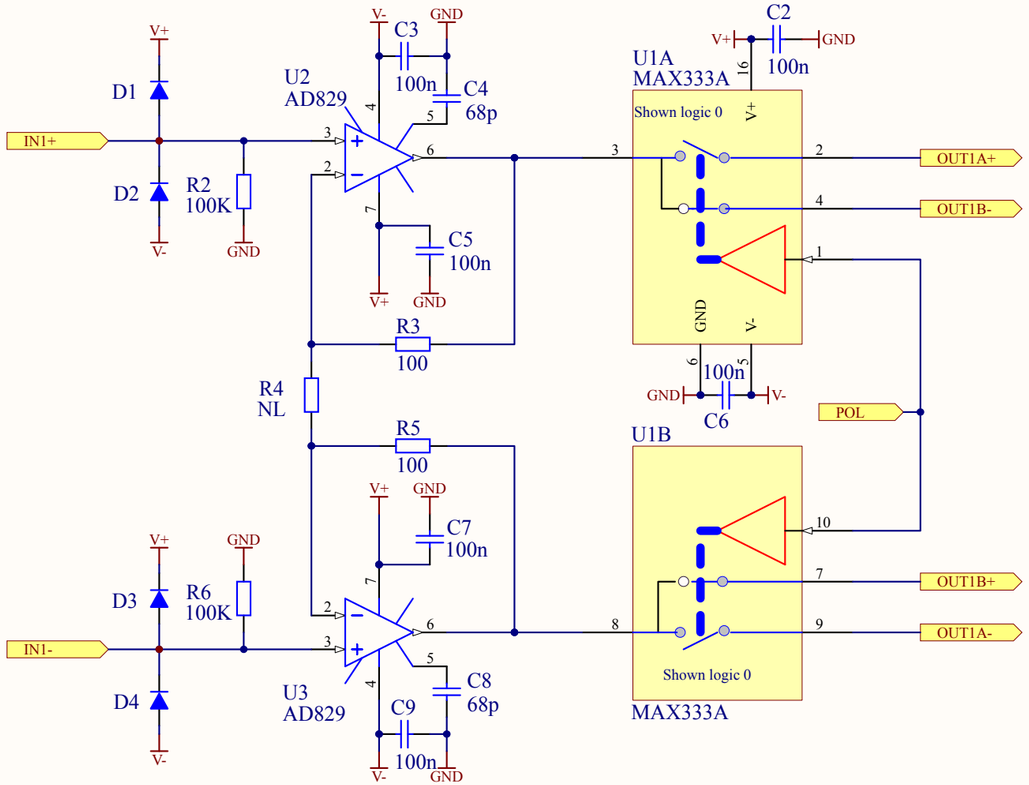
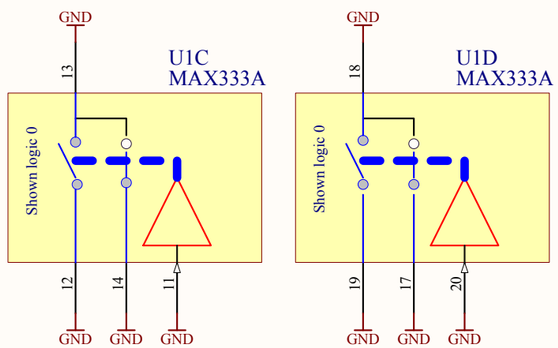


Title	**PLL for VCO**	
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet 1 of 13
File: D:\Users\..\PLL0.SchDoc		Drawn By: Sheila Dwyer

For small input signals add gain to these instrumnentation amplifier stages.





Title	**PLL Board: Input**		
Size: B	Number: D1300812		Revision: 1
Date: 11/25/2013		Sheet 2 of 13	
File: D:\Users\..\PLL1.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg	

Gain must be 0dB or greater for best noise performance

-8dB

-16dB

-8dB

dB	G5G4G3	1Y2Y3Y4Y
-32	0 1 1	1 1 1 1
-24	0 1 0	1 0 1 1
-16	0 0 1	0 1 1 1
-8	0 0 0	0 0 1 1
0	1 1 1	0 0 1 1
8	1 1 0	0 0 1 0
16	1 0 1	0 0 0 1
24	1 0 0	0 0 0 0

16dB

8dB

Title	PLL Board: Amp	
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet 3 of 13
File: D:\Users\..\PLL2A.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg

4dB

2dB

1dB

U10B
MAX333A
Shown logic 0

U13A
MAX333A
Shown logic 0

U13B
MAX333A
Shown logic 0

U13C
MAX333A
Shown logic 0

U13D
MAX333A
Shown logic 0

U14
AD829

U15
AD829

U16
AD829

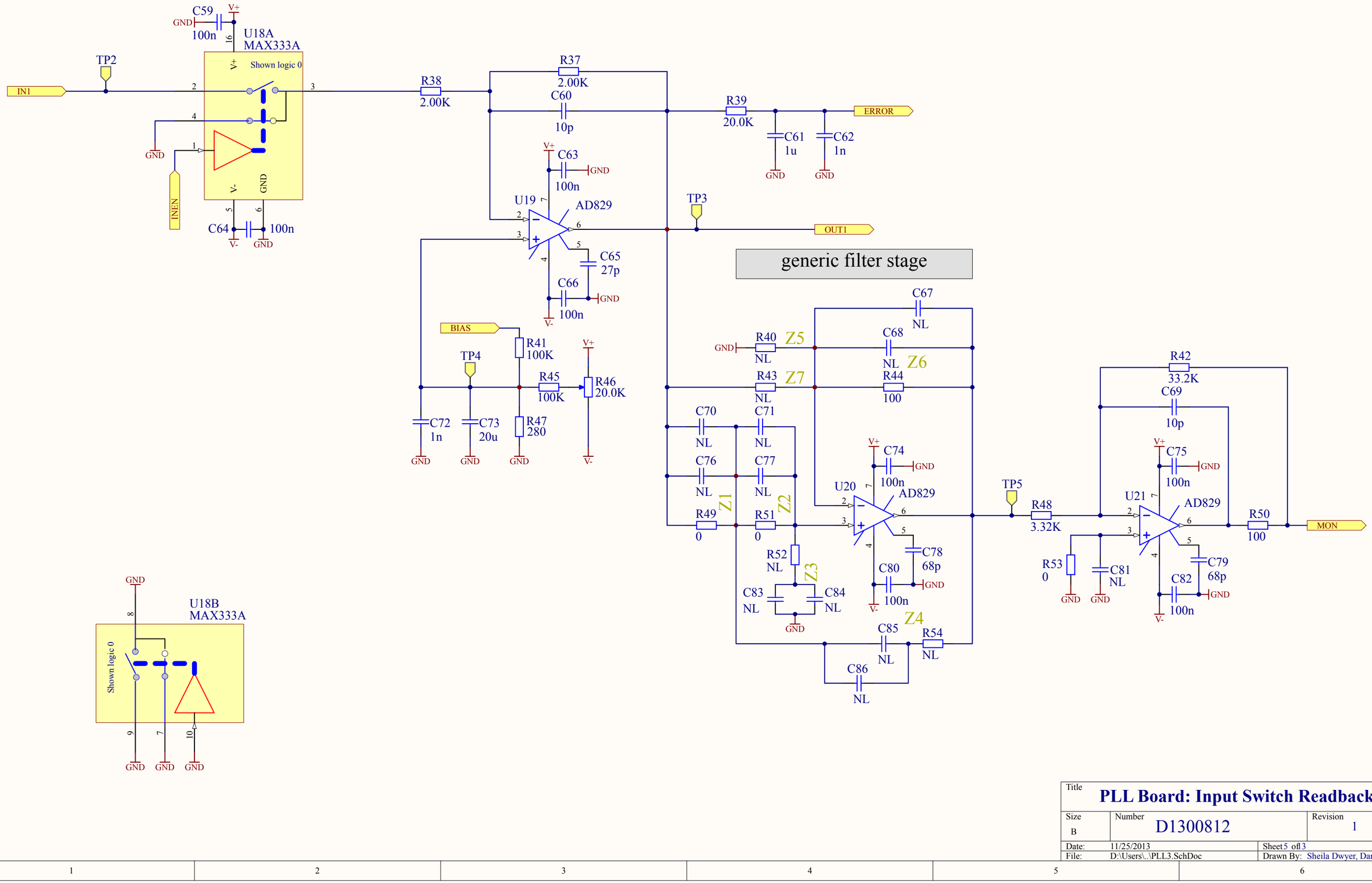
U17
AD829

R29 10.0K
R30 1.20K
R31 499
R32 2.00K
R33 2.00K
R34 100
R35 374
R36 3.32K

C42 100n
C43 100n
C44 100n
C45 33p5
C46 47p5
C47 100n
C48 100n
C49 100n
C50 18p
C51 68p
C52 100n
C53 100n
C54 68p
C55 68p5
C56 100n
C57 100n
C58 33p

GND
V+
V-
S
G2
G1
G0
OUT

Title	PLL: Amp		
Size: B	Number: D1300812	Revision: 1	
Date: 11/25/2013		Sheet 4 of 13	
File: D:\Users\..\PLL2B.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg	

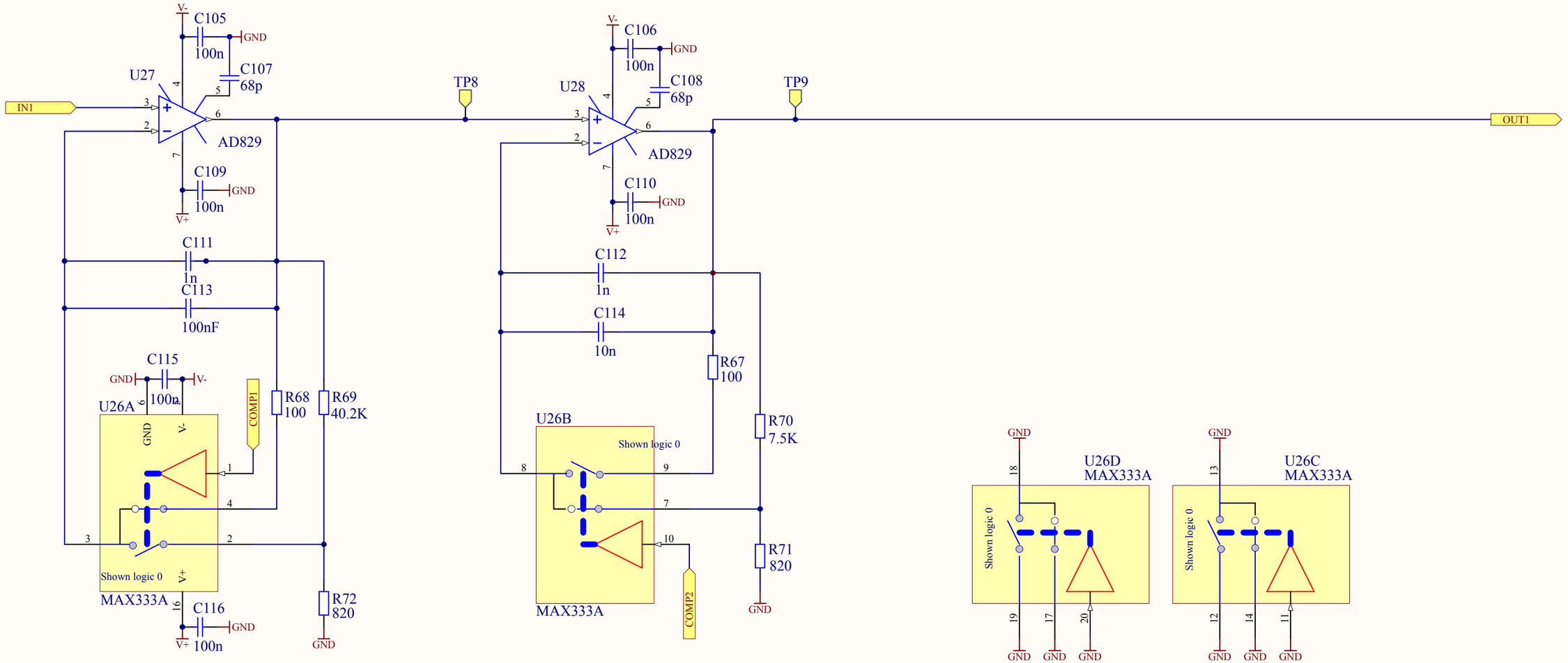


Title	**PLL Board: Input Switch Readbacks**		
Size: B	Number: D1300812	Revision: 1	
Date: 11/25/2013	Sheet 5 of 13		
File: D:\Users\..\PLL3.SchDoc	Drawn By: Sheila Dwyer, Daniel Sigg		

Title	**PLL Board: Excitation**		
Size: B	Number: D1300812	Revision: 1	
Date: 11/25/2013		Sheet 6 of 13	
File: D:\Users\..\PLL4.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg	

40Hz/2kHz pole/zero pair

2kHz/20kHz pole/zero pair



Title	**PLL:Common Filters**		
Size: B	Number: D1300812	Revision: 1	
Date: 11/25/2013		Sheet 7 of 13	
File: D:\Users\..\PLL5.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg	

generic filter stage
dc gain of 1

optional daughter board

IN2

JP1
Header 10X2A

JP2
Header 10X2A

VCC
V+
V-
GND

TP11

C131 100n
U31A MAX333A
Shown logic 0

Z1 R85 3.32K
TP12

OPTION

C140 100n

C117 NL
C118 NL
R74 NL
Z5
Z6
R75 NL
Z7
R76 100

C121 NL
C122 NL
C124 NL
C125 NL
Z1
Z2
R80 0
R81 0

U30 AD829
C123 100n
C129 68p
C130 100n
R82 NL
Z3
C133 NL
C132 NL
C134
R83 NL
C135 NL
Z4

Z1
R86 3.32K
R87 20.0K
CONTROL
C138 1n
C139 1u

TP10

R73 3.32K
C119 10p
C120 100n
U29 AD829
R77 3.32K
R78 100
MON
R79 0
C127 NL
C126 68p
C128 100n

R84 3.32K
C136 NL
C137 10p
Z2
C141 100n
U32 OP27
R88 100
C142 NL
C143 100n
OUT

P24
D5
K1 IM07GR
J7 SMA
Q1 PZT2222A
D6
R89 3.32K

U31B
Shown logic 0
R90 1.00K
INTERNAL
MAX333A

U31D MAX333A
Shown logic 0

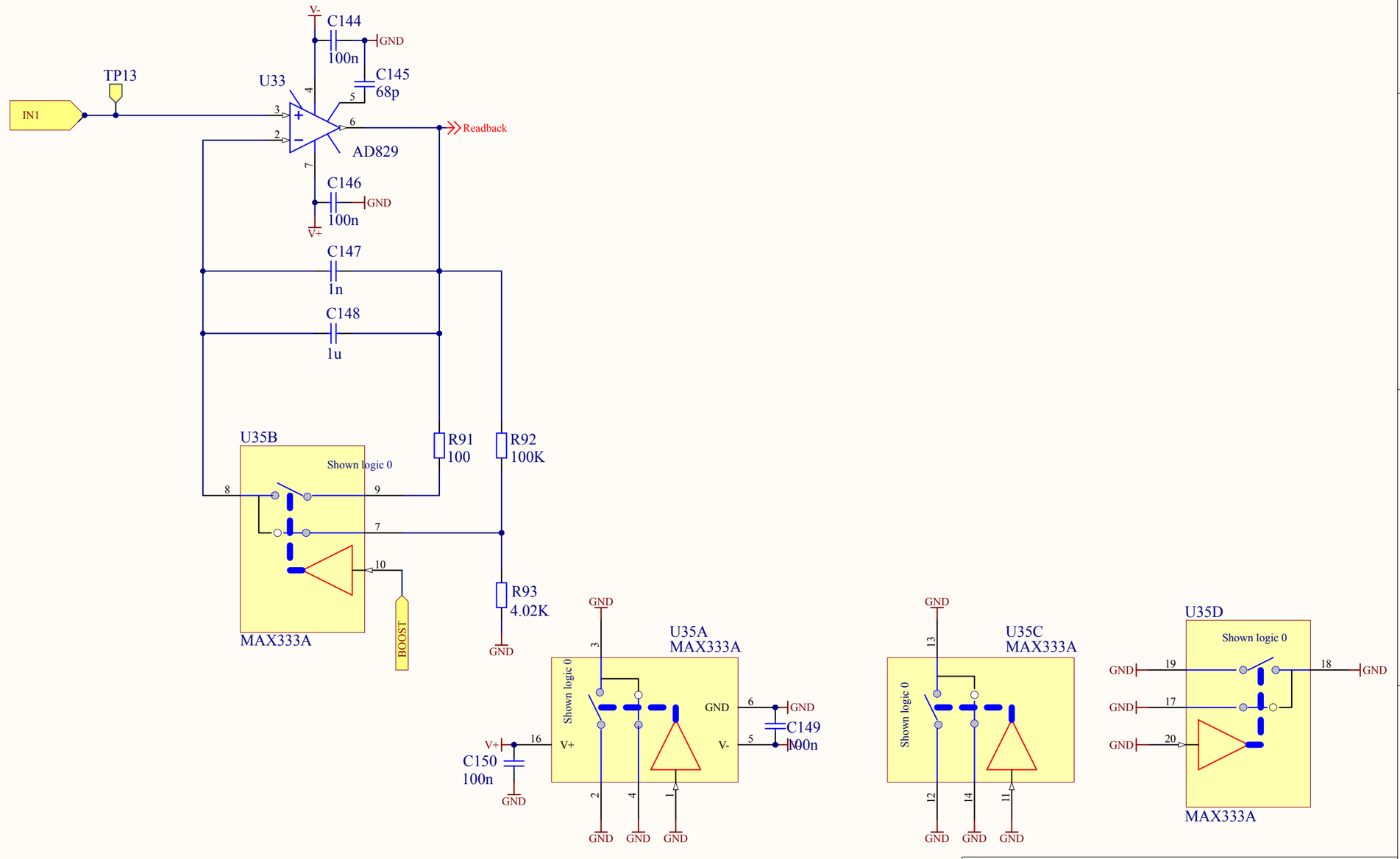
U31C MAX333A
Shown logic 0

M1 M3 standoff, 12mm
M3 M3 standoff, 12mm
M5 M3 standoff, 12mm
M7 M3 standoff, 12mm
Digi-Key
24434K-ND

M2 M3 pan, 8mm
M4 M3 pan, 8mm
M6 M3 pan, 8mm
M8 M3 pan, 8mm
M9 M3 pan, 8mm
M10 M3 pan, 8mm
M11 M3 pan, 8mm
M12 M3 pan, 8mm
McMaster-Carr
90317A115

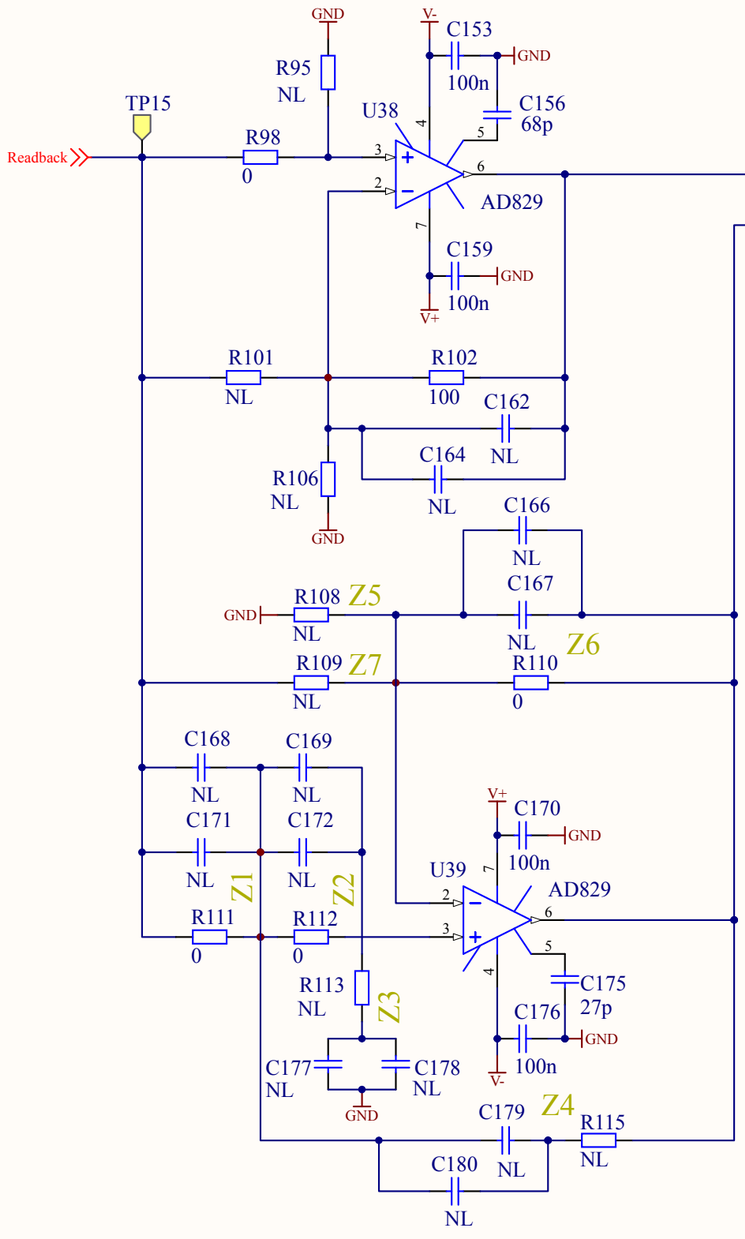
Title: **PLL Board: VCO path**		
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet8 of 13
File: D:\Users\..\PLL6.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg

1.6Hz/40Hz pole/zero pair

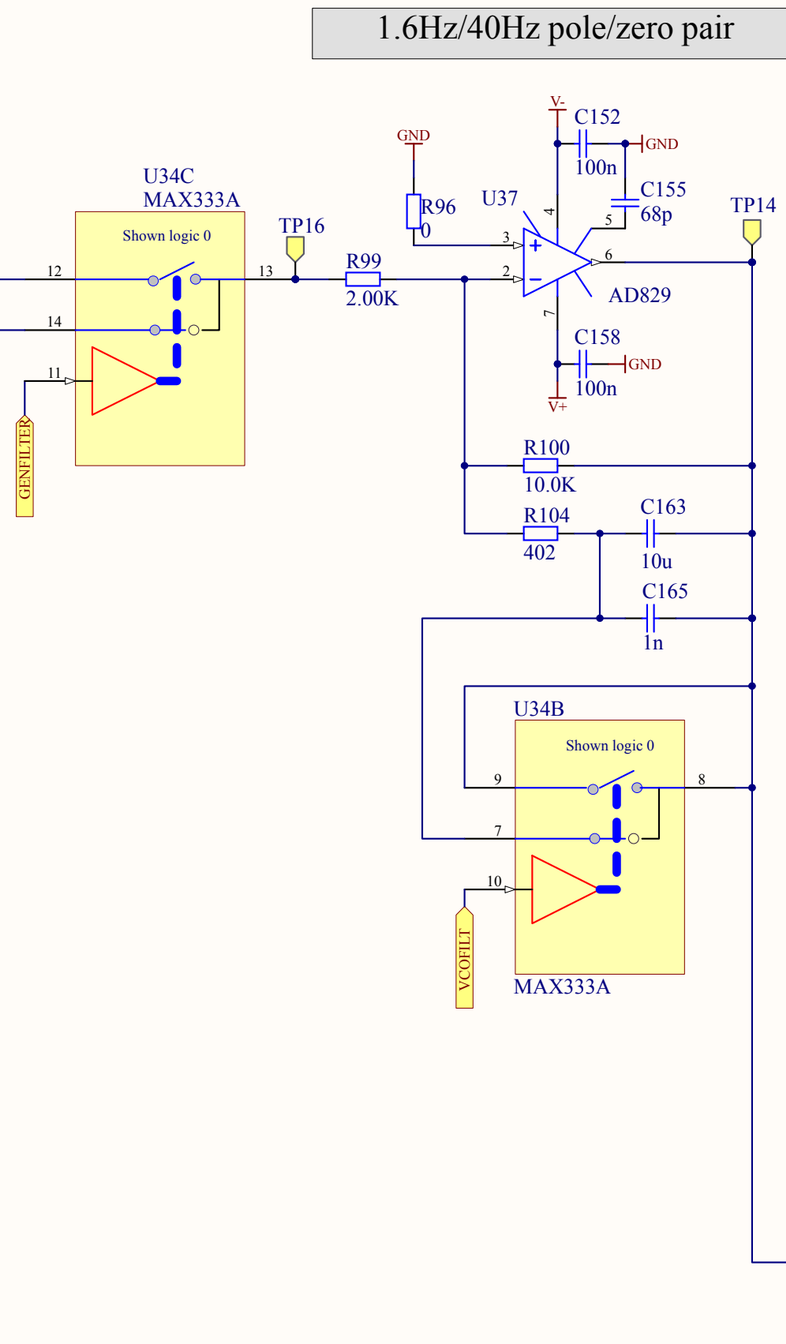


Title	**PLL Board: Readout Path**	
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet 9 of 13
File: D:\Users\..\PLL7A.SchDoc		Drawn By: Daniel Sigg

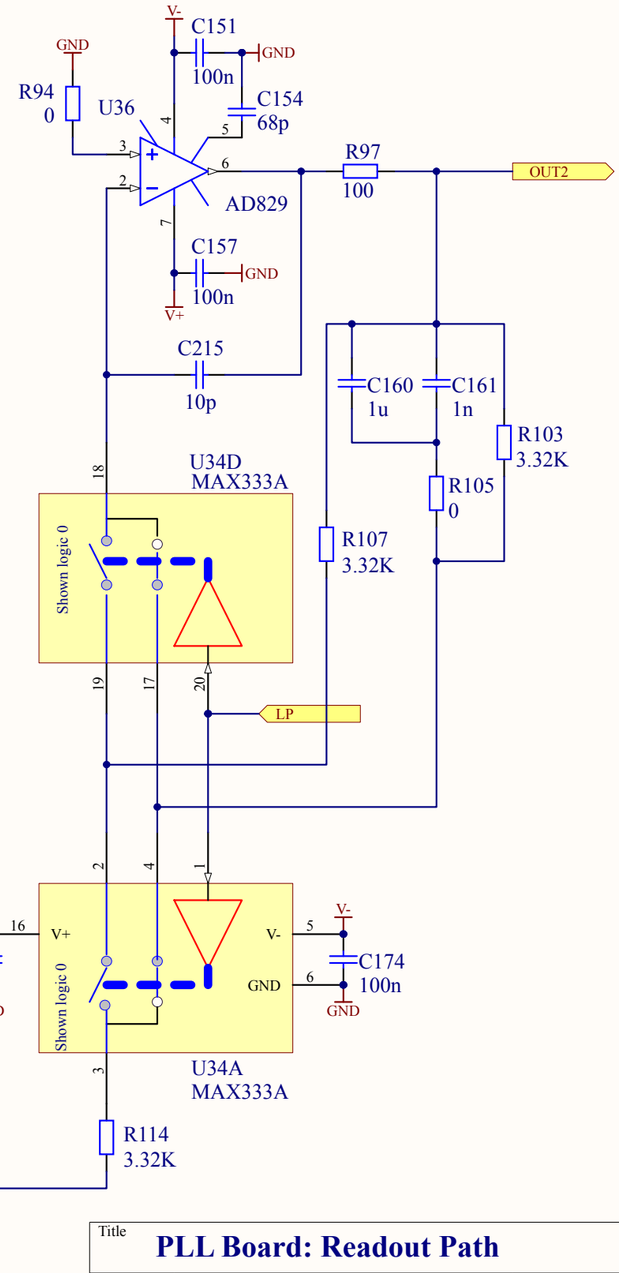
generic filter stage



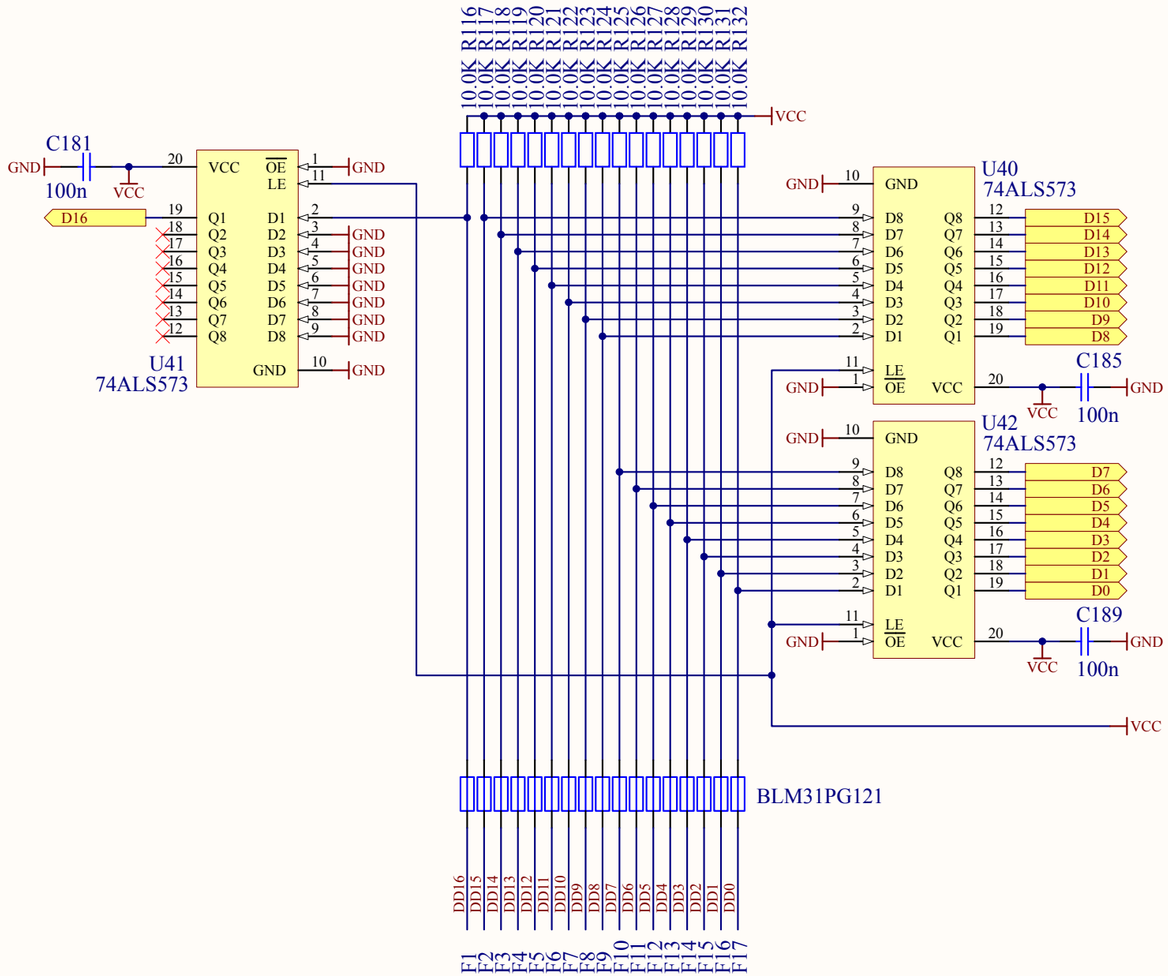
1.6Hz/40Hz pole/zero pair

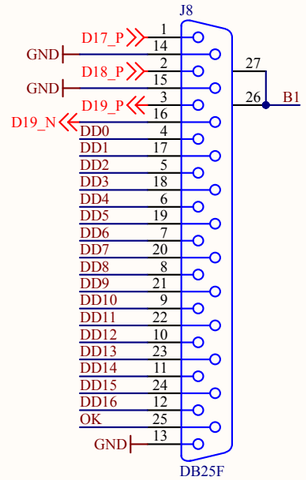


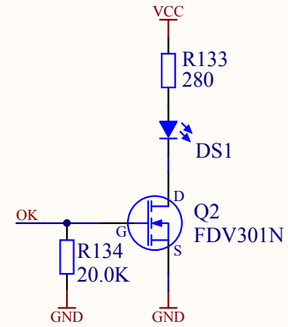
48Hz pole

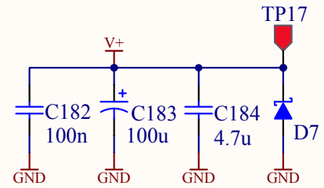


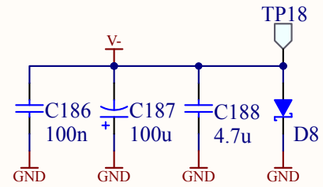
Title: **PLL Board: Readout Path**		
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet 10 of 13
File: D:\Users\..\PLL7B.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg

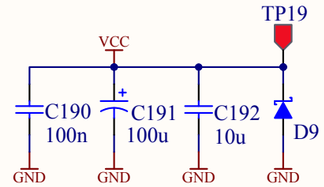


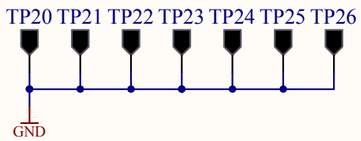


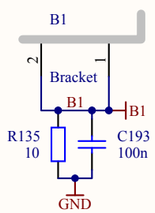


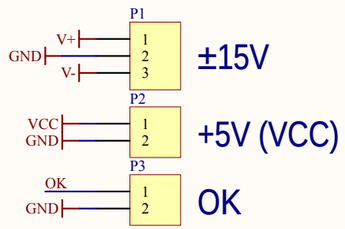




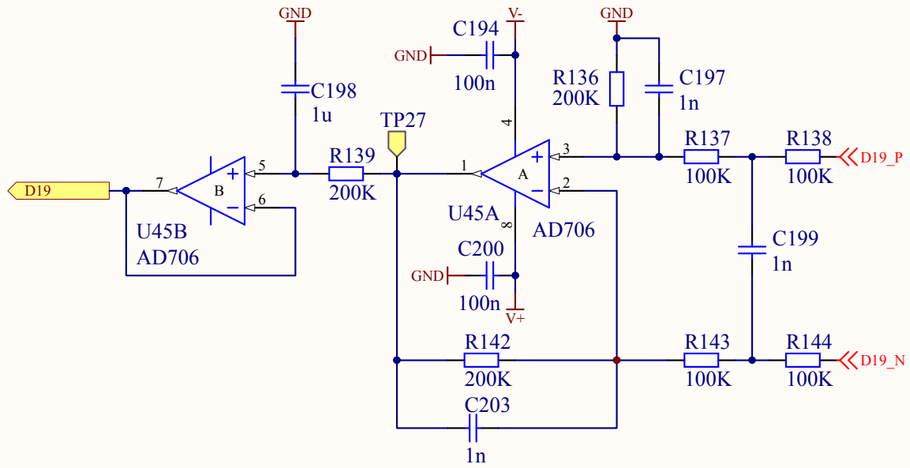


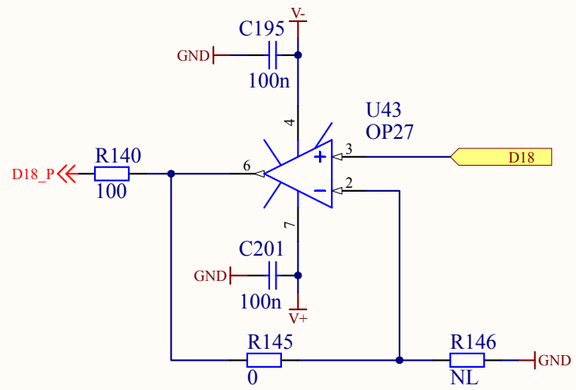


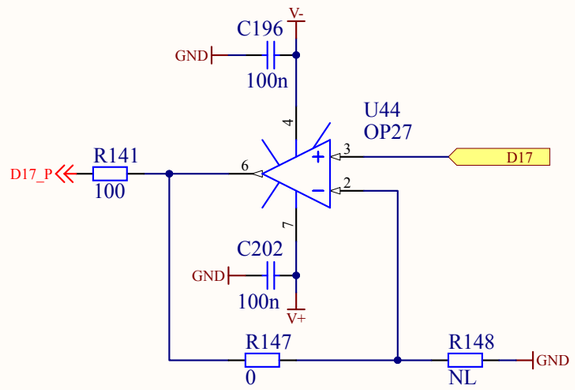




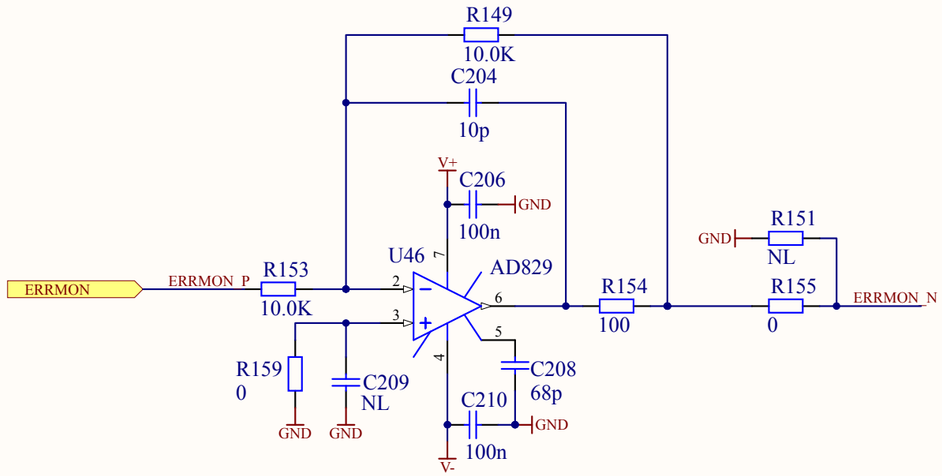
Title: **PLL Board: Backplane(P1)**		
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet 11 of 13
File: D:\Users\..\PLL8A.SchDoc		Drawn By: Sheila Dwyer, Daniel Sigg

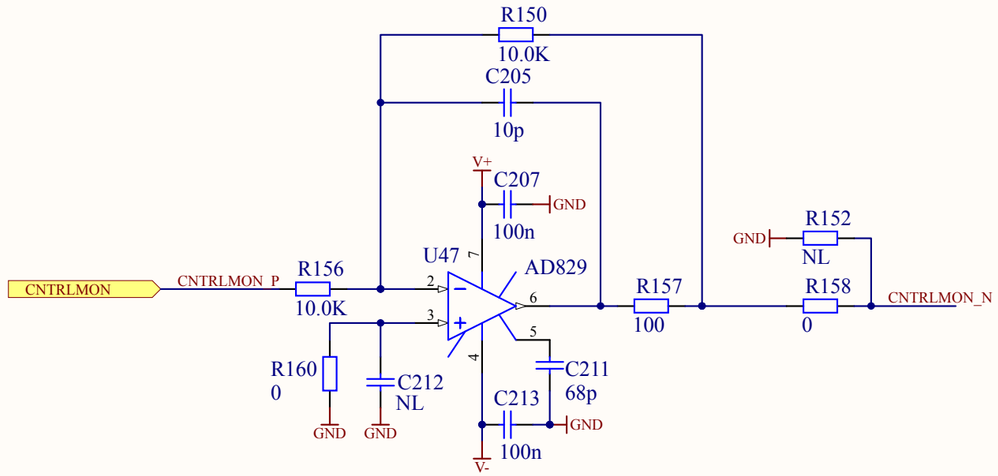


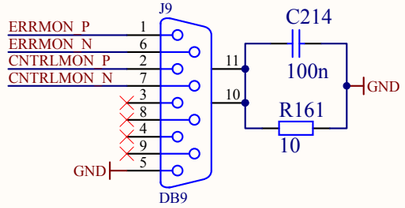




Title: **PLL Board: Backplane(P2)**		
Size: B	Number: D1300812	Revision: 1
Date: 11/25/2013		Sheet 12 of 13
File: D:\Users\..\PLL8B.SchDoc		Drawn By: Sheila Dwyer, Daneil Sigg







Title	**PLL Board: DAQ**
Size: B	Number: D1300812
Revision: 1	
Date: 11/25/2013	Sheet 13 of 13
File: D:\Users\..\PLL9.SchDoc	Drawn By: Sheila Dwyer, Daniel Sigg