

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
- LIGO -
CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	LIGO-T950137-00 - D	7/31/95
Description of the Electronics for the FMI Wavefront Experiment		
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Distribution of this draft:

This is an internal working note
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1 INTRODUCTION

One of the challenges of a 4 km long interferometer arm is to keep the laser beam aligned with the optical axes defined by the interferometer optics, e.g., to make sure that the far mirror returns the beam exactly in the direction of the incident beam. Furthermore, if the interferometer contains arm and recycling cavities, all the additional cavity mirrors have to be aligned as well. The purpose of the fixed mass interferometer experiment is to show that the concept of the wavefront alignment system works as expected in a real-world implementation.

This document gives an overview of the electronic layout of the FMI wavefront experiment¹. A glossary can be found at the end of the document.

2 HARDWARE LAYOUT

2.1 Interferometer

The laser light used for locking the interferometer consists of a carrier, a subcarrier and several sidebands which are phase modulated onto these two carriers (see Table 1). The required frequencies are generated by 4 master clock oscillators. The modulated laser light is fed into the fixed mass interferometer, consisting of two arm cavities and a recycling cavity (see Fig. 1 and Table 2). The locking of the cavity length is performed by measuring and demodulating both the reflected light from the recycling mirror and light coming out at the dark port with a total of four photodiodes. All the mirrors and the beamsplitter of the interferometer are mounted on PZTs (either slow or fast) which control their spatial position.

Table 1: Modulation Sidebands and their Frequencies

Description	Name	Sideband	Modulation	f (MHz)
Subcarrier	SC	single	acousto-optical, double pass	391.0
Carrier sideband	CSB	double	phase, Pockels cell	19.54 ^a
Subcarrier sideband 1	SCSB1	double	phase, Pockels cell	39.07
Subcarrier sideband 2	SCSB2	double	phase, Pockels cell	32.33

a. optional: 58.6 MHz.

-
1. A description of the optical layout and the design considerations for the interferometer can be found elsewhere:
 Y. Hefetz and N. Mavalvala, “*Demonstration of Automatic Alignment of a suspended Fabry-Perot Cavity*”.
 N. Mavalvala and Y. Hefetz, “*Design Considerations for a Table-Top Prototype Interferometer*”, LIGO-T952109-01-I (1995).
 D. Shoemaker, “*ASC DRD*”, Detector Alignment Sensing/Control Design, LIGO-T952007-00-I (1995).

The angular misalignment is measured with 5 or 6 wavefront sensors, consisting of a quadrant photodiode and the necessary demodulator boards. The wavefront sensor heads are placed so, that they can measure the reflected light (TEM01) from the recycling mirror, the light coming out at the dark port and alternatively also the light reflected by the near mirrors of the arm cavities. To be able to correct for the detected misalignment angles, the vertical and horizontal angles of the two back mirrors, the two near mirrors and the recycling mirror are controlled by PZTs. Furthermore, the angles of these mirrors are measured directly by 5 pointing systems. This allows a comparison between the amount of TEM01 mode in the interferometer and the true physical misalignment angles.

Beam centering information is obtained from 2 quadrant photo diodes which are mounted behind the two back mirrors of the arm cavities and which measure the amount of transmitted light. Both the intensity of the incoming laser beam and the recycling gain are measured with two single photodiodes.

Table 2: Optical Components of the Interferometer

Description	Abbreviation	spatial PZT	angular PZTs
Beamsplitter	BS	slow	—
Back mirror of arm 1	BM1	fast	H^a+V^b
Near mirror of arm 1	NM1	slow	H+V
Back mirror of arm 2	BM2	fast	H+V
Near mirror of arm 2	NM2	slow	H+V
Recycling mirror	RM	slow	H+V
Common near Michelson	CNM	fast	—
Differential near Michelson	DNM	fast	—

- a. horizontal
- b. vertical

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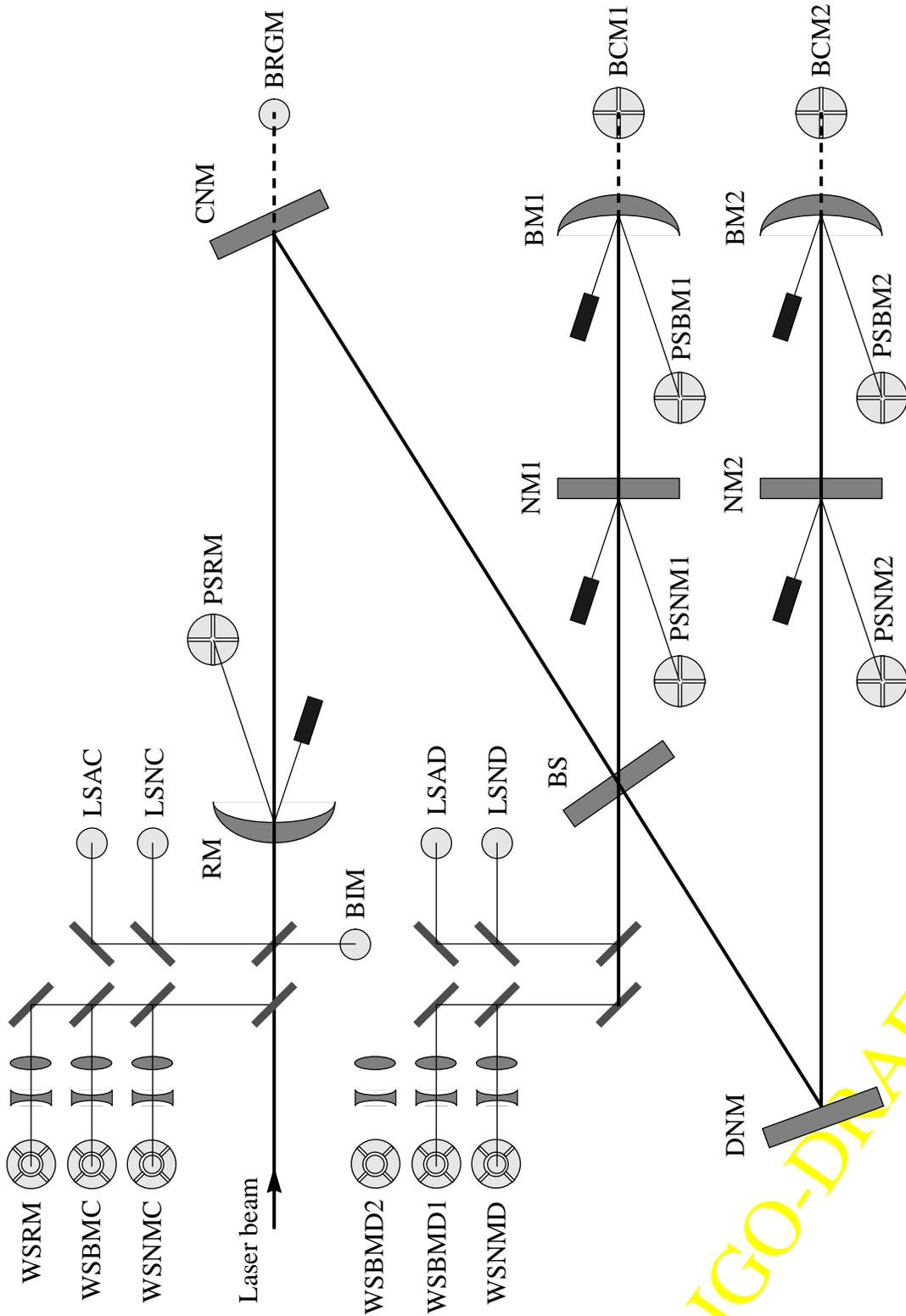


Figure 1: Layout of the Interferometer

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Table 3: Measuring Subsystems (Sensors)

Description	Abbreviation	Detector	Chn ^a
Length sensing, near Michelson, common	LSNC	photodiode	1
Length sensing, near Michelson, differential	LSND	photodiode	1
Length sensing, arms, common	LSAC	photodiode	1
Length sensing, arms, differential	LSAD	photodiode	1
Wavefront sensing, back mirrors, common	WSBMC	5-segment photodiode ^b	15 ^c
Wavefront sensing, back mirrors, differential 1	WSBMD1	5-segment photodiode	15
Wavefront sensing, near mirrors, common	WSNMC	5-segment photodiode	15
Wavefront sensing, near mirrors, differential	WSNMD	5-segment photodiode	15
Wavefront sensing, recycling mirror	WSRM	5-segment photodiode	15
Wavefront sensing, back mirrors, differential 2	WSBMD2	5-segment photodiode	15
Pointing system, back mirror, arm1	PSBM1	quadrant photodiode	3 ^d
Pointing system, near mirror, arm1	PSNM1	quadrant photodiode	3
Pointing system, back mirror, arm2	PSBM2	quadrant photodiode	3
Pointing system, near mirror, arm2	PSNM2	quadrant photodiode	3
Pointing system, recycling mirror	PSRM	quadrant photodiode	3
Beam centering monitor, arm 1	BCM1	quadrant photodiode	3 ^e
Beam centering monitor, arm 2	BCM2	quadrant photodiode	3
Beam intensity monitor	BIM	photodiode	1
Beam recycling gain monitor	BRGM	photodiode	1

- a. Number of read-out channels.
- b. Quadrant with central circular piece.
- c. DC signal: 5; RF I-phase signal: 5; RF Q-phase signal: 5.
- d. DC signals: Vertical and horizontal differences plus sum.
- e. Same as pointing system.

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2.2 Laser Table

2.2.1 Laser Frequency Stabilization

The frequency of the laser is stabilized by locking to a reference cavity (see Fig. 2). The incoming laser beam is phase modulated at 12 MHz with a Pockels cell. A steering lens and a steering mirror are used to align the offset and angle of the incident beam to the fundamental mode of the cavity, respectively. The reflected light of the cavity is measured with a photodiode and demodulated to obtain the error signal which is used to control the laser frequency. The transmitted light is measured with another photodiode and a camera.

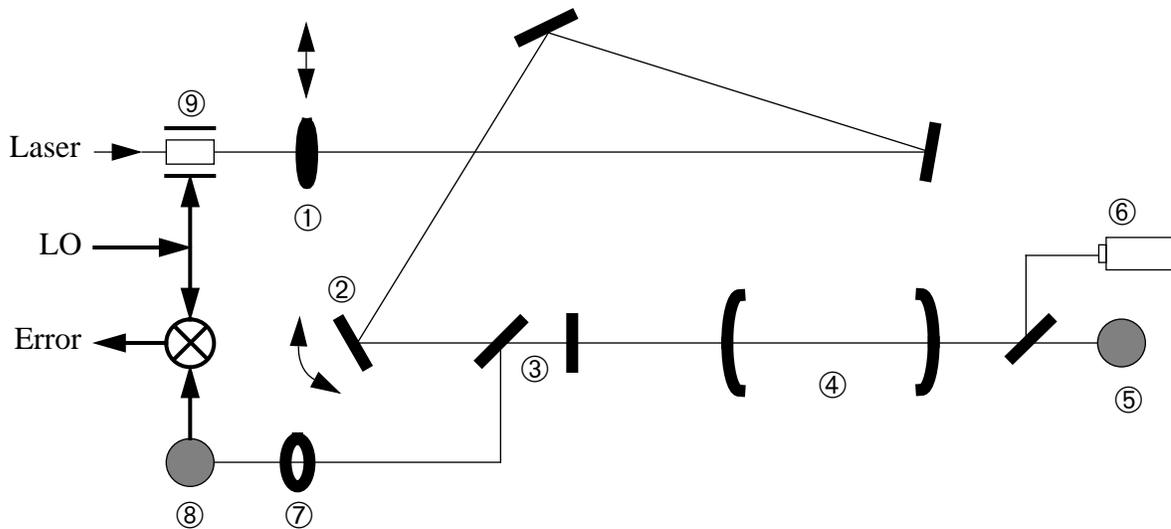


Figure 2: Optical Layout of the Laser Frequency Stabilization

- ① Steering lens, ② Steering mirror, ③ Polarized beamsplitter with $\lambda/4$ plate,
- ④ Reference cavity, ⑤ Photodiode for transmitted light, ⑥ Camera, ⑦ Iris,
- ⑧ RF Photodiode for reflected light and ⑨ Pockels cell.

The setup of the electronics is shown in Fig. 3. An oscillator is used to generate the high frequency signal at 12 MHz which is used to drive the Pockels cell and to demodulate the signal from the RF photodiode (limiter/phase shifter and laser loop amplifier). The demodulated signal serves as an error signal for the laser PZT driver. A camera and a photodiode which measure the transmitted light are used mainly for diagnostics and mode matching.

A description how to engage the frequency stabilization loop can be found in Appendix A.

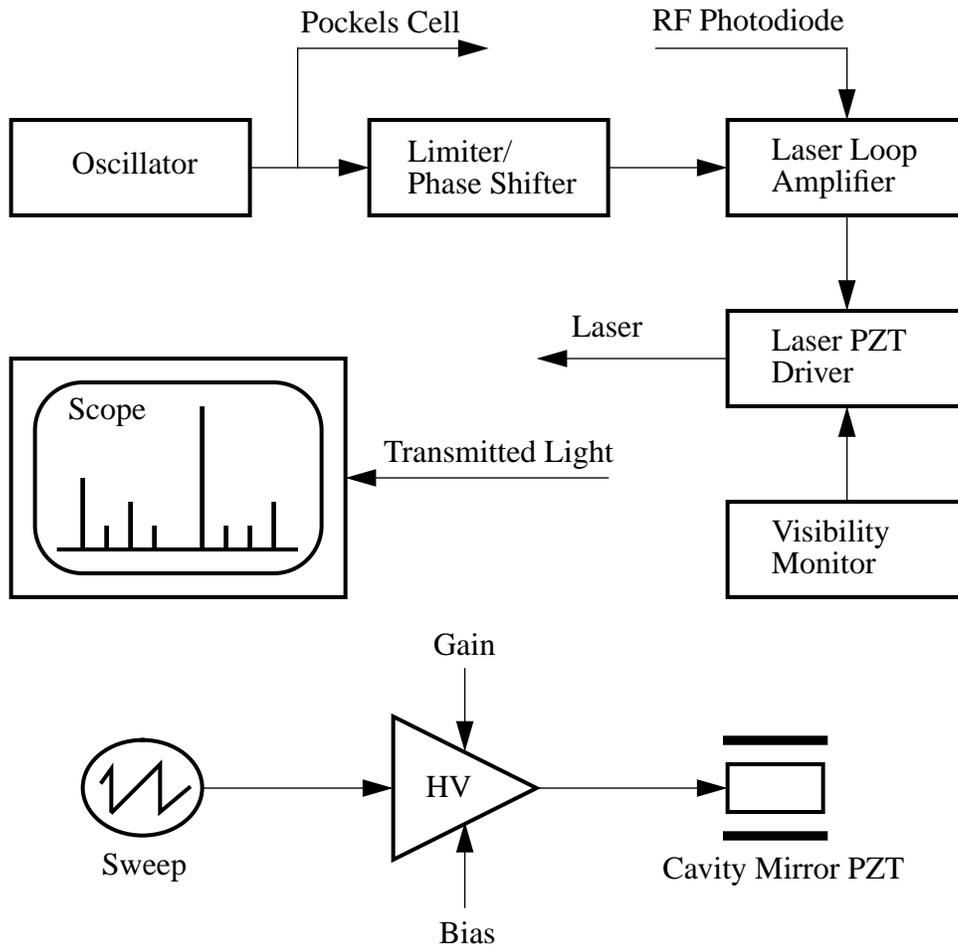


Figure 3: Electronics of the Laser Frequency Stabilization Subsystem

2.3 Length Sensing and Control

There are 4 constraints on the interferometer which affect the resonance condition in the cavities. One way to express them is as follows:

- The carrier must be resonant in arm cavity 1.
- The carrier must be resonant in arm cavity 2.
- The carrier must be resonant in the recycling cavity.
- There should be minimal carrier power leaking out at the dark port.

The sum of the two arm lengths is measured with a photodiode (LSAC) which detects the beating of the reflected light between the carrier and its sidebands (see Fig. 4). The difference of the two arm cavity lengths is measured by a photodiode at the dark port (LSAD). The two measured RF signals are separately down-converted. The resulting error signals are added and subtracted to

obtain the error signals of the two arm cavities. The error signals are fed into a compensation network which produces the needed control signals for the near and the back mirrors. The near mirrors are mounted on slow PZTs which have a large dynamic range, whereas the back mirrors are mounted on fast PZTs which have a small dynamic range. The common length of the near Michelson interferometer is measured with the subcarrier (SC) and its second sideband (SCSB2) at the symmetric port (LSNC), whereas its differential length is measured with the subcarrier and its first sideband (SCSB1) at the dark port (LSND). No adding or subtracting is required here, because the recycling mirror and the CNM both adjust the common length, whereas the differential length is adjusted by the beam splitter and the DNM. High voltage drivers are used to generate the required steering signals for the PZTs. A detailed description of the PZT compensation network is given in Appendix B. The module and channel assignment lists for the length sensing and control can be found in Table 4 and Table 5.

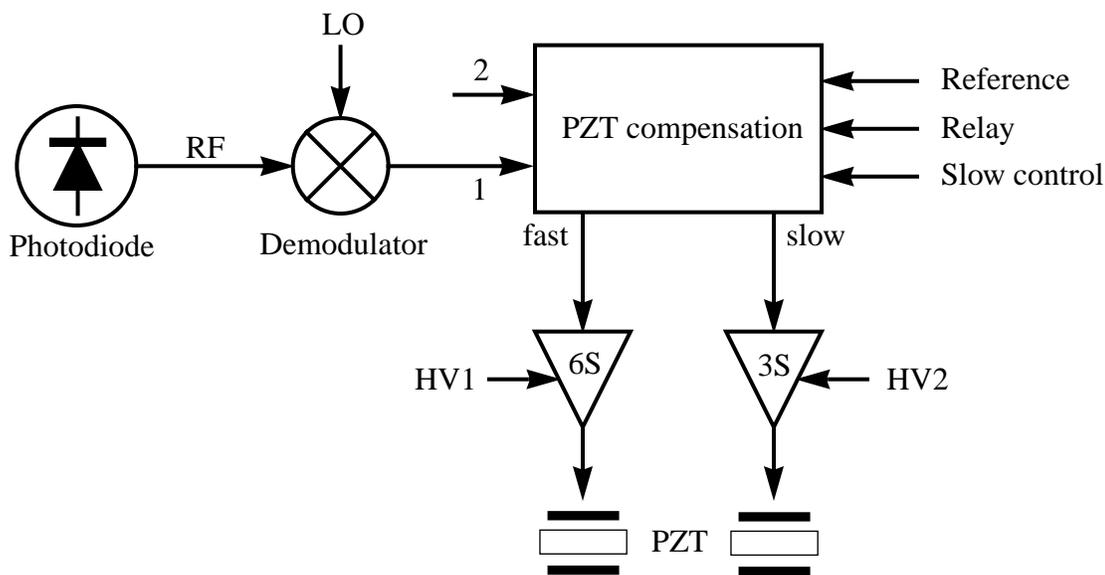


Figure 4: Length Sensing and Control

Table 4: Channel and Module Assignment: Length Sensing

Channel	LSAD	LSAC	LSND	LSNC
Modulation	CSB	CSB	SCSB1	SCSB2
Demodulator module / channel	1 / 1	1 / 2	2 / 1	2 / 2

Table 5: Channel and Module Assignment: Length Control

	Arm 1		Arm 2		Recycle. diff.		Recycle. common	
Input (1/2)	LSAD	LSAC	LSAD	LSAC	LSND	—	LSNC	—
Reference	DA11		DA12		DA13		DA14	
Relay	BO13		BO14		BO15		BO16	
Sweep	DA11		DA12		DA13		DA14	
Output (fast/slow)	AD97	AD98	AD99	AD100	AD101	AD102	AD103	AD104
HV Driver (6S/3S)	1 / 1 ^a	1 / 1	1 / 2	1 / 2	1 / 3	2 / 1	1 / 4	2 / 2
PZT (mirror)	BM1	NM1	BM2	NM2	DNM	BS	CNM	RM

a. Module number / channel number.

2.4 Wavefront Sensing and Control

Any angular misalignment of one of the interferometer mirrors can be seen as a transfer of light power from the TEM00 mode into higher order modes, mostly TEM01 and TEM10 for small angular misalignment. Hence, an angular misalignment can be detected by measuring the amount of TEM01 and TEM10 modes in the interferometer. To disentangle the misalignment signals originating from different mirrors, the beating between the desired TEM01 mode and the corresponding TEM00 sideband is observed with a 5-segment photodiode after the beam has passed a telescope which selects the appropriate Guoy phase shift. This signal is down-converted in I (‘in-phase’) and Q (‘quadrature’) phase to restore its complete information. The reconstruction of the signal from both the I and the Q information makes a phase shifter for the local oscillator unnecessary. However, a phase shifter can easily be added for “diagnostic purposes”.

Additionally, the average light power on the photodiodes is measured as a DC signal. It provides useful information about the beam intensity and its centering (see Fig. 5).

The center diode can be used to determine the contribution of the “doughnut”-mode (a sum of TEM02 and TEM20) and is therefore a measure how well the curvature of the mirrors is matched to the properties of the Gaussian beam. In the present configuration this center diode is not implemented. However, it usually shows up in drawings and in passing in descriptions.

The measured signals from the wavefront sensors are sampled with ADC boards which are hosted in a VME chassis. A CPU reads these data periodically and processes them to obtain the feedback control signals for the actuators which steer the angles of the mirrors (see Fig. 6). A recycling interferometer with Fabry-Perot arm cavities has 10 angular degree of freedoms: 5 each in the vertical and the horizontal directions. These 10 misalignment angles are measured with either 5 or 6 wavefront sensors. Their channel and module assignments are listed in Table 6. The computed feedback control signals are converted into analog signals with a VME hosted DAC board. After passing a filter which smooths the step function produced by the DAC (zero-order hold), the signals are applied to the angular PZTs via high-voltage drivers. Their channel and module

assignment list can be found in Table 7. A detailed specification of the performance of the wavefront sensors is given in Appendix . A complete description of the compensation network for the angular degree of freedoms is given in Appendix E.

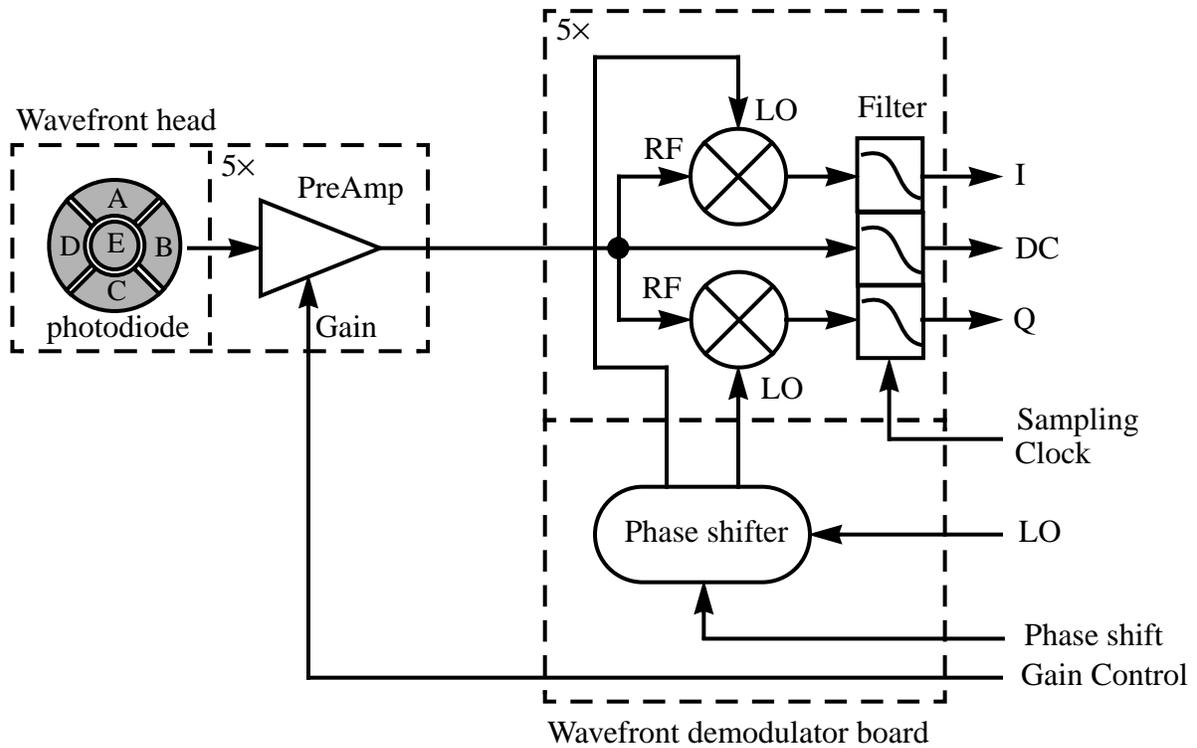


Figure 5: Wavefront Sensor

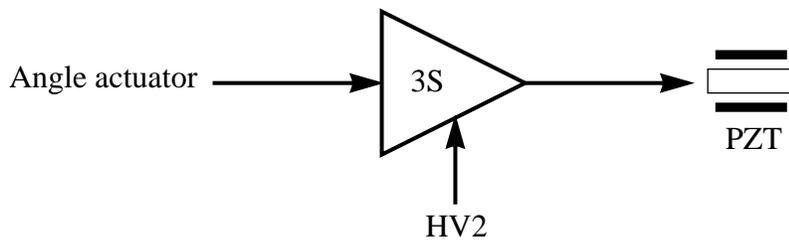


Figure 6: Wavefront Controller

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Table 6: Channel and Module Assignment: Wavefront Sensing

	WSNMD	WSNMC	WSRM	WSBMD1	WSBMC	WSBMD2
Modulation	SCSB1	SCSB2	SCSB2	CSB	CSB	CSB
Demodulator module	1	2	3	4	5	6
A ^a , DC	AD01	AD16	AD33	AD48	AD65	AD80
B, DC	AD02	AD17	AD34	AD49	AD66	AD81
C, DC	AD03	AD18	AD35	AD50	AD67	AD82
D, DC	AD04	AD19	AD36	AD51	AD68	AD83
E, DC	AD05	AD20	AD37	AD52	AD69	AD84
A, I phase	AD06	AD21	AD38	AD53	AD70	AD85
B, I phase	AD07	AD22	AD39	AD54	AD71	AD86
C, I phase	AD08	AD23	AD40	AD55	AD72	AD87
D, I phase	AD09	AD24	AD41	AD56	AD73	AD88
E, I phase	AD10	AD25	AD42	AD57	AD74	AD89
A, Q phase	AD11	AD26	AD43	AD58	AD75	AD90
B, Q phase	AD12	AD27	AD44	AD59	AD76	AD91
C, Q phase	AD13	AD28	AD45	AD60	AD77	AD92
D, Q phase	AD14	AD29	AD46	AD61	AD78	AD93
E, Q phase	AD15	AD30	AD47	AD62	AD79	AD94
Gain control 1	BO01	BO03	BO05	BO07	BO09	BO11
Gain control 2	BO02	BO04	BO06	BO08	BO10	BO12
Phase shift	DA17	DA18	DA19	DA20	DA21	DA22

a. Diode number

Table 7: Channel and Module Assignment: Wavefront Control

	BM1	NM1	BM2	NM2	RM
3S vertical	3 / 1	4 / 1	5 / 1	6 / 1	7 / 1
3S horizontal	3 / 2	4 / 2	5 / 2	6 / 2	7 / 2
Vertical Angle	DA1	DA3	DA5	DA7	DA9
Horizontal Angle	DA2	DA4	DA6	DA8	DA10

2.5 Pointing System

The pointing system provides an independent measurement of the mirror angles. This makes it possible to relate the measured amount of TEM₀₁ and TEM₁₀ modes with the true physical mirror angles, and hence test the modal model. Each pointing system consists of a diode laser which points to a reflecting part on one of the interferometer mirror. The reflected beam is then directed to a quadrant photodiode which measures horizontal and vertical intensity asymmetries (see Fig. 7). A list of the channel assignment for the pointing system can be found in Table 8.

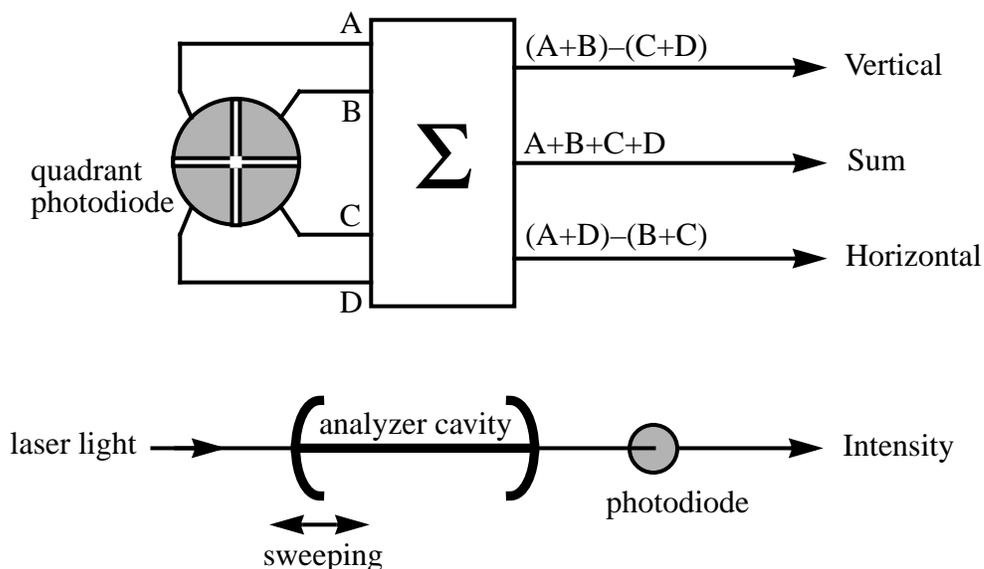
**Figure 7: Pointing System and Beam Intensity Monitor**

Table 8: Channel Assignment: Pointing System

	PSBM1	PSNM1	PSBM2	PSNM2	PSRM
Vertical	AD105	AD108	AD111	AD114	AD117
Horizontal	AD106	AD109	AD112	AD115	AD118
Sum	AD107	AD110	AD113	AD116	AD119

2.6 Beam Intensity and Centering

To guarantee that the measured angular misalignment does not scale with the output power of the argon laser, the absolute light intensity is monitored by a single photodiode with a pick-off in the incoming beam. The measured misalignment signals also depend on the modulation depth of the sidebands which are used to lock the cavities. The intensities of the various modulation frequencies are continuously monitored by a photodiode which measures the transmitted light of a sweeping analyzer cavity (see Fig. 7). Together, the signals of the two photodiodes provide all the necessary normalization factor for the wavefront sensing.

The light which is transmitted through the back mirrors of the interferometer is analyzed with the same kind of quadrant photodiode detector as used in the pointing system. This allows both a determination of the light power in the arm cavities and a measurement of the lateral beam position (centering) on the back mirrors. The recycling gain is measured with an additional single photodiode placed behind the CNM. The channel assignment of the beam monitors can be found in Table 9.

Table 9: Channel Assignment: Beam Intensity and Centering

	BCM1	BCM2	BIM	BRGM
Vertical	AD120	AD123	—	—
Horizontal	AD121	AD124	—	—
Sum ^a	AD122	AD125	AD126	AD128
Cavity sweep signal	—	—	AD127	—
3S (module. / channel)	—	—	1 / 3	—

a. Corresponds to the total intensity for the single photodiodes.

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2.7 Data Acquisition System

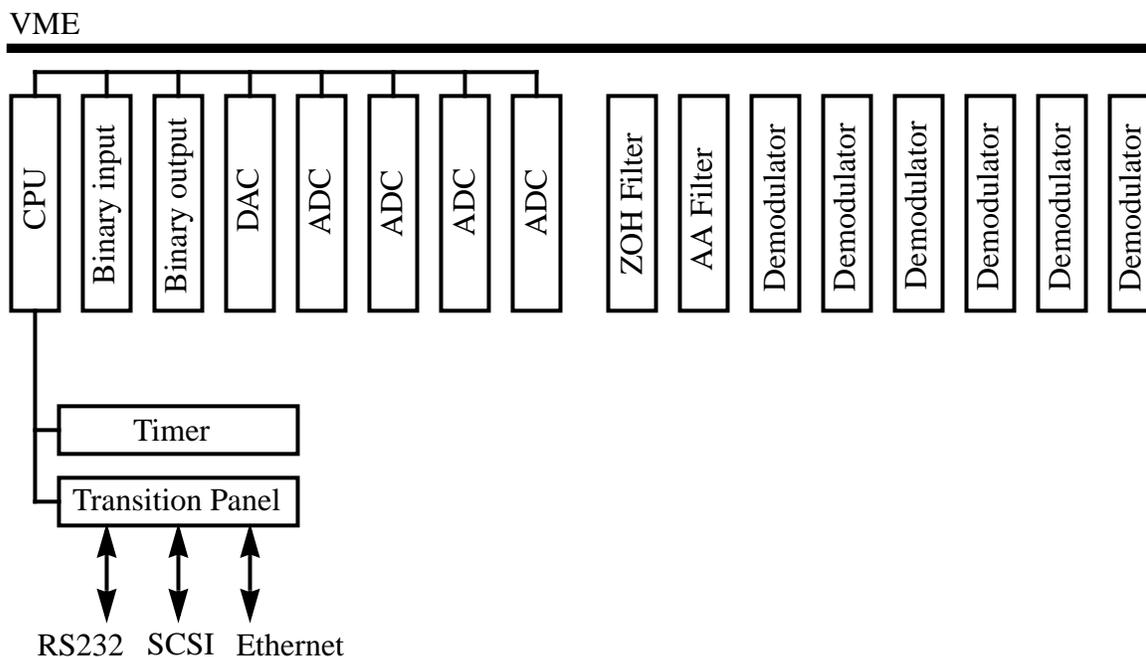


Figure 8: Data Acquisition System

2.8 Miscellaneous

2.8.1 Support Equipment

Support equipment are: high voltage power supplies, high frequency synthesizers, cameras, scopes, crates and racks (see Table 10). Because the carrier, its sideband, the subcarrier and one of its sideband all have to be resonant in the recycling cavity, the frequency ratios of the CSB, the SC and the SCSB1 have to be close to rational numbers. To obtain good relative stability between the different frequency generators, they can be locked to the same 10 MHz crystal oscillator. The frequency generators for the CSB, the SCSB1 and the SCSB2 are operated at +13 dBm. These frequencies are then fed into 6-way power splitters which reduce the signal level to about +4 dBm and which are used to drive the Pockels cell amplifiers and the demodulators for the length and the wavefront sensing.

2.8.2 Filters

Filters are needed on both ends of the digital interface to the analog signals. At the input an anti-aliasing (AA) filter should prevent an aliasing of high frequency noise down to the sampled frequency band. The demodulator boards already incorporate them, but all the other analog

Table 10: Support Equipment

Unit	Name	Description
High voltage power supply	HV1	± 400 VDC, 120 mA
High voltage power supply	HV2	0 to 1000 VDC, 225 mA
High Frequency Synthesizer	CSB	sine, 10 to 70 MHz, +13 dBm
High Frequency Synthesizer	SC	sine, 200 MHz, +10 dBm
High Frequency Synthesizer	SCSB1	sine, 10 to 50 MHz, +13 dBm
High Frequency Synthesizer	SCSB2	sine, 10 to 50 MHz, +13 dBm
XY-scope	SCOPE1	monitor of the intensity in the analyzer cavity
CCD camera	CAM1	monitor of the locking of the arm cavity 1
CCD camera	CAM2	monitor of the locking of the arm cavity 2
CCD camera	CAM3	monitor of the locking of the recycling cavity
NIM crate		standard NIM, 3 units
VME crate		12 slot VME, 8 slot analog
Rack		standard 19", 3 units

signals which are digitized by an ADC have to pass an AA filter stage. The AA filters are based on the switched capacitor technique which makes it particular easy to change the sampling rate.

On the other end the output of a DAC is a zero-order hold (ZOH), i.e. the waveform of the output signal is a step function. To convert this step function into a smooth curve, a low noise filter stage is needed. Because the corner frequency of the filter is only determined by the bandwidth of the subsequent device, no adjustment for the sampling rate has to be done and, hence, the filter can be implemented as a classical active filter. See Appendix F for more details.

2.9 Integration

The integration of the different subsystems into the FMI, can be divided into a physical level and a logical level. Physically, one has to guarantee that the hardware interfaces between the subsystems are compatible, i.e. the cables are equipped with the right connectors and wired correctly. Logically, one has to guarantee that the signal levels are compatible, e.g. the dynamic range of an ADC should match the dynamic range of the measured signal. In order to work properly together, the ADCs, the DACs and the CPU have to be synchronized on the same global timer.

2.9.1 Timing

2.9.2 Signal Levels

Both ADC and DAC have a voltage range of 10V (bipolar, single ended). Any measured or applied physical signal which has a total different range, must be converted by an instrumentation amplifier. Some signals may also need an additional offset to properly interface with the subsystems. Table 11 lists the range for all signals which are either measured by an ADC, provided by a DAC or generated by a binary output board.

Table 11: Voltage Level of ADC, DAC and Binary Signals

	Signal name	Signal range		Remarks
		full ^a	interest ^b	
Length sensing and control	Reference	15V	10V	
	Sweep	20V	10V	required resolution: 30 mV
	Output fast PZT	20V	10 to 20V	may need a divide by 2
	Output slow PZT	20V	10 to 20V	may need a divide by 2
	Relay	TTL	o.c. ^c	
Wavefront sensing and control	WSxx / RF	10V	10V	
	WSxx / DC	0 to 10V	0 to 10V	
	gain	TTL	o.c.	
	phase shift	10V	10V	
	angle	20V		required resolution
PS	angle	10V		required resolution
	sum	10V		required resolution
Beam intensity	difference	10V		required resolution
	sum	10V		required resolution
	sweep	10V	10V	

- Corresponds to the full dynamic range over which the signal is meaningful.
- Corresponds to the signal range of interest. If this range is not the same as the one from the ADC/DAC or binary input/output, the levels have to be adjusted by instrumentation amplifiers.
- open collector, TTL signals need a pull-up resistor

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2.9.3 Cabling

To ease the task of cabling, the signals from some of the VME boards which connect to multiple subsystems are distributed via a series of transition modules (see Table 12). Usually, they have a flat ribbon cable header on one side and a panel of BNC jacks on the other side. These BNC/ribbon header transition modules may use commercially available ribbon header/terminal block modules. The connections between the terminal blocks and the BNC jacks are then done with simple one-wire cables.

Table 12: Transition Panels

Panel	Signals	Connectors	Comment
TP1	AA filter	16 BNC / 10 9 pin D-sub / 50 pin ribbon header	analog signals
TP2	ZOH filter	16 BNC / 32 pin ribbon header	analog signals
TP3	Binary Input	32 BNC / 2 × 50 pin ribbon header	made for relays
TP4	Binary Output	32 BNC / 2 × 50 pin ribbon header	open collector, needs pull-up resistors
TP5	Timing	48 BNC / 50 pin ribbon header	provides also TTL I/O
TP6	CPU	SCSI, 2 × RS232, Ethernet	MVME712M
TP7 ^a	AA filter	32 BNC / 50 pin ribbon header	analog signals
TP8	ZOH filter	16 BNC / 32 pin ribbon header	analog signals

a. TP7 and TP8 are optional.

The transition modules greatly simplify the wiring requirements, because commercially available cables can be used in most instance. Most of the cables are either normal BNCs, coaxial LEMOs or flat ribbon cables with a 1:1 wiring. An extended wire plan is listed in Table 13.

Table 13: Wire Plan

	Signal	Connector	From	To
Timing	sampling clock	50 pin ribbon header	Timer	TP5
		BNC	TP5	AA filter
		BNC	TP5	DAC
		BNC	TP5	ADC
LO	CSB, SC, SCSBx	BNC	high frequency synthesizer	Pockels cell, demodulators

Table 13: Wire Plan

	Signal	Connector	From	To
HV	HV1	LEMO	HV supply	6S
	HV2	HV	HV supply	3S
AA Filter	x	50 pin ribbon header	TP1	AA filter
	all	50 pin ribbon header	AA filter	ADC
ZOH Filter	x	32 pin ribbon header	DAC	ZOH filter
	all	32 pin ribbon header	ZOH filter	TP2
Length sensing and control	LSxx	BNC	photodiode	demodulator
		BNC	demodulator	PZT compensation
	control	BNC	PZT compensation	TP1, 3S, 6S
	reference	BNC	TP2	PZT compensation
	relay	BNC	TP4	PZT compensation
	sweep	BNC	TP2	PZT compensation
Wavefront sensing and control	RF	LEMO coaxial	sensor head	demodulator
	DC/gain	15 pin D-sub	sensor head	demodulator
	WSxx	50 pin ribbon header	demodulator	ADC
	gain	BNC	demodulator	TP4
	phase shift	BNC	TP8	demodulator
	angle	BNC	TP2	3S
PS	angle	9 pin D-sub	photodiode head	TP1
	sum	9 pin D-sub	photodiode head	TP1
Beam intensity	difference	9 pin D-sub	photodiode head	TP1
	sum	9 pin D-sub	photodiode head	TP1
	sweep	BNC	analyzer cavity	TP1

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APPENDIX A SETTING UP THE ARGON LASER

A.1 Frequency Stabilization

A description of the optical and electronic layout of the laser frequency stabilization loop can be found in chapter 2.2.1.

To engage the laser frequency stabilization the following steps are required.

1. Turn on the power of the camera monitor, the scope and the high voltage amplifier. Close the iris in front of the RF photodiode which measures the transmitted light.
2. Turn up the gain and adjust the bias of the high voltage amplifier, so that the sweep of the PZT covers a full spectral range. (The cavity modes can be seen on the scope.)
3. Use the steering lens and the steering mirror to minimize the misalignment of the incident beam and the fundamental mode of the reference cavity by looking at the transmitted light on the scope. (To find out which peaks on the scope correspond to which modes in the reference cavity, turn the gain of the high voltage amplifier down, until only one mode is within the range of the PZT sweep. Then use the bias to scan the modes on the scope and watch the corresponding mode patterns on the scope.)
4. Turn the gain of the high voltage amplifier to zero.
5. Open the iris which was closed in step 1.
6. Check the DC voltage of the RF photodiode to be 0.20V (system must be in an unlocked status).
7. Lock the cavity to its fundamental mode by engaging the feedback loop (set the switch on the laser PZT driver module to automatic (Au) and adjust the bias of the high voltage amplifier).

LIGO-DRAFT

APPENDIX B LENGTH CONTROL LAYOUT

B.1 Design and Specifications

The fast PZT compensation network is used to control the spatial position of laser mirrors. Each of the cavities in the FMI has at least two mirrors which can be used to adjust the length of the cavity, one of them is driven by a fast PZT which has a small dynamic range, whereas the other one is driven by a slow PZT which has a large dynamic range. The length misalignment of a cavity is measured with the Pound-Drever scheme. The error signal which serves as an input into the PZT compensation network is directly proportional to spatial misalignment.

The following design considerations and constraints had to be taken into account:

- The bandwidth of the length compensation should be about 20 kHz.
- The control signal has to be divided into a low frequency range and a high frequency range to drive both the slow and the fast PZTs.
- Because the misalignment signals are measured at the dark and the symmetric port of the Michelson interferometer, the misalignment of the two arm cavities is measured as a common and a differential signal.
- The fast PZTs show a sharp resonance ($Q \cong 10$) at about 58 kHz.

The actual compensation network was then realized as follows:

- Each cavity has its own NIM module to control its mirrors.
- Each module has two input channels with individual adjustable gain and sign.
- The control signal of the fast PZT is taken as the error signal of the slow PZT compensation.
- A notch filter was implemented to cancel the PZT resonance.
- The feedback loop is unconditionally stable, in order to avoid troubles arising from the non-linearities in the error signal.

A complete feature list of the PZT compensation network can be found in Table 14.

B.2 Schematics

The schematics for the PZT compensation network are given in Fig. 9 to 15.

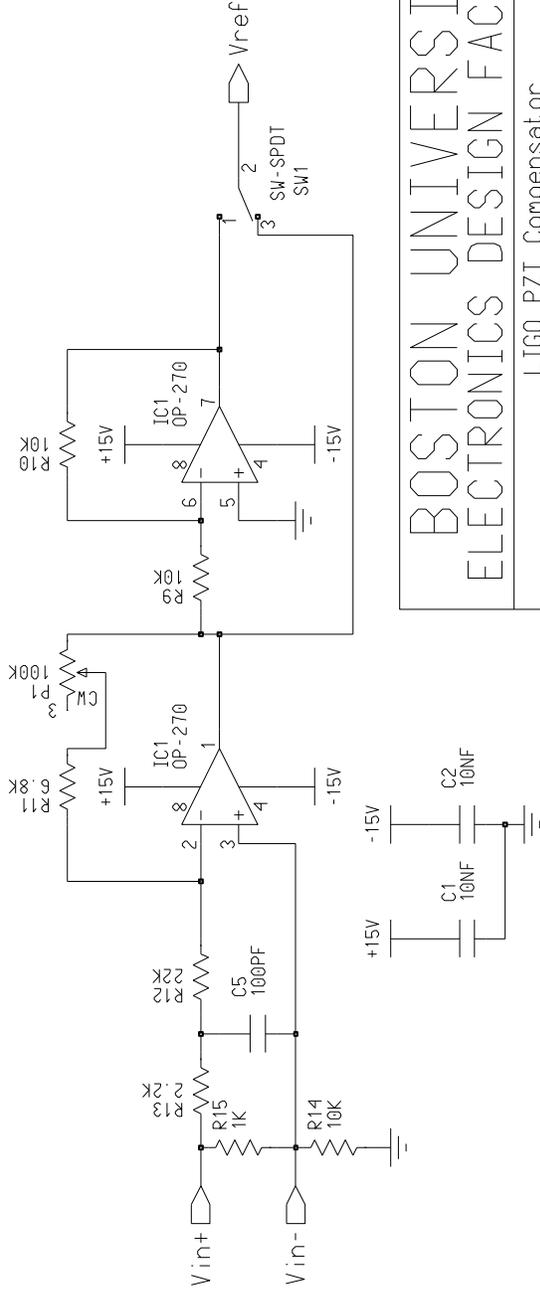
LIGO-DRAFT

Table 14: Features of one PZT Compensation Module

Description	Value
Input channels with adjustable gain and sign	2
Additional reference inputs	1
Output channels with adjustable gain and sign	2 ^a
PZT control input for lock catcher	slow PZT ^b
Poles	10 Hz and 150 kHz
Notch for compensating the PZT resonance	57 kHz (Q=10)
Double poles	48 kHz (Q=1)
Unity gain (fast PZT)	25 kHz
Additional pole for slow PZT compensation	1 Hz
Additional lag compensation (pole/zero)	10 Hz / 5 kHz ^c
Unity gain (slow PZT)	~100 Hz

- a. For driving a slow and a fast PZT.
- b. For the error signal of the slow PZT compensation a relay is used to chose between the PZT control input and the output of the fast PZT compensation.
- c. Modified version only

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14 Aug 95, esh - make input differential
add polarity switch

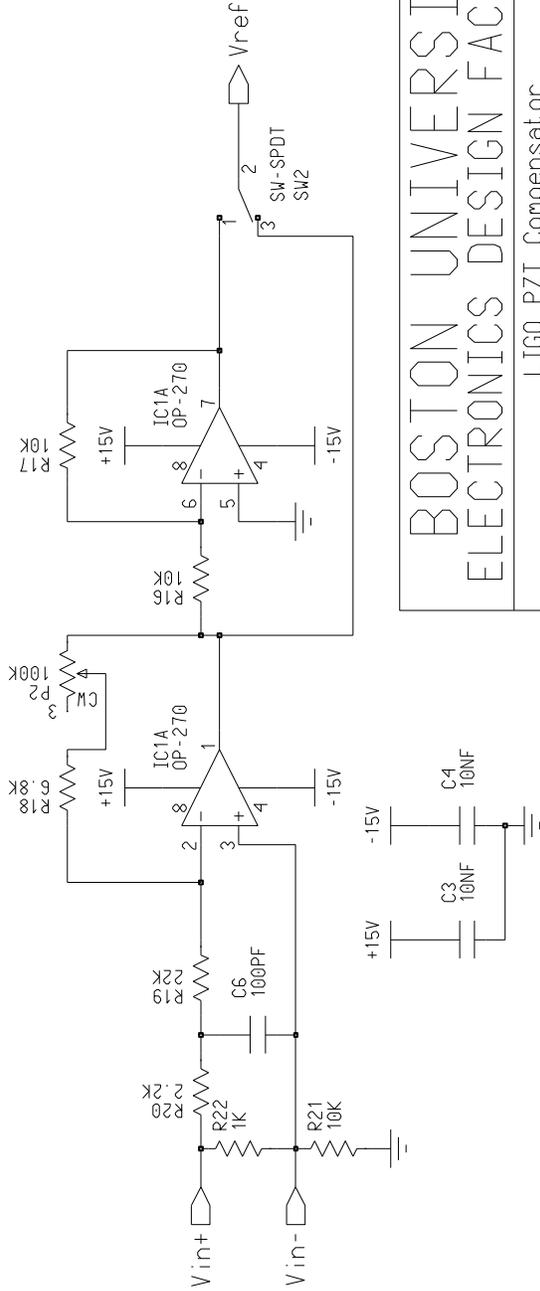
BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

LIGO PZT Compensator
Input channel schematic

DESIGNED BY	D. Sigg	BLOCK	/input
DRAWN BY	E. Hazen	PART NO	XXX-A REV A
SHEET	2 OF 0	PRELIMINARY	ECO'S
DATE	8/10/95	RELEASED	AS BUILT X
PATH	vpcb/er-ic/ligo/pzg_comp/des-ign-lib/input_sheet1		

Figure 10: PZT Compensation Schematics: Input Channel 1

DRAFT

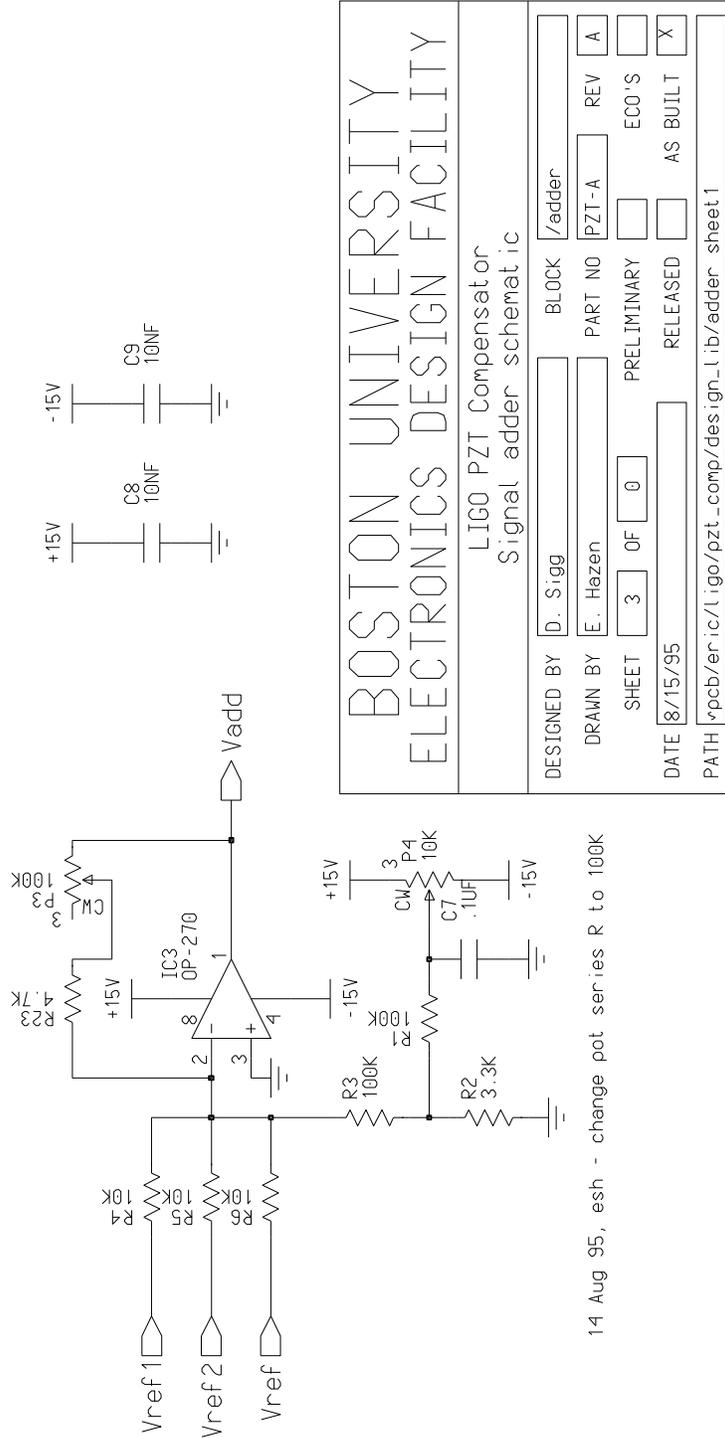


14 Aug 95, esh - make input differential
add polarity switch

BOSTON UNIVERSITY			
ELECTRONICS DESIGN FACILITY			
LIGO PZT Compensator Input channel schematic			
DESIGNED BY	D. Sigg	BLOCK	/input
DRAWN BY	E. Hazen	PART NO	XXX-A
SHEET	2 OF 0	PRELIMINARY	ECO'S
DATE	8/10/95	RELEASED	AS BUILT
PATH		/pcb/er-ic/ligo/pz-comp/des-ign-lib/input-sheet1	

Figure 11: PZT Compensation Schematics: Input Channel 2

NO-DRAFT



14 Aug 95, esh - change pot series R to 100K

BOSTON UNIVERSITY	
ELECTRONICS DESIGN FACILITY	
LIGO PZT Compensator Signal adder schematic ic	
DESIGNED BY	D. Sigg
DRAWN BY	E. Hazen
SHEET	3 OF 0
DATE	8/15/95
PATH	vpcb/er ic/Ligo/pzt_comp/design_lib/adder_sheet.1
BLOCK	/adder
PART NO	PZT-A
PRELIMINARY	<input type="checkbox"/>
RELEASED	<input type="checkbox"/>
ECO'S	<input type="checkbox"/>
AS BUILT	<input checked="" type="checkbox"/>
REV	A

Figure 12: PZT Compensation Schematics: Adder

NO-DRAFT

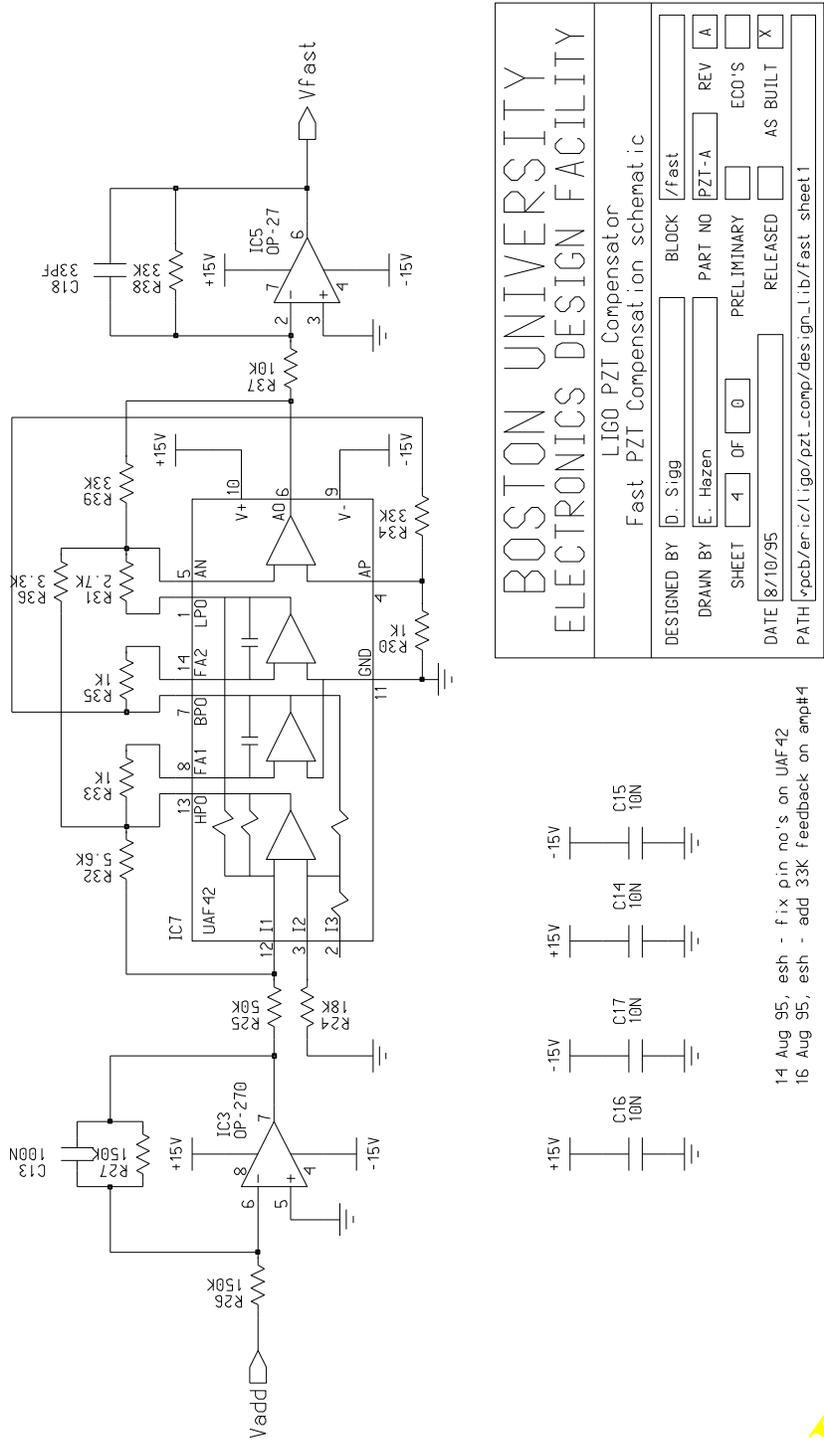


Figure 13: PZT Compensation Schematics: Fast PZT Network

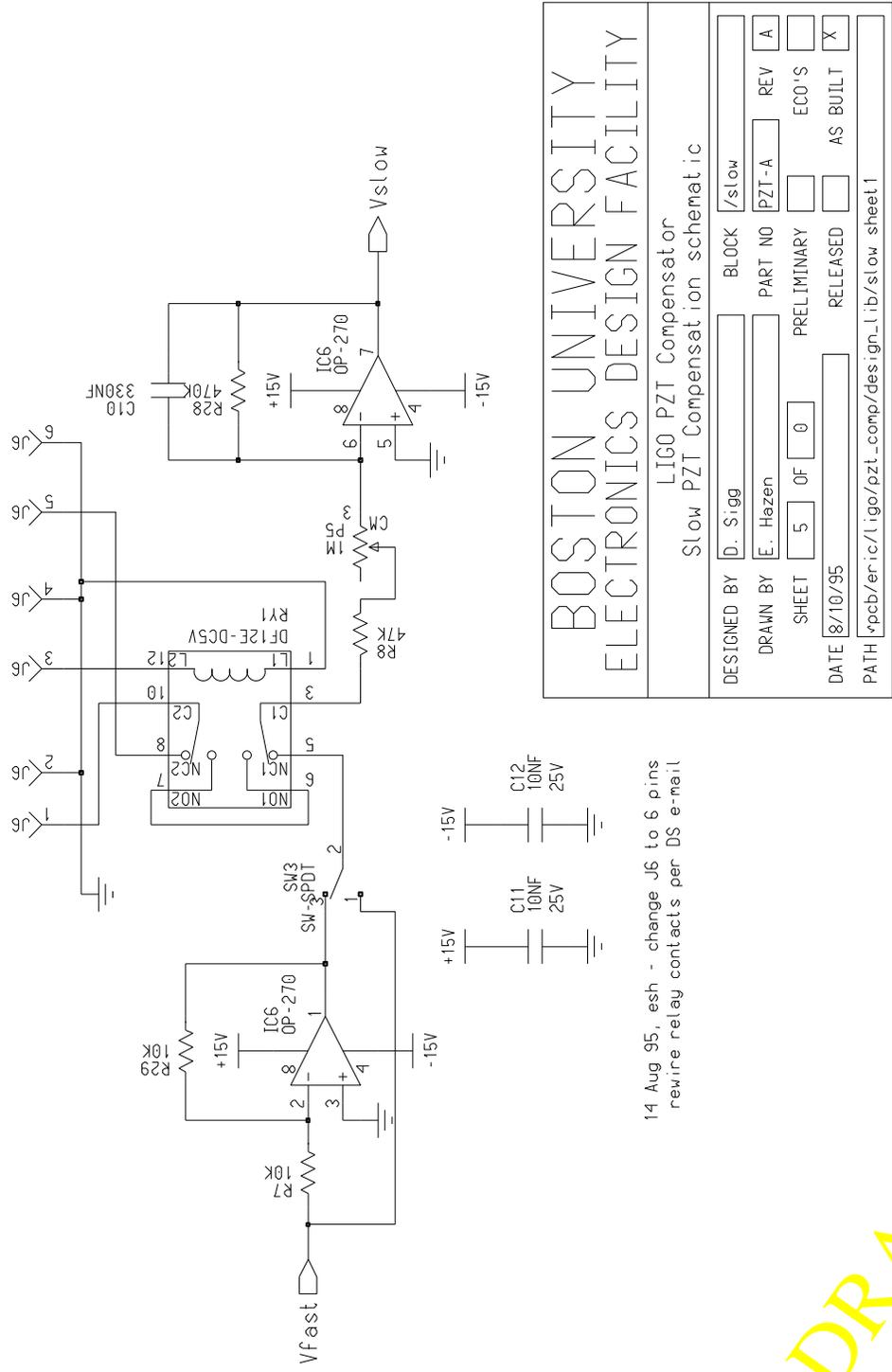
BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

LIGO PZT Compensator
Fast PZT Compensation schematic

DESIGNED BY	D. Sigg	BLOCK	/fast
DRAWN BY	E. Hazen	PART NO	PZT-A
SHEET	4	OF	0
DATE	8/10/95	PRELIMINARY	<input type="checkbox"/>
PATH	/pcb/er.ic/ligo/pzt_comp/des/ign_lib/fast_sheet1		
		RELEASED	<input type="checkbox"/>
		AS BUILT	<input checked="" type="checkbox"/>
		ECO'S	<input type="checkbox"/>
		REV	A

14 Aug 95, esh - fix pin no's on UAF42
16 Aug 95, esh - add 33K feedback on amp#4

LIGO-DRAFT



**BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY**

LIGO PZT Compensation
Slow PZT Compensation schematic

DESIGNED BY	D. Sigg	BLOCK	/slow
DRAWN BY	E. Hazen	PART NO	PZT-A REV A
SHEET	5 OF 0	PRELIMINARY	ECO'S
DATE	8/10/95	RELEASED	AS BUILT X
PATH: \\pcb\er.ic\ligo\pzt_comp\des\ign.lib\slow sheet 1			

14 Aug 95, esh - change J6 to 6 pins
rewire relay contacts per DS e-mail

PRO-DRAFT

Figure 14: PZT Compensation Schematics: Slow PZT Network

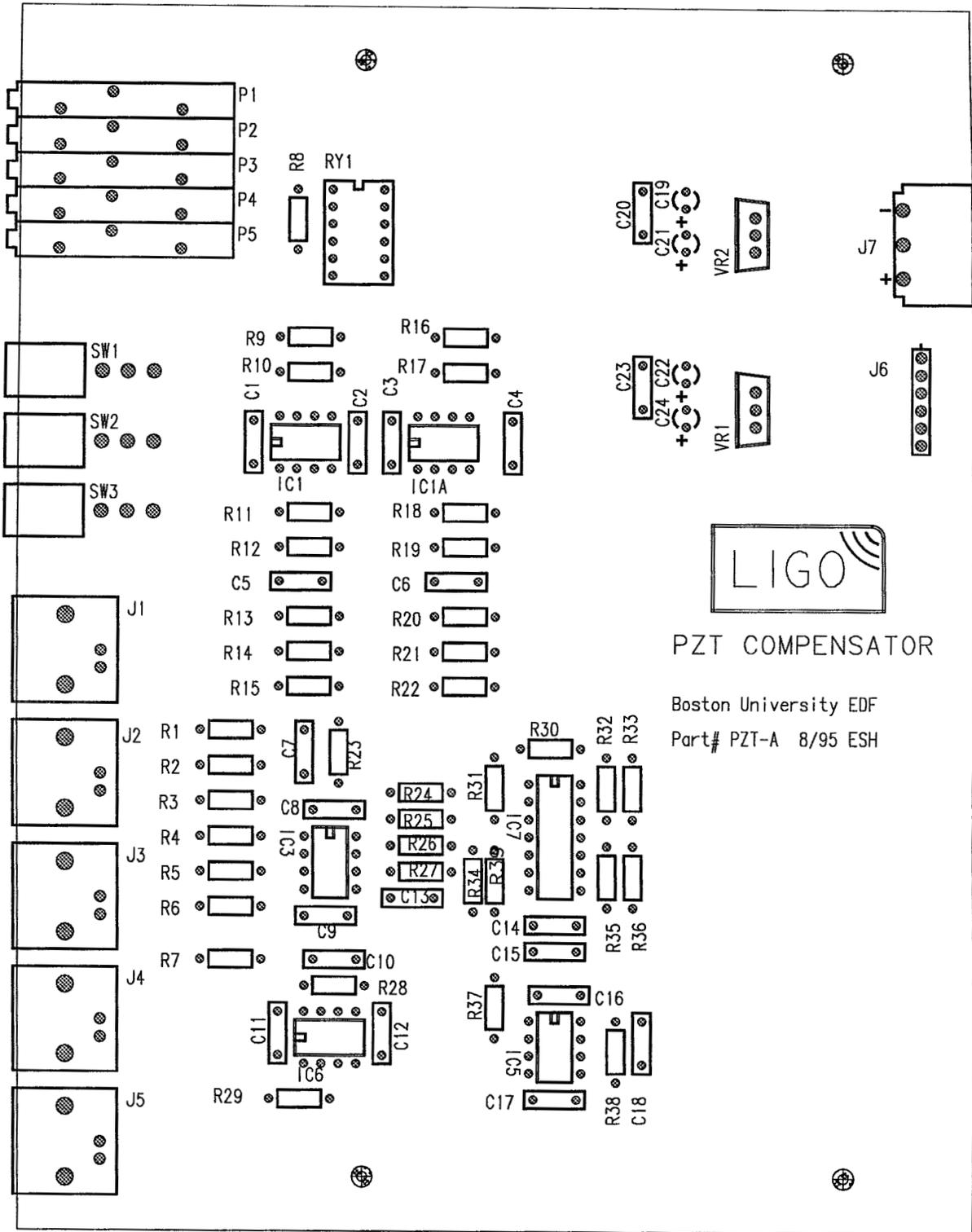


Figure 16: PZT Compensation Schematics: Silkscreen

APPENDIX C WAVEFRONT SENSOR LAYOUT

C.1 Specifications

C.2 PCB Design

One wavefront sensor consists of the pieces: a sensor head and a demodulator board. The main part of the sensor head is a 5-segment photodiode with the corresponding amplifier electronics. The demodulator board has an RF part (see Fig. 17) and a low frequency part. The RF part performs the actual demodulation of the measured light intensity. It is itself divided into two parts: the local oscillator which provides the demodulation clock signals and the mixer part which performs the down-conversion. The low frequency part of the demodulator board is responsible for the control signals to the wavefront sensor head and the measurement of the average DC light intensity.

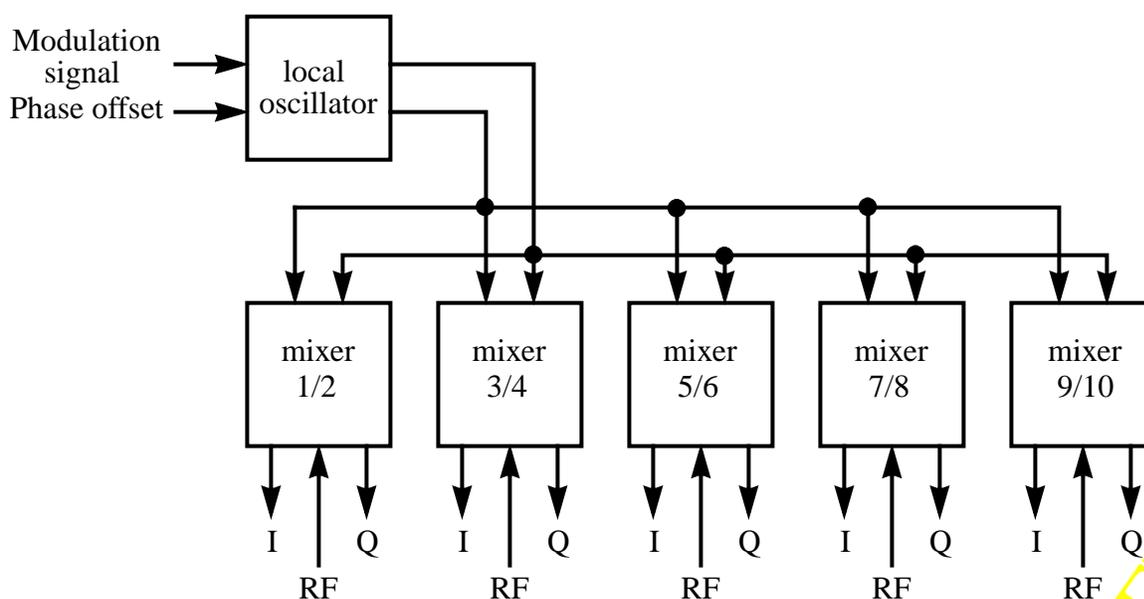


Figure 17: Demodulation (RF) part of the wavefront sensor

C.2.1 Demodulator Board

C.2.1.1 Mixer

For each of the 5 RF signals from the 5-segment photodiode 2 mixers are used (AD831) to demodulate the in-phase and quadrature-phase signal. The RF signal is led directly to the input of

the mixer. The necessary demodulation clock signals are provided by a local oscillator (see next section) which produces 2 master clock signals which are 90° out of phase. The down-converted output signal of the mixer is low-pass filtered (corner frequency at about 300 kHz), before it is fed into the on-chip amplifier which is set to unity gain. The output signal is further amplified and filtered (corner frequency at about 10 kHz to 100 kHz). An optional switched capacitor filter implementing a 5th-order Butterworth (LTC1063) can be used as an anti-aliasing filter, if the signal is digitally sampled.

C.2.1.2 Local Oscillator

The on-board oscillator (VCO) has to provide the required local oscillator signals for the mixers and has to have the capability to adjust its global phase over a range of 360° . The VCO is locked to the modulation signal with a phase locked loop (PLL). The input modulation signal is converted to an ECL signal with an ultra-fast comparator (AD96687). The ECL clock signal is divided by 2 with a D-flip-flop (MC10H131), before it is fed into the phase detector (AD9901). This division doubles the intrinsic phase range of the phase detector to 720° , providing a good linear regime of at least 360° . The error signals due to the phase difference is passed through a passive low pass filter with a corner frequency of 75 kHz and a lag compensation with a pole/zero pair at 0 Hz/7 kHz to the tuning input of a voltage controlled oscillator (Mini-Circuits POS-xx series). The parameters of the PLL open loop transfer function are listed in Table 15. Because the output of the VCO is divided by 4 with two D-flip-flops, before it is fed into the phase detector, the VCO runs at double the frequency of the modulation clock signal. The in-phase (I) clock signal for the mixers is taken from the divided-by-2 signal of the VCO. The quadrature-phase (Q) clock signal is obtained by dividing the inverted VCO signal by 2 with an other D-flip-flop. To cases remain: either the Q signal is 90° ahead of the I signal or 90° behind. To fix this ambiguity in the circuit, a logical NOR operation (MC10H102) is performed from the VCO signal and the inverted divided-by-2 signal of the VCO. The resulting signal is used to either set (90° ahead) or reset (90° behind) the D-flip-flop which is responsible for the Q clock signal. A timing diagram can be found in Fig. 18.

Table 15: Parameters of the PLL Open Loop Transfer Function

Parameter	Value
Double pole	0 Hz
Low pass filter pole	75 kHz
Zero	7 kHz
Unity-gain frequency	10 kHz
Phase Offset (reference input)	1/36 V/ degree

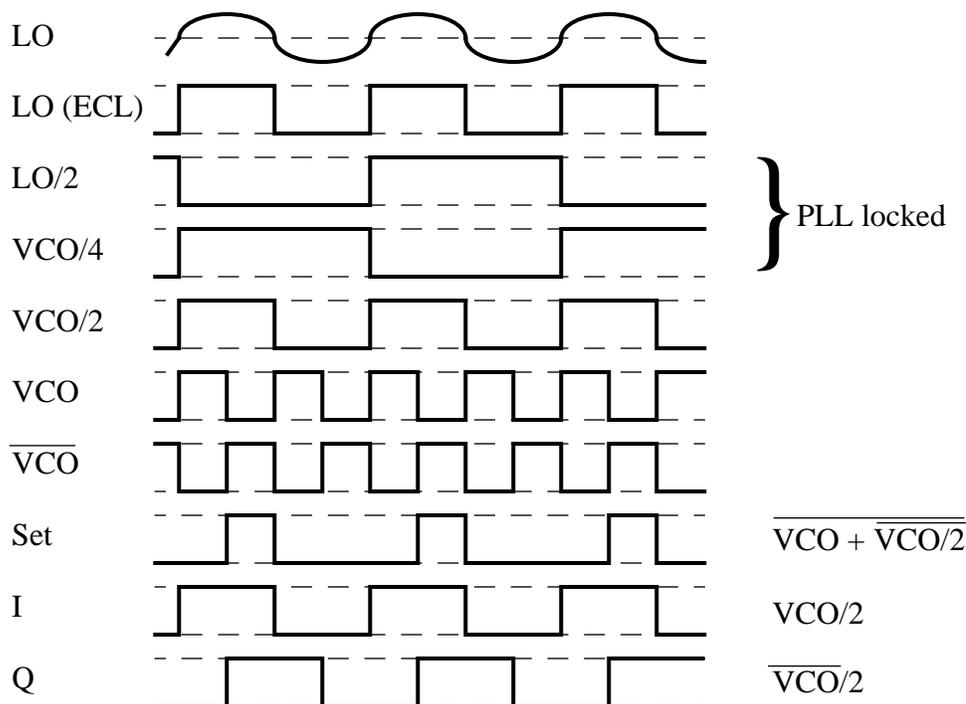


Figure 18: Timing Diagram for the PLL

C.2.2 Sensor Head

Designed and written by William E. Earle, November 22, 1995

This section describes the proposed wavefront sensor electronics as shown on the attached diagram. The earlier design used gain changing in both the RF and diode-current-sensing sections, but with the elimination of gain changing, the design became relatively simple. The three parts of the design are an RF tuning section, an RF amplifier and a diode-current-sensing section.

C.2.2.1 RF Tuning

The fundamental tuned circuit consists of the capacitance of the photodiode D1 resonating with L4. In the diagram, the resonant frequency is given as 20 MHz, but the actual frequency may lie anywhere between 20 and 70 MHz. Diode D1 has a capacitance determined by the bias voltage; for the particular diode used, the capacitance will be about 10 pF with a 40 V bias. This bias is applied through an LC filter consisting of C1, C2 and L1, a filter intended to decouple the bias supply from the RF signal. Since the value of C2 is large compared to the diode capacitance, its value will have little effect upon the resonant frequency. Two other capacitors, C5 and C6, are involved with detecting the dc component of diode current, but they too have large values

compared to the diode capacitance so can also be neglected. From an RF standpoint, the circuit can be treated as a shunt-tuned circuit consisting of the capacitance of D1 in parallel with the inductance of L4. L3-C4 and L2-C3 are two series resonant circuits intended to reduce the second and third harmonics of the fundamental frequency.

At a nominal dc diode current of 0.5 mA, the RF or ac signal current is assumed to have a value of 0.8 μ A rms, or 1.13 μ A peak. This current appears in parallel with the tuned circuit, so the peak voltage is a function of the shunt resistance, which is in turn a function of the circuit Q. If we assume a tuned circuit capacitance of 10 pF and a Q of 10, then at 20 MHz this shunt resistance will be 7958 Ohms, giving a peak signal voltage of 8.99 mV or an rms value of 6.36 mV.

C.2.2.2 Shot and Thermal Noise

A significant amount of shot noise is generated by the dc photodiode current. This noise has an rms value per $\sqrt{\text{Hz}}$ of $I_{\text{shot}} = \sqrt{2QI}$, which at our nominal diode current of 0.5mA is $12.6 \text{ pA}/\sqrt{\text{Hz}}$. There is also some thermal noise from the shunt resistance whose rms value per $\sqrt{\text{Hz}}$ is given by $I_{\text{thermal}} = \sqrt{kT/R}$. For 7958 Ohms, this is $1.44 \text{ pA}/\sqrt{\text{Hz}}$, which is sufficiently small compared to the shot noise that it can be ignored. If we assume a tuned circuit Q of 10 at 20 MHz, then the bandwidth is 2 MHz, so the total shot noise appearing across the tuned circuit will be 141.8 μ V.

C.2.2.3 Tunable Inductors

Three of the inductors shown on the circuit diagram are shown as adjustable. However, since the exact operating frequencies can lie anywhere in the range of 20 to 70 MHz (and two and three times this for harmonics), we need inductors that can be easily modified rather than prewound inductances. This means that we have to wind our own coils as we determine the operating frequencies, so we need coil forms rather than prewound coils.

There are many manufacturers of prewound coils, but relatively few suppliers of bare coil forms. One such manufacturer is Lodestone Pacific from whom I have obtained a sample kit of adjustable coil forms in various sizes. These coil forms are fully shielded, which is an important requirement if we are to minimize coupling between channels, and come in sizes down to 0.3 inches square. The Q's of the coils are generally above 50, and can be optimized by selecting wire and cores according to an application selection guide. If the fundamental tuned circuit should have a Q considerably higher than 10, it may be desirable to reduce it by adding series resistance R1. Although a high Q is desirable from a signal-to-noise standpoint, it also increases the sensitivity of phase change to frequency shift, an undesirable effect.

The Lodestone coil forms that seem reasonable for this application are

- L31-6-CT-B-4. Used for 2.0 to 30MHz.
- L31-10-CT-B-4. Used for 10 to 100MHz.
- L31-17-CT-B-4. Used for 20 to 200MHz.

These forms are 0.3 inch square and use very small removable bobbins. A removable bobbin is desirable because this makes it possible to change an inductance value without having to remove the complete coil form from the PC board.

It should be noted that these are very small coil assemblies that will require patience and care for proper assembly.

These coil forms are quite inexpensive, in the vicinity of \$1 each.

C.2.2.4 The RF Amplifier

Assuming a maximum full-scale output of 10 dBm into 50 Ohms, we get a maximum voltage output of 1.0 V peak. However, since there is to be an overrange of 30 dB, which is a factor of 31.6, we end up needing a 31.6 mV peak signal under normal operating conditions. Since our nominal signal from the tuned circuit is 8.99 mV peak, determined previously, the output amplifier needs a voltage gain of $31.6/8.99=3.52$. It is customary practice when using an op-amp to drive a 50 Ohm line to use a series resistance of 50 Ohms, and if we do this we actually need a gain of $2 \times 3.52 = 7.04$. This is sufficiently close to the minimum gain of 10 for a low-noise CLC425 amplifier, that we might as well just use a gain of 10 rather than the calculated 7.04.

C.2.2.5 Amplifier Noise

The CLC425 has a voltage noise component, a current noise component and a thermal noise component from the amplifier feedback resistor. The CLC425 is specified to have a voltage noise of 1.05×10^{-9} V per \sqrt{Hz} and a current noise of 1.6×10^{-12} A per \sqrt{Hz} .

At a gain of 10, the CLC425 has a bandwidth of 170 MHz, so the total voltage noise at its input will be 13.7 mV. The current noise flows through the tuned circuit shunt resistance of 7958 Ohms, so it sees a bandwidth of only 2 MHz. Thus the voltage at the amplifier input due to the current noise will be 18.0 mV. The thermal noise due to the feedback resistor network of 90 Ohms is 15.9 mV using a 170 MHz bandwidth. Adding the three noise sources gives an amplifier input noise of 27.6 mV. Note that the shot noise calculated previously was 141.8 mV, so the amplifier noise is a negligible part of the total noise. Using the previously determined signal level of 6.36 mV, then the signal-to-noise ratio is 33 dB. Of course, the use of a narrower output bandwidth will increase this value.

C.2.2.6 Diode Current Measurement

The dc component of the diode current is sensed by a transconductance amplifier whose negative input terminal is held at virtual ground potential. Thus, the current sensing does not introduce any offset voltage that would change the diode bias and circuit tuning and RF phase. Of course, for this approach to work, the amplifier must be stable with the relatively large capacitive load, C5, that is needed to provide a low impedance path for the RF current flowing through L4.

Some amplifiers are designed to be stable with capacitance up to 1000 pF, but few can stand higher capacitive loads. Fortunately, there is at least one amplifier, the AD847 (and its dual version, the AD827) that is stable with any capacitive load. This amplifier also has a low offset voltage, a low offset current and a 35 MHz bandwidth. (It is also readily available and not merely a data sheet.) It does have a limited gain of about 3500, though, so should not be used without considerable feedback to maintain gain stability.

Capacitor C6 serves the two functions of providing a relatively low impedance RF path (for the same reason as C5) and in combination with R5 setting the bandwidth of the current-sensing circuit. Unfortunately, maintaining a reasonable bandwidth with a large value for C6 means a low value of R5, but this reduces the gain and increases the effect of the error from the amplifier offset voltage. With the compromise values shown on the diagram, the bandwidth is 48 kHz and the output is 1.66 V for a 0.5 mA diode current. The maximum amplifier offset voltage is 2 mV, but

the typical is only 0.5 mV, so the error is of the order of 0.1% or less. The maximum offset current error is 300 nA with a typical value of 50 nA. Using the maximum value, a 1.0 mV error would occur, less than 0.1% of the full-scale signal.

A second stage of amplification with a gain of 3 brings the final output to 5 V for a diode current of 0.5 mA. This stage includes a 160 kHz lowpass network to remove any remaining traces of the RF signal without affecting the 48 kHz bandwidth. The current offset error from this second amplifier is negligible but the voltage offset error will be the same as for the input stage. This means that the total error could exceed 0.1%, but typically this won't be the case.

Another approach using a composite amplifier consisting of a very low offset, narrow bandwidth amplifier combined with a wider bandwidth amplifier was considered, but the increase in circuit complexity did not seem worthwhile. If an error of 0.1% or so is acceptable, then I prefer the suggested approach; if we really need a smaller error, then we need to consider a more complicated circuit.

C.2.2.7 Power Supplies

It seems reasonable to use supplies of ± 12 V and on-board regulators to provide the ± 5 V needed by the CLC425's. In order for the AD827's to provide a +5 V output, these amplifiers can use the unregulated +12 V supply.

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C.3 Schematics

C.3.1 Demodulator Board

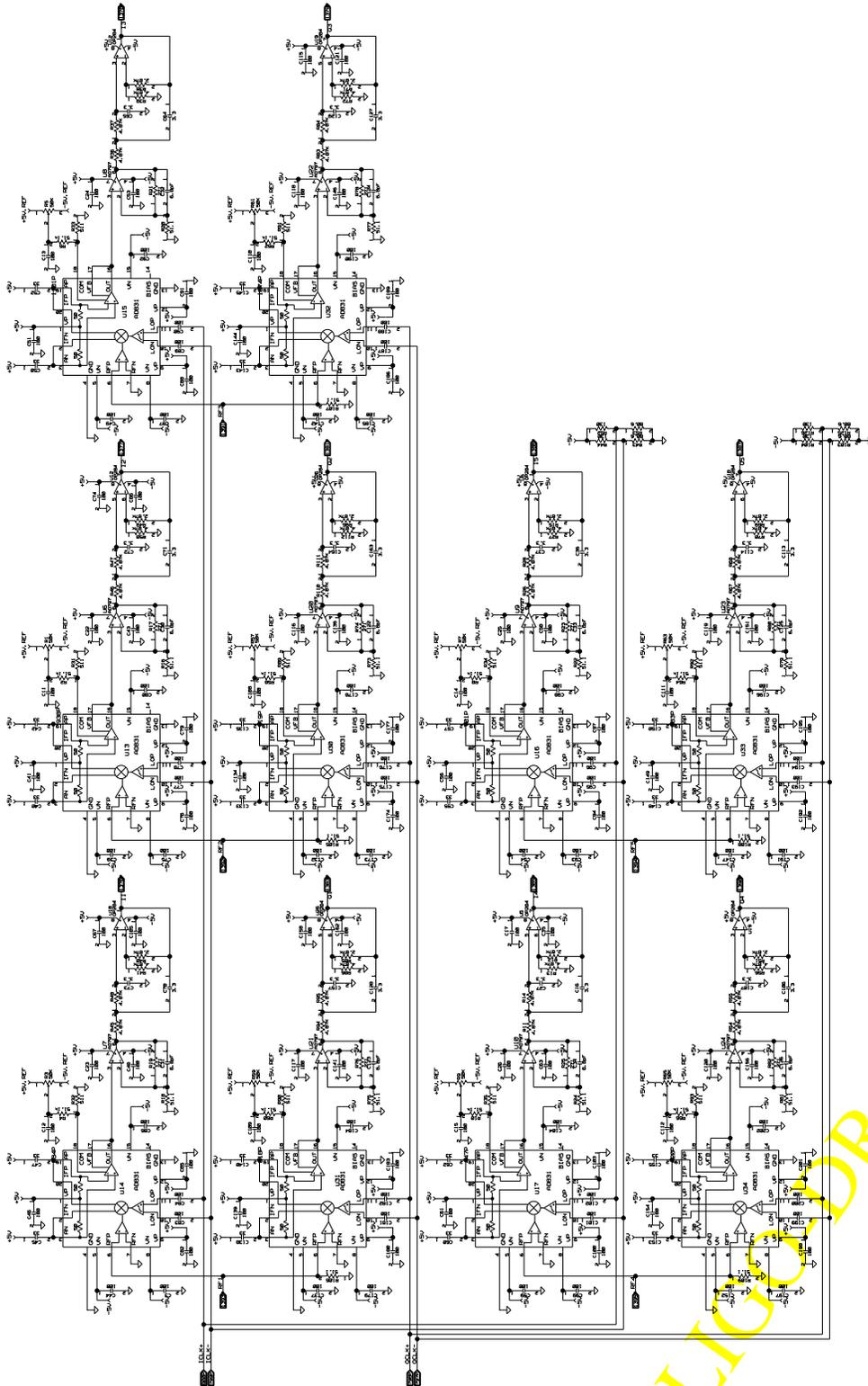


Figure 19: Wavefront sensor demodulator: Mixer

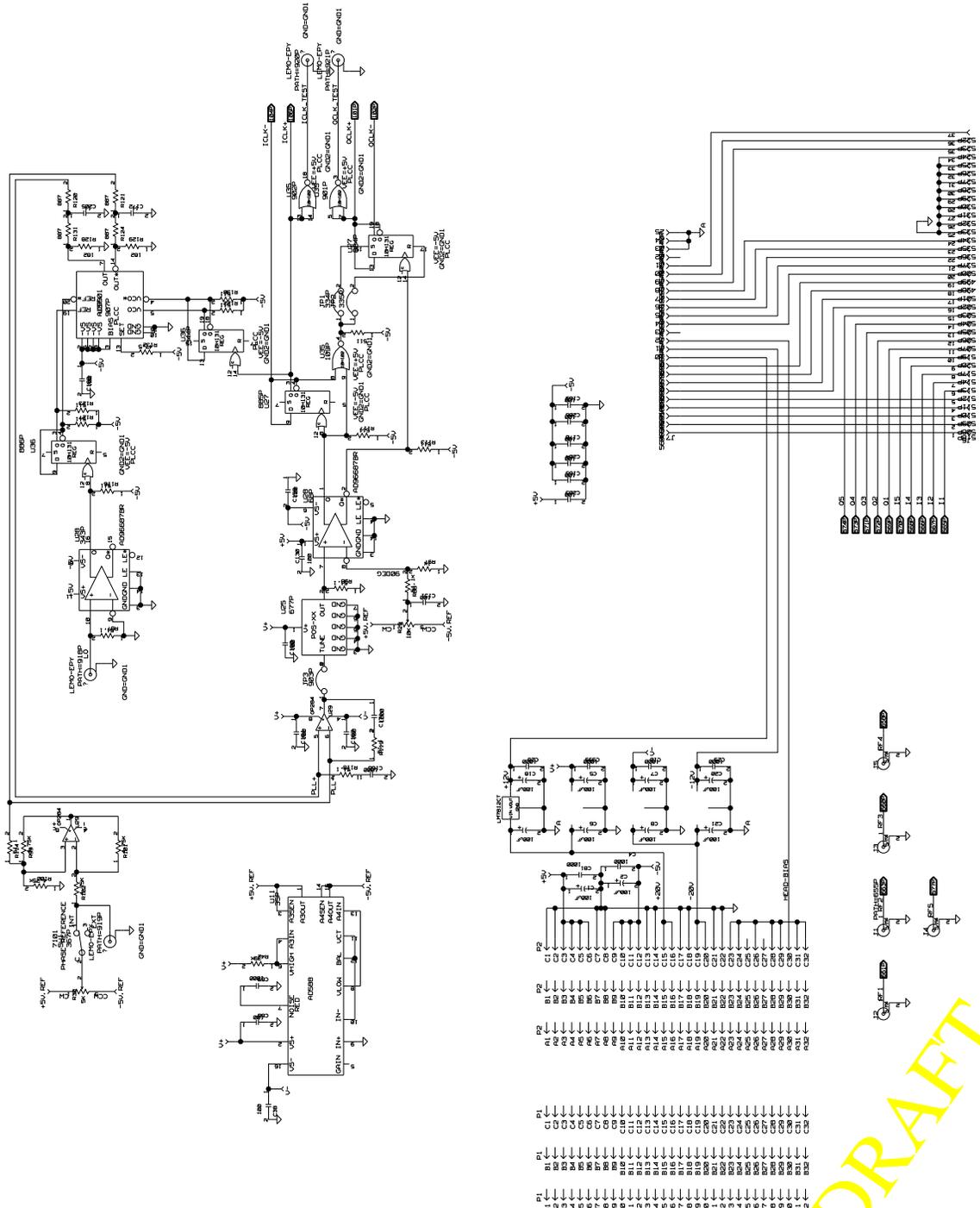
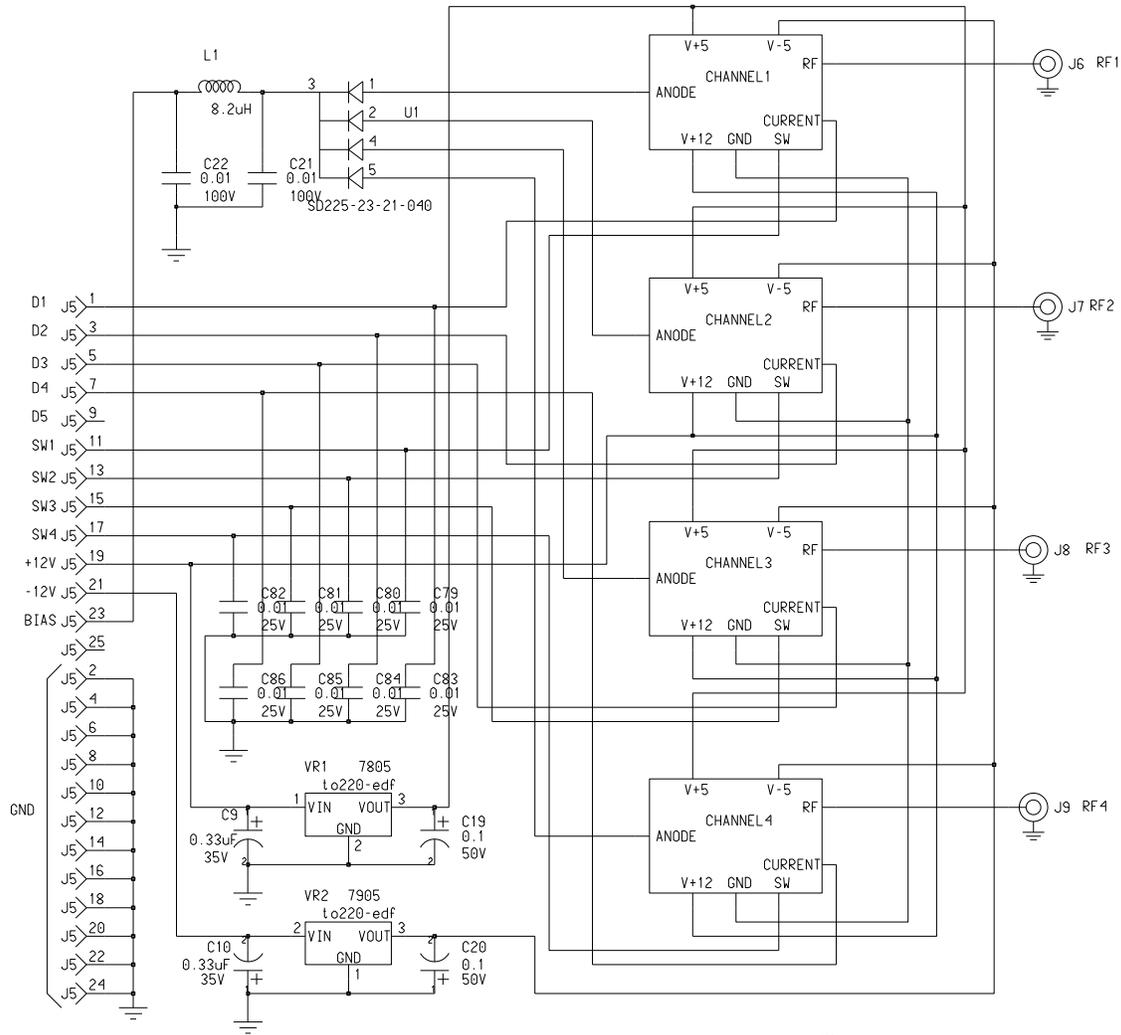


Figure 20: Wavefront sensor demodulator: VCO

C.3.2 Sensor Head



BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

LIGO Wavefront Sensor

DESIGNED BY	W. E. Earle	BLOCK	/AAA/BBB/CCC
DRAWN BY	W. E. Earle	PART NO	XXX-A REV A
SHEET	1 OF 1	PRELIMINARY	<input type="checkbox"/> Y <input type="checkbox"/> N
DATE	12/18/95	RELEASED	<input type="checkbox"/> N <input type="checkbox"/> AS BUILT <input type="checkbox"/> N
PATH /bill/wavefront			

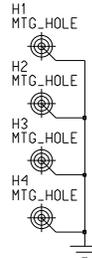


Figure 21: Wavefront sensor head: Overview



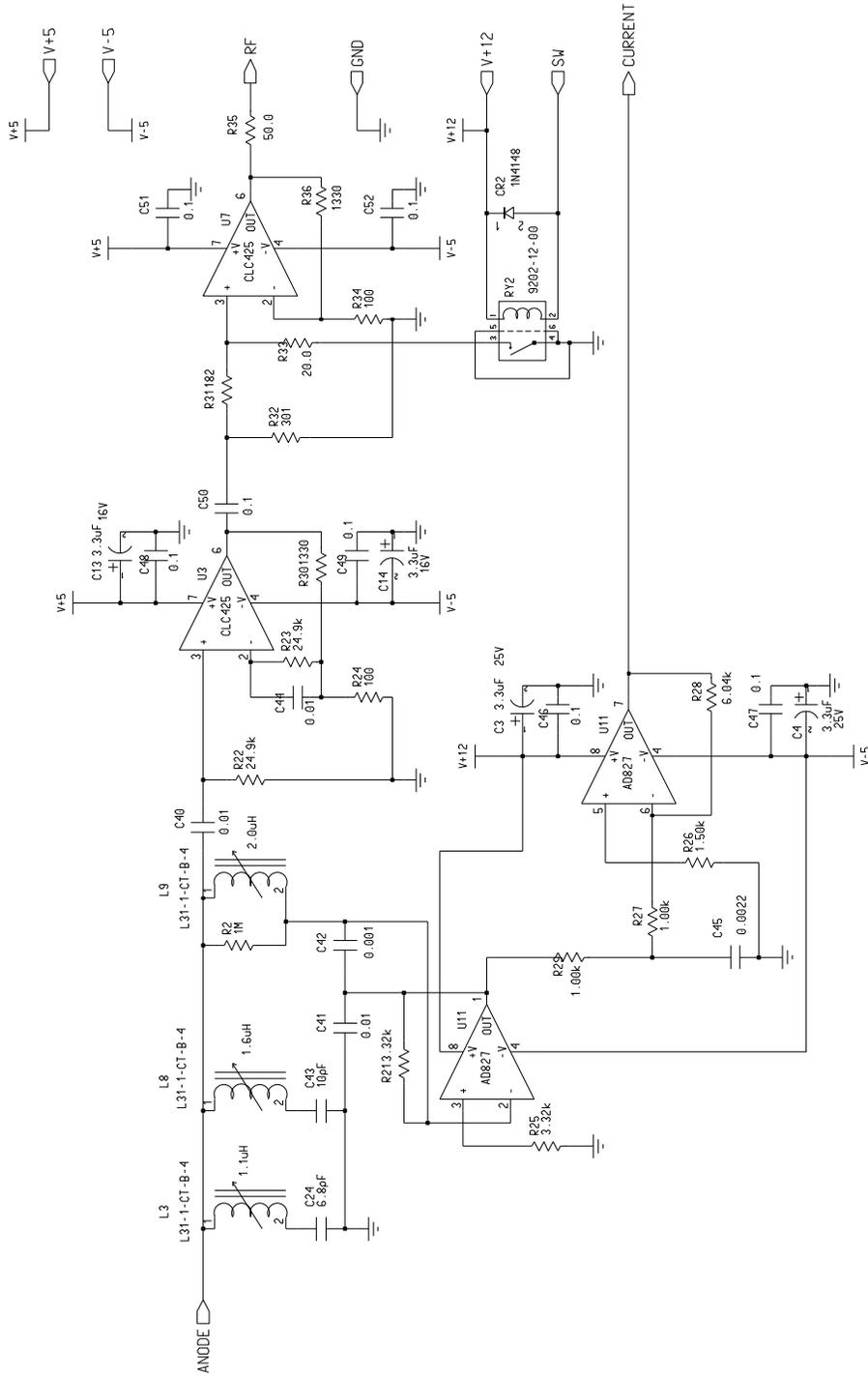


Figure 23: Wavefront sensor head: Channel 2



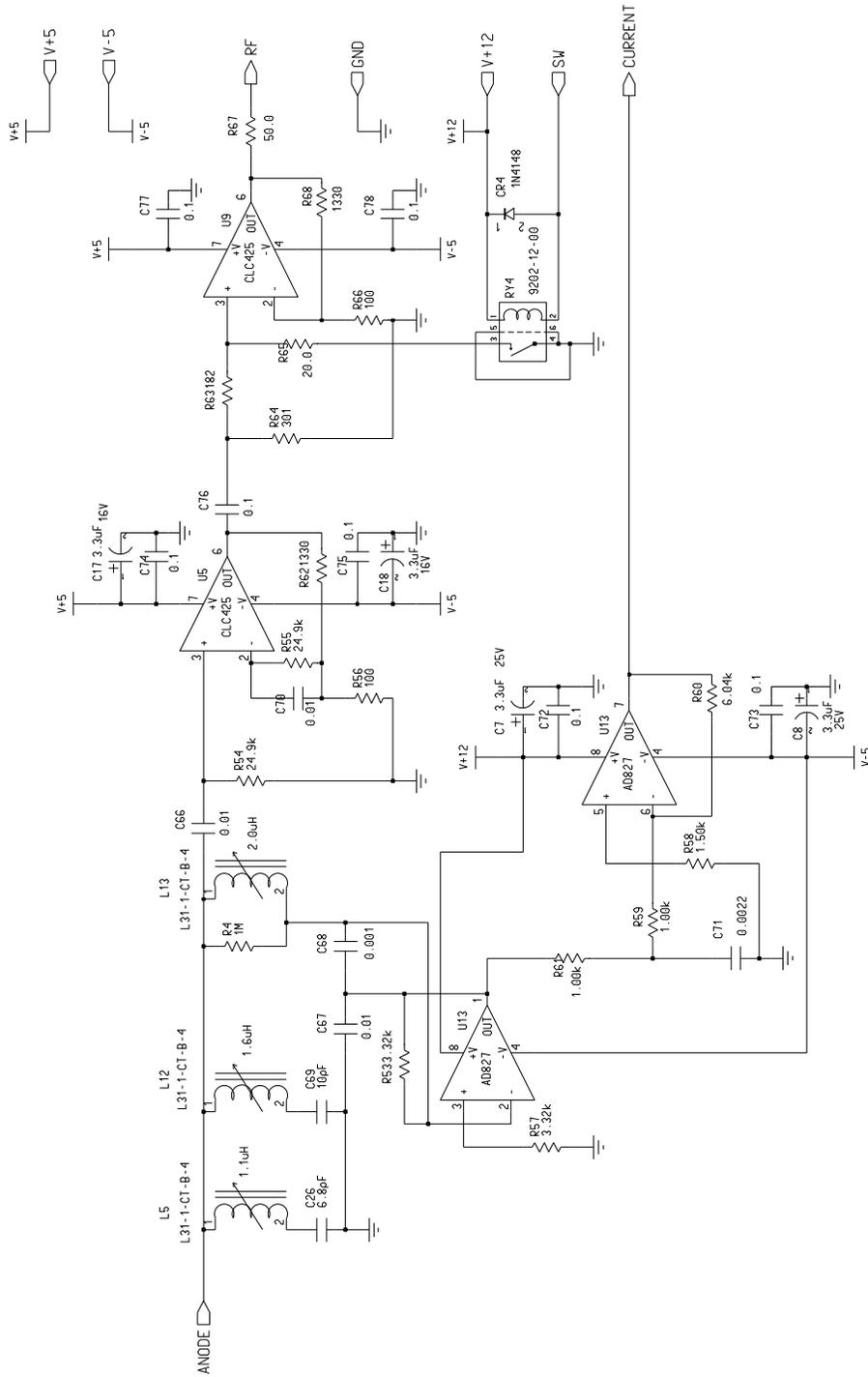


Figure 25: Wavefront sensor head: Channel 4

LIGO

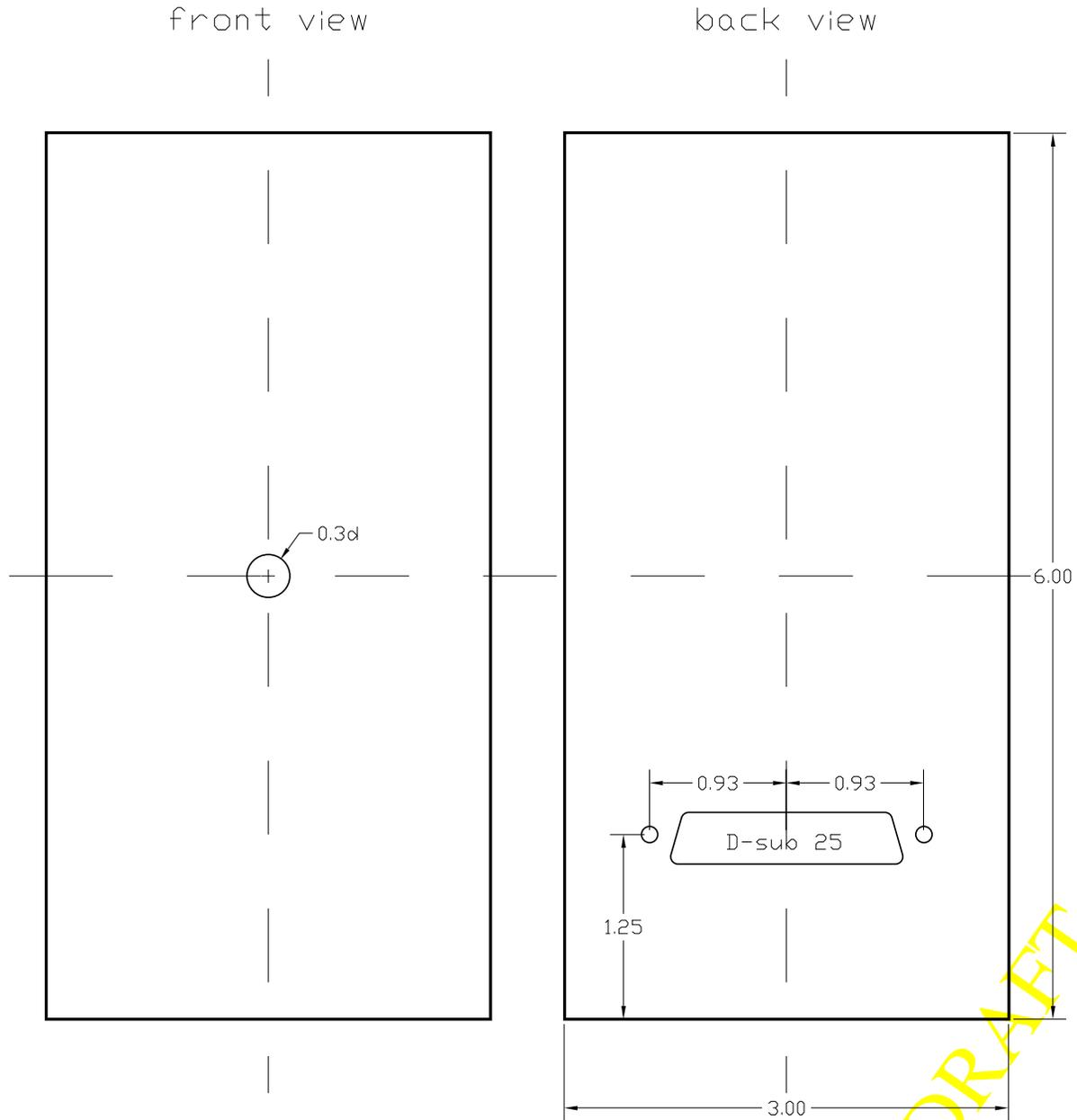
C.4 Board Layout

C.4.1 Demulator Board

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C.5 Enclosure

Wavefront Sensor Head Enclosure

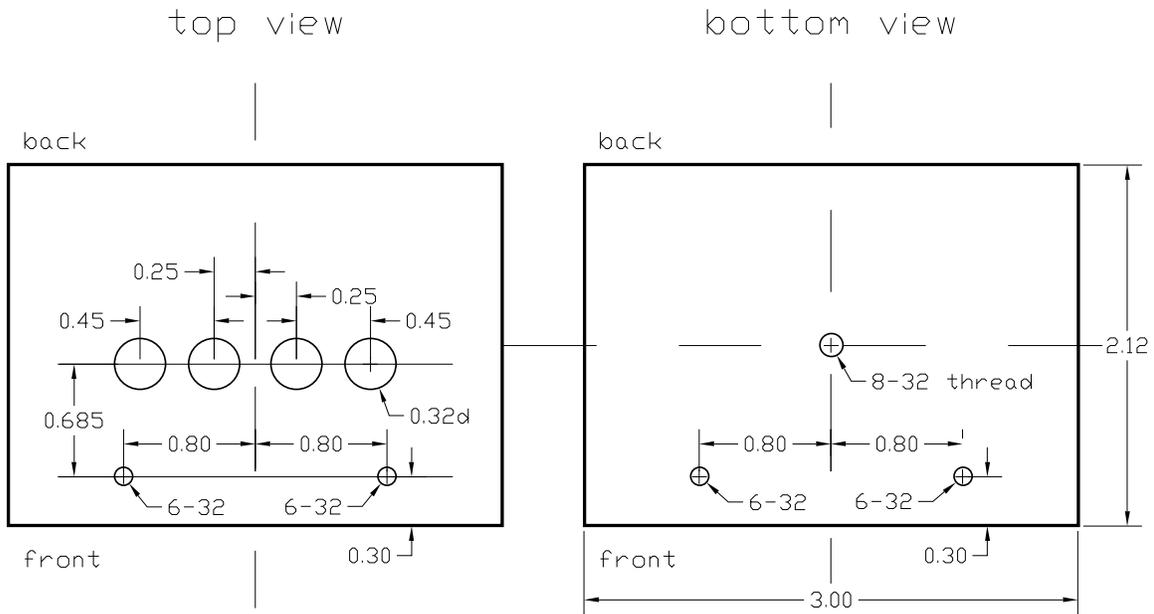


0.3 diameter hole is a thru hole
 D-sub 25 is an open hole for a 25 pin D-sub socket
 Units are in inch; all tolerances are +/- 0.005

Figure 27: Wavefront sensor head: Enclosure front and back view

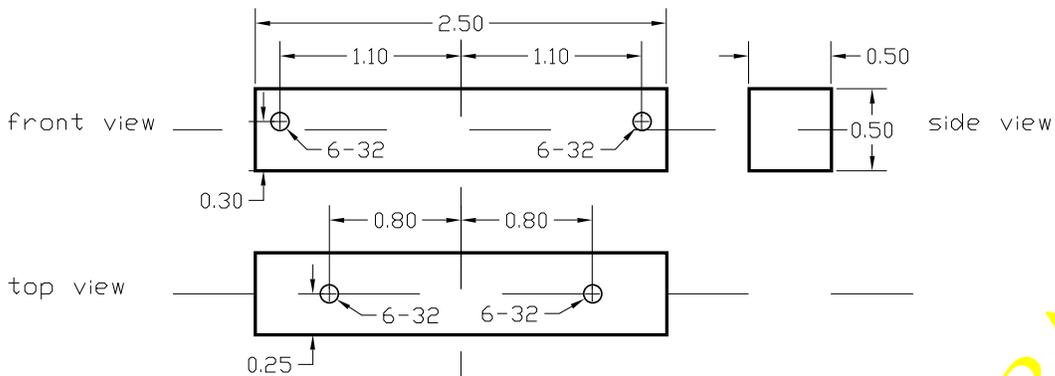
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Wavefront Sensor Head Enclosure



6-32 screw thru holes are counter sunk
 0.32 diameter holes are connector thru holes
 8-32 screw hole is threaded
 Units are in inch; all tolerances are +/- 0.005

Mounting Bars



6-32 screw holes are threaded
 Units are in inch; all tolerances are +/- 0.005

Figure 28: Wavefront sensor head: Enclosure top and bottom view

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APPENDIX D 32.33 MHZ OSCILLATOR

D.1 Design and Specification

The second sideband of the subcarrier does not enter the recycling cavity of the FMI experiment. Hence, no fine-tuning of the frequency will ever be required. A quartz oscillator with a fixed frequency of 32.33 MHz was chosen to provide the necessary RF signal for the Pockels cell and the demodulator. Since the output power of the used quartz oscillator (HSO-100) is only +4 dBm, an additional RF gain stage was implemented to boost the signal level to +13 dBm. A 30 MHz low pass filter at the RF output suppresses harmonics below 70 dBc.

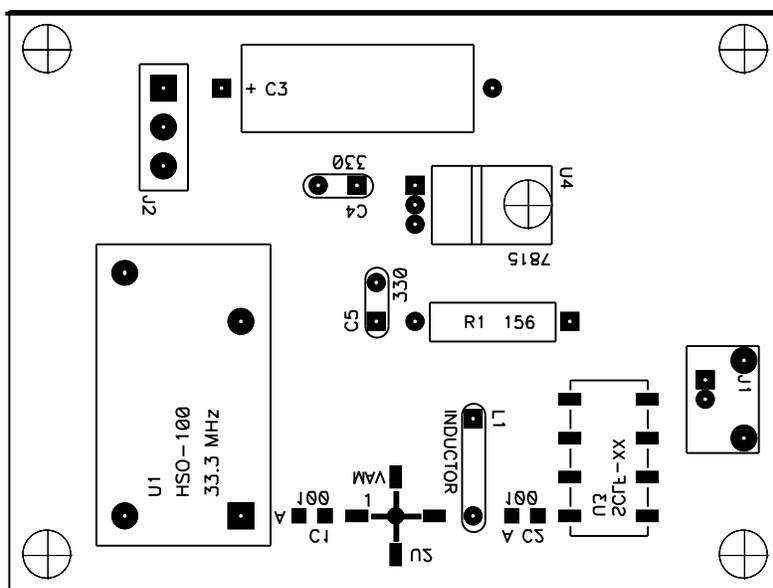


Figure 29: 32.33 MHz Oscillator Board Layout

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D.2 Schematics

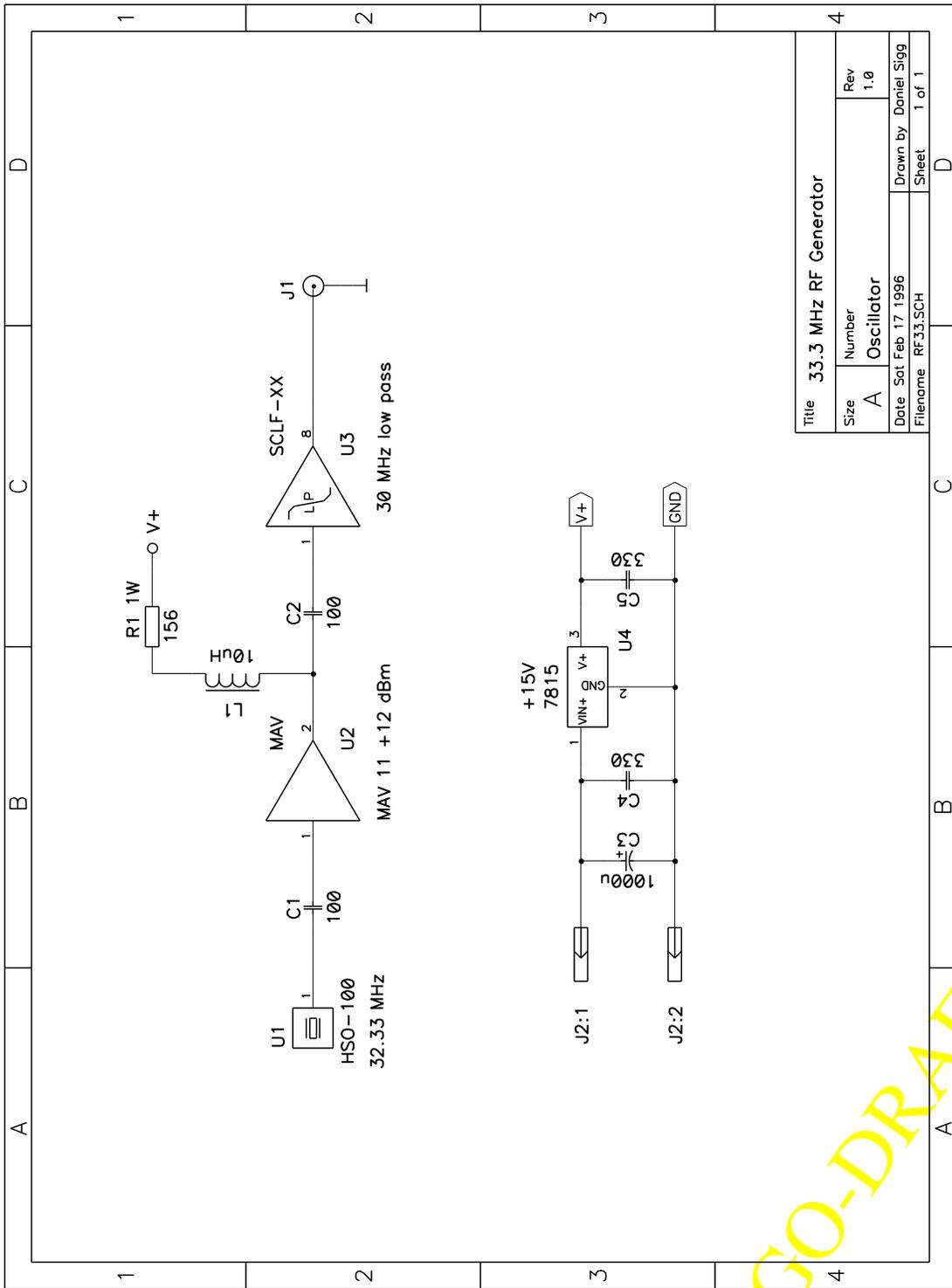


Figure 30: 32.33 MHz Oscillator

APPENDIX E ANGULAR COMPENSATION NETWORK

E.1 Design and Specification

E.2 Implementation

APPENDIX F FILTER BOARDS

F.1 Design and Specification

F.2 Schematics

APPENDIX G GLOSSARY

TBD.

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