LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

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LASTI Noise Prototype Electronics and Controls Quick Start Guide		
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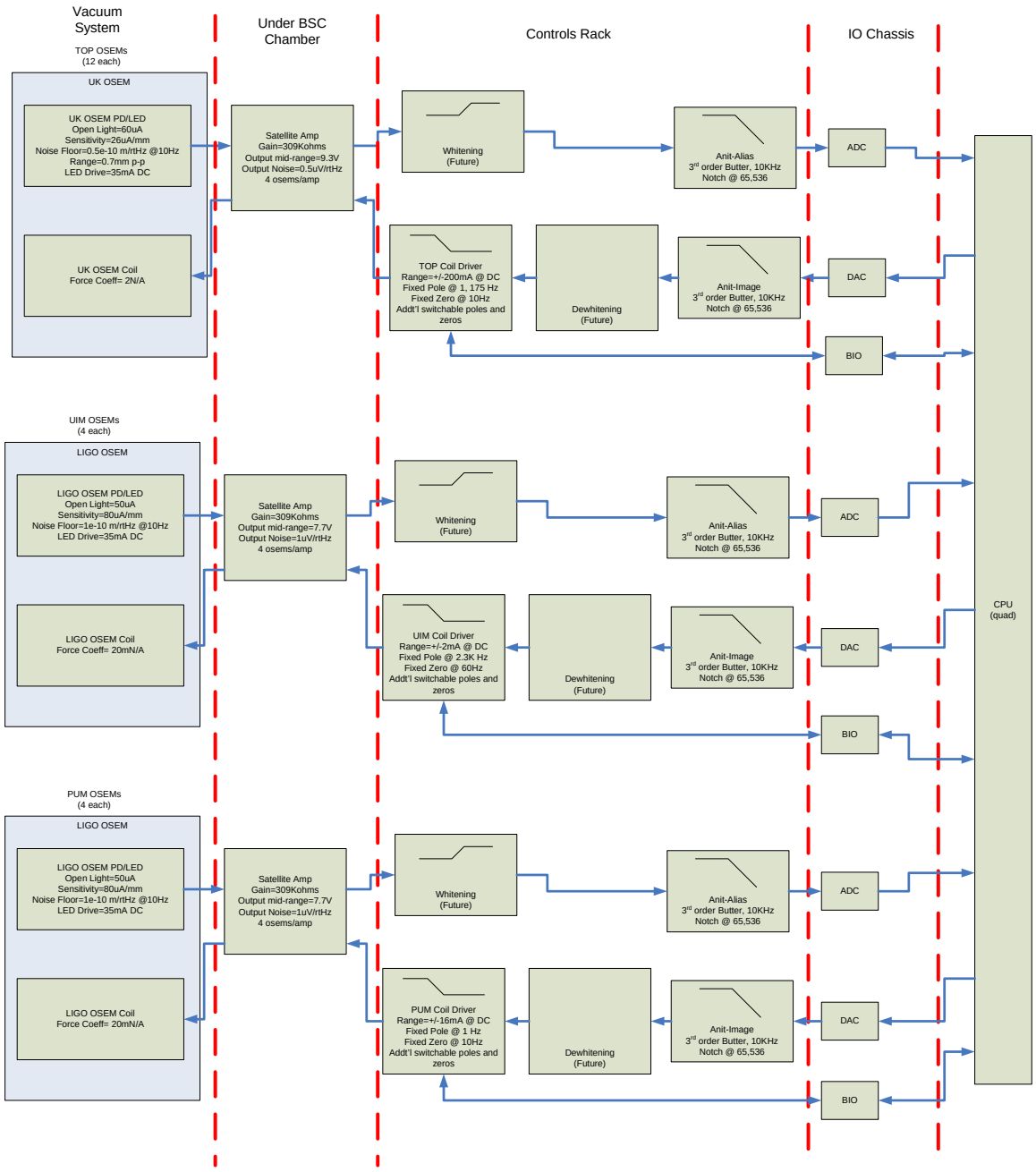
1 Introduction

This quick start guide is meant to as a quick reference and guide to the LASTI Noise Prototype electronics hardware and software. Detailed descriptions and documentation for each of the individual modules can be found in the schematics and test procedures for those components.

The figure below is a basic block and signal flow diagram for the installed system.

LASTI Noise Prototype Signal Flow



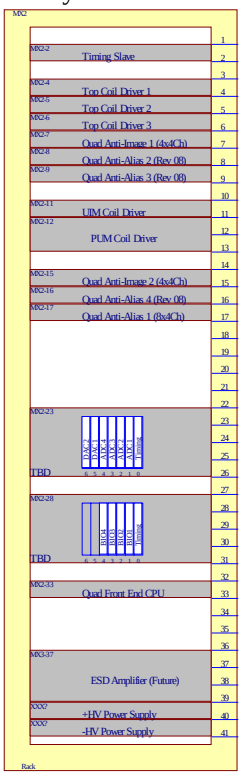
Each of the components is described in the sections below.

2 Electronics Hardware

2.1 System Wiring Diagram and Rack layout

The system wiring diagram can be found in the LIGO DCC or at:
http://www.ligo.caltech.edu/~jay/drawings/D080180-00-C.pdf

The figure below shows the rack layout for the system.



2.2 UK Satellite Amplifier

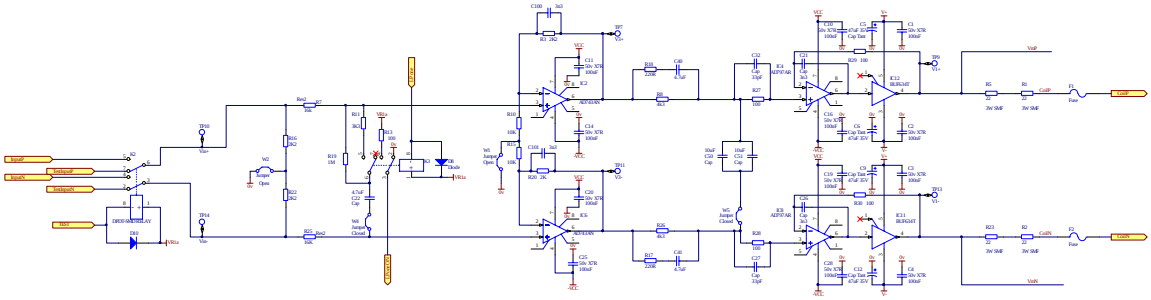
The satellite amplifier provides two main functions in the system:

- Constant 35 mA bias current for the OSEM LEDs.
- Gain stage for the OSEM photodiode. The gain of the stage is 309 Kohms.

The coil driver signals from the coil driver to the OSEM coils only pass through the satellite amplifier. As can be seen from the figure above, the satellite amplifiers are located on a small wire shelf under the BSC chamber.

2.3 UK TOP Coil Driver

The figure below shows the schematic for a single channel of the UK Top Coil Driver module.

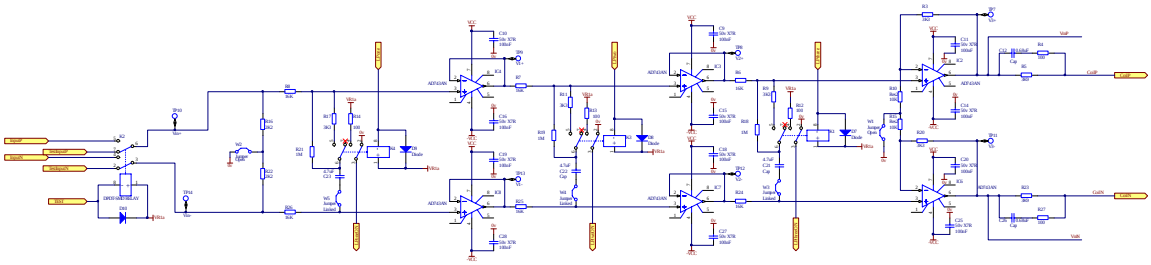


The nominal response of the circuit without relay K3 energized has poles at 1 Hz and 175 Hz and a zero at 10Hz. When relay K3 is energized, an additional 1Hz pole and 10Hz zero are added to response. Relay K2 is used to connect the circuit input to the chassis test input connector (K2 de-energized) or the control input from the Anti-Image chassis (K2 energized).

The second set of contacts on relay K3 are used as a positive indication of the state of relay K3. A low indicates K3 not energized and a high indicates K3 energized. This signal is connected to a binary input in the control system.

2.4 UK UIM Coil Driver

The figure below shows the schematic for a single channel of the UK UIM Coil Driver module.

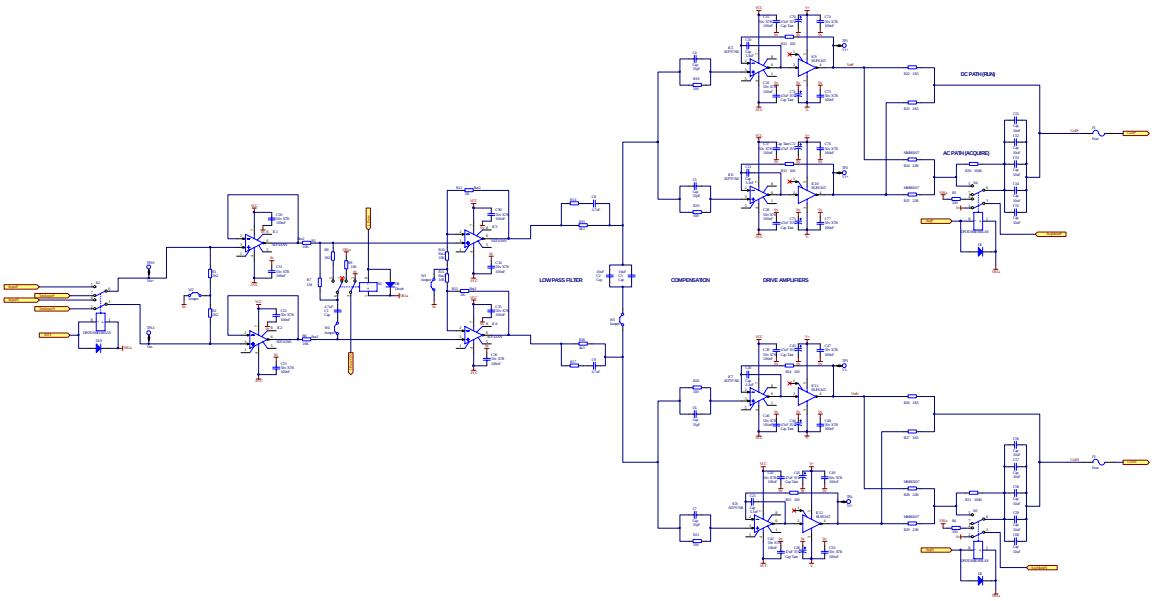


The nominal response of the circuit without relays K1, K3 and K4 energized is a zero at 60 Hz and a pole at 2.3 KHz. Each of these relays (K1, K3, K4) when energized adds an additional pole at 1Hz and zero at 10Hz to the response. Relay K2 is used to connect the circuit input to the chassis test input connector (K2 de-energized) or the control input from the Anti-Image chassis (K2 energized).

The second set of contacts on relays K1, K3 and K4 are used as a positive indication of the state of the relays. A low indicates that the relay is not energized and a high indicates relay energized. These signals are connected to binary inputs in the control system.

2.5 UK PUM Coil Driver

The figure below shows the schematic for a single channel of the UK UIM Coil Driver module.



The nominal response of the circuit without relays K3, K4 and K5 energized is a pole at 1 Hz and a zero at 10 Hz. When relay K3 is energized an additional pole at 1 Hz and zero at 10 Hz are added to the response. Relays K4 and K5 are used to implement the acquire mode for the channel. These relays (K4 and K5) should be operated as a pair. When they are energized a zero at 2Hz and 145 Hz pole are added to the channel response. Relay K2 is used to connect the circuit input to the chassis test input connector (K2 de-energized) or the control input from the Anti-Image chassis (K2 energized).

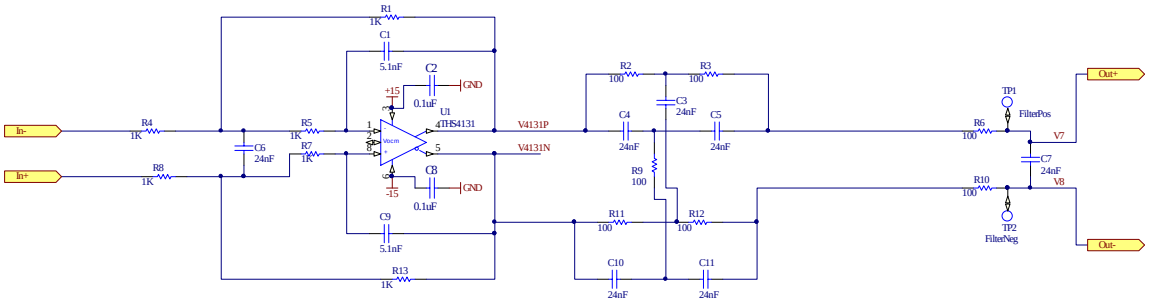
The second set of contacts on relays K3, K4 and K5 are used as a positive indication of the state of the relays. A low indicates that the relay is not energized and a high indicates relay energized. These signals are connected to binary inputs in the control system.

It should be noted that there is a design flaw in the installed version of the PUM Driver that will be corrected in future versions. The flaw is in the design of the low pass filter stage prior to the differential driver stage. The design, as implemented, only works for small signal amplitudes as the large capacitors C8, C2, C3, C9 present a very low impedance that the op amps (IC3 and IC4) can not drive at frequencies much above a few hertz.

2.6 Anti-Alias and Anti-Image Chassis

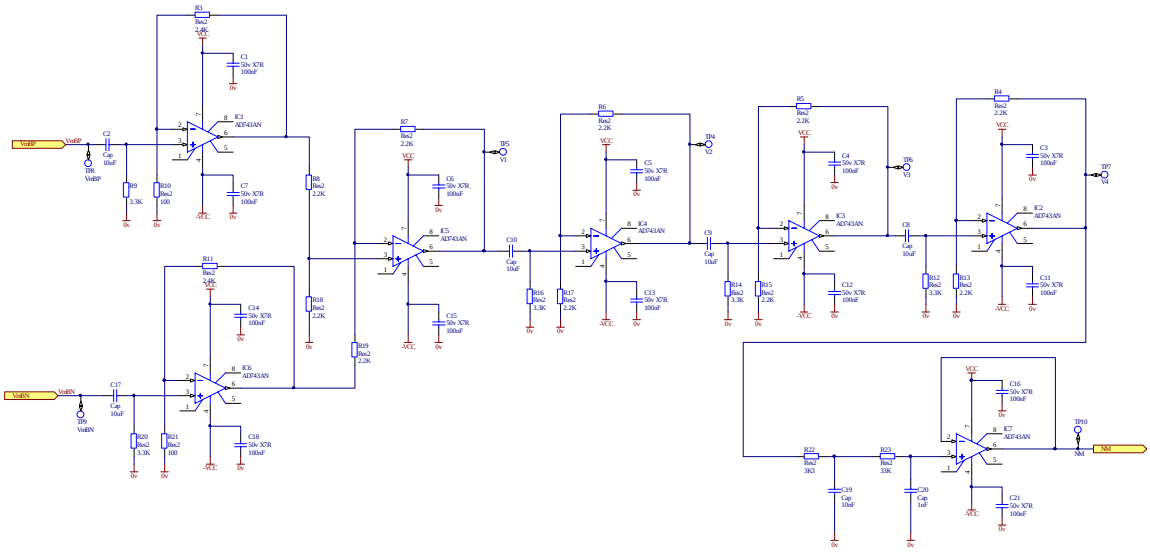
The anti-alias and anti-image filters used for the LASTI Noise prototype are the standard 3rd order, 10KHz Butterworth low pass filters with a notch at 65536 Hz. The fundamental sample frequency for the system is 65536 SPS and the data is software decimated to 16384 SPS for the controls. The figure below shows the schematic for a single channel of the anti-alias/anti-image filter.

3rd order Butterworth, 10KHz, notch at 65536Hz

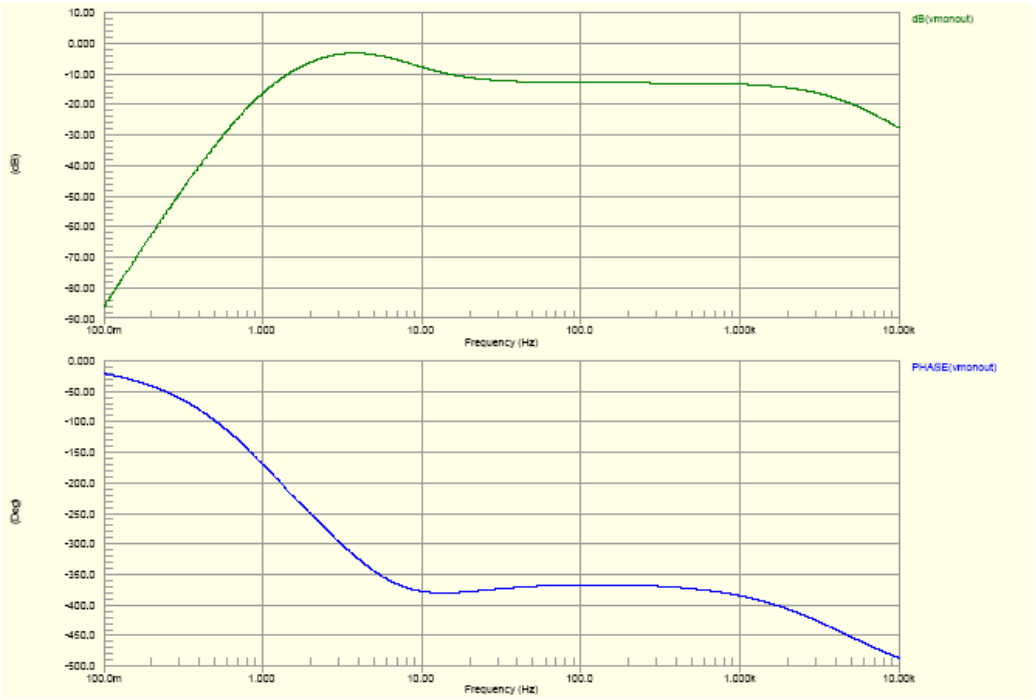


2.7 Additional Voltage, Current and Noise Monitors

Each of the coil driver channels have monitors for output voltage, output current (fast) and rms output current (slow). In addition, each coil driver output has a noise monitor channel that has been designed to allow the output noise floor of the driver to be measured at frequencies above 10 Hz. The figure below is a schematic of the noise monitor output for a typical driver channel. The input of this circuit is connected across the differential voltage output of the driver channel being monitored.



The typical response of the noise monitor circuit is shown in the figure below.



Note that the actual circuit design and response vary slightly for each type of coil driver.

The voltage and fast current monitor signal are DC coupled, direct, real-time measurements of the instantaneous coil driver output voltage and current. The slow current monitor is a low pass filtered measure of the rms coil driver output current. The design uses an AD736 rms to DC converter.

All of these channels are monitored by the control system and available to the framebuilder and data analysis tools such as DTT and dataviewer. The channel names for a typical coil driver channel are:

- Noise Monitor M1:SUS-MON-*stage-osem*-NM
- Voltage Monitor M1:SUS-MON-*stage-osem*-VM
- Fast Current M1:SUS-MON-*stage-osem*-FI
- Slow Current M1:SUS-MON-*stage-osem*-SI
- Where *stage* is the quad stage such as M0, R0, UI or PEN and *osem* is the particular OSEM for the stage, namely FACE1, FACE2, FACE3, LEFT, RIGHT, or SIDE for the M0 and R0 stages and UL, LL, UR or LR for the UI and PEN stages

2.8 ADC, DAC and Binary IO (BIO) Modules

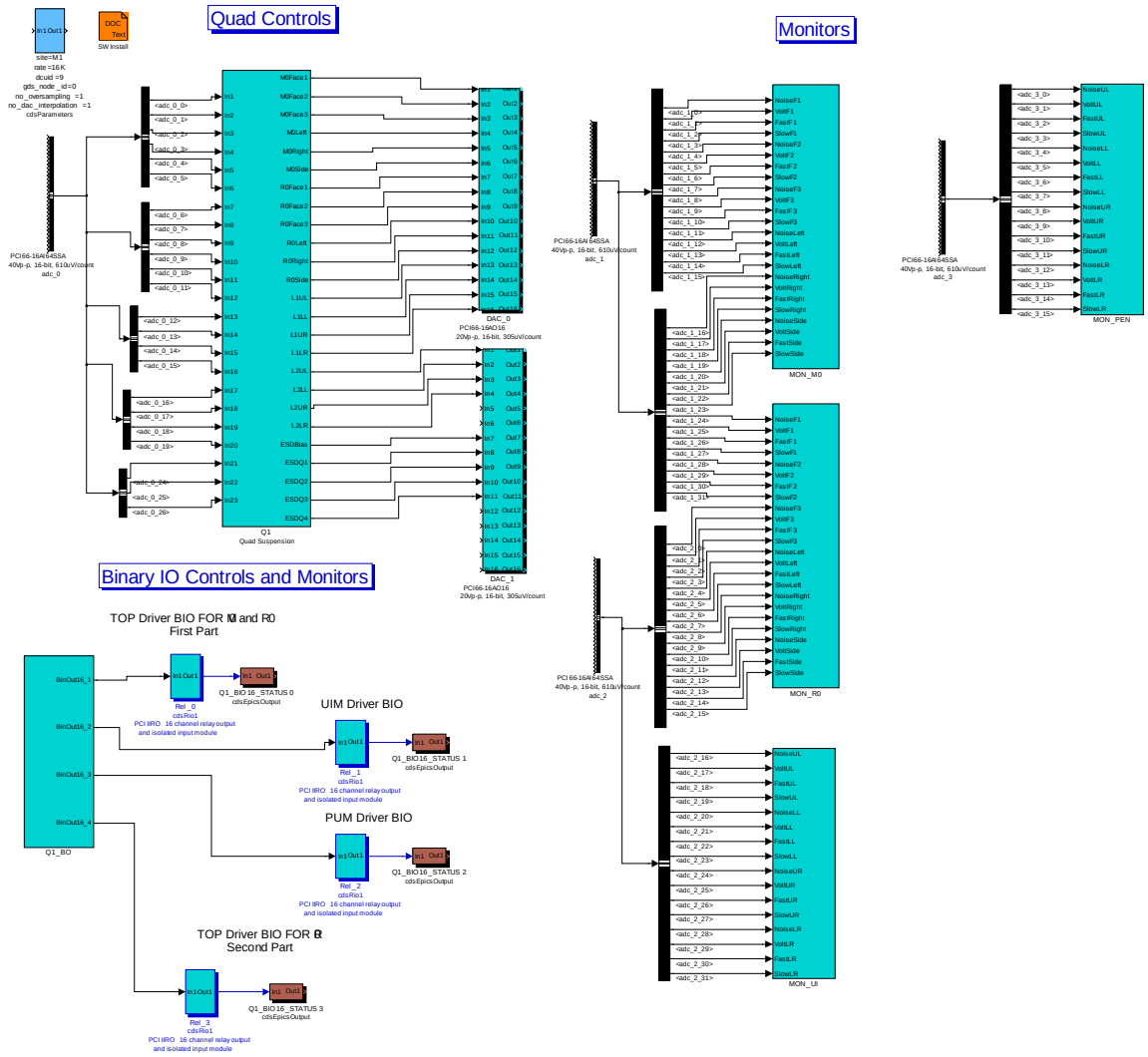
The ADCs and DACs used in the controls for the LASTI Noise prototype are the same ADC and DAC modules used in a variety of control systems at LASTI and elsewhere in LIGO. They are both manufactured by General Standards Corporation. The user manuals can be found at:

- ADC- http://www.generalstandards.com/user-manuals/pmc66_16ai64ssa_c_man_082006.pdf
- DAC- http://www.generalstandards.com/user-manuals/pmc66_16ao16_man_090406.pdf

The binary IO modules used in the control system are 16 channel isolated digital input, 16 channel relay output cards manufactured by Accesio. The manual for the card can be found at: http://www.accesio.com/MANUALS/PCI-IIRO-16.PDF .

3 Control Software

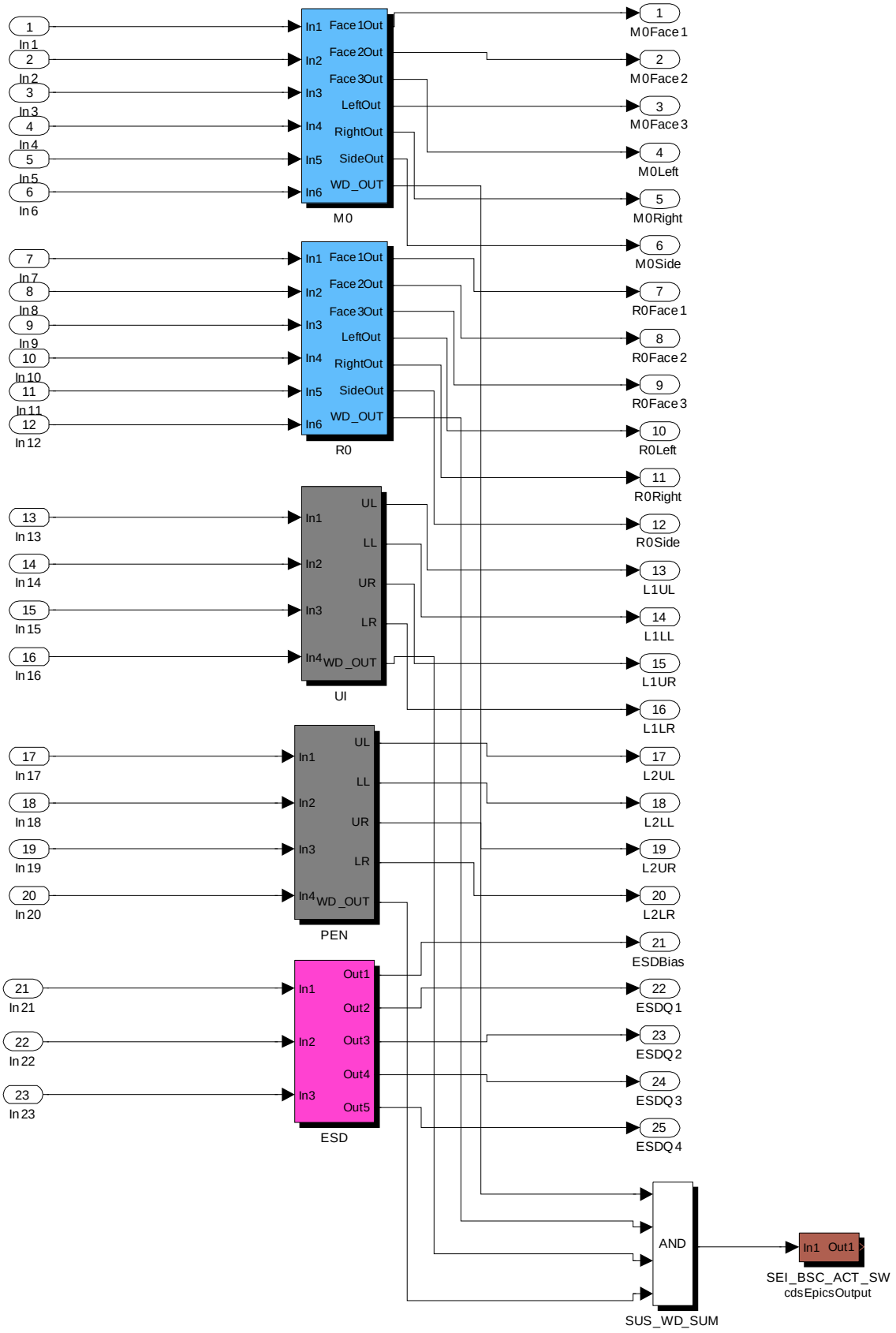
The control software for the LASTI Noise prototype was generated using Simulink and the real-time and Linux compilers used for all CDS control systems. The top level Simulink diagram for the system is shown in the figure below.



The main Simulink diagram is broken into three separate sections:

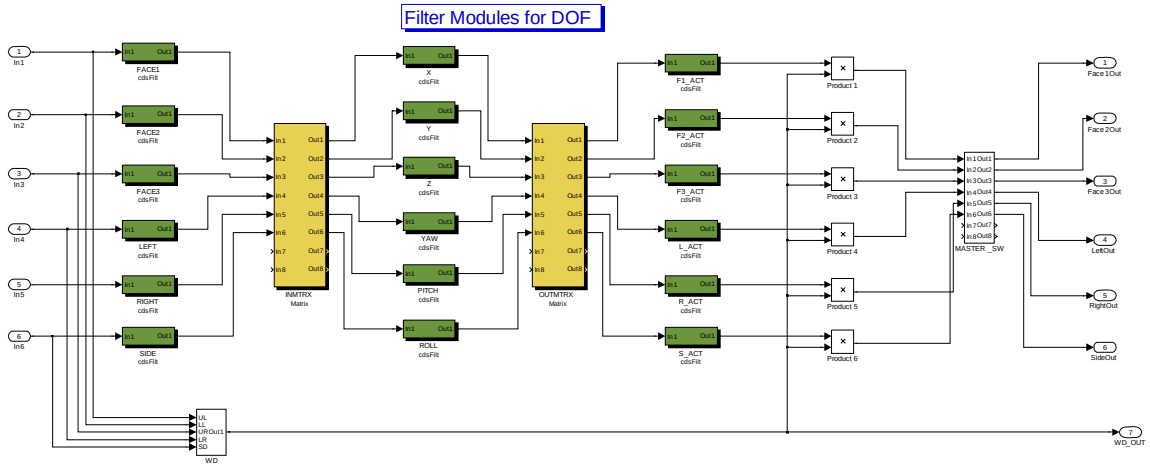
- Quad Controls—these are the OSEM inputs, input and output matrices, degrees of freedom and coil driver outputs that are used for the damping control of the quad.
- Monitors—these are the noise, voltage, fast current and slow current monitors for each coil driver channel
- Binary IO Controls and Monitors—these are the relay control and monitors for each of the filter and test inputs relays in each coil driver channel.

The figure below shows the inside of the Q1 subsystem block.


1
In1
2
In2
3
In3
4
In4
5
In5
6
In6
M0
Face1Out
Face2Out
Face3Out
LeftOut
RightOut
SideOut
WD_OUT
1
M0Face1
2
M0Face2
3
M0Face3
4
M0Left
5
M0Right
6
M0Side
7
In7
8
In8
9
In9
10
In10
11
In11
12
In12
R0
7
R0Face1
8
R0Face2
9
R0Face3
10
R0Left
11
R0Right
12
R0Side
13
In13
14
In14
15
In15
16
In16
UI
UL
LL
UR
LR
13
L1UL
14
L1LL
15
L1UR
16
L1LR
17
In17
18
In18
19
In19
20
In20
PEN
17
L2UL
18
L2LL
19
L2UR
20
L2LR
21
In21
22
In22
23
In23
ESD
Out1
Out2
Out3
Out4
Out5
21
ESDBias
22
ESDQ1
23
ESDQ2
24
ESDQ3
25
ESDQ4
AND
SUS_WD_SUM
Out1
SEI_BSC_ACT_SW
cdsEpicsOutput

As can be seen from the figure, the OSEM channels for each stage feed subsystem blocks for the corresponding stages. Note that each subsystem stage also provides a watchdog output that is summed and used as an interlock for the BSC seismic controls.

The figure below shows the control diagram for the M0 stage. The control diagrams for the other stages are similar.



The controls for the Binary IO and Monitor subsystems are typical of other CDS systems and the Simulink diagrams for each are self-explanatory.

4 Documentation List

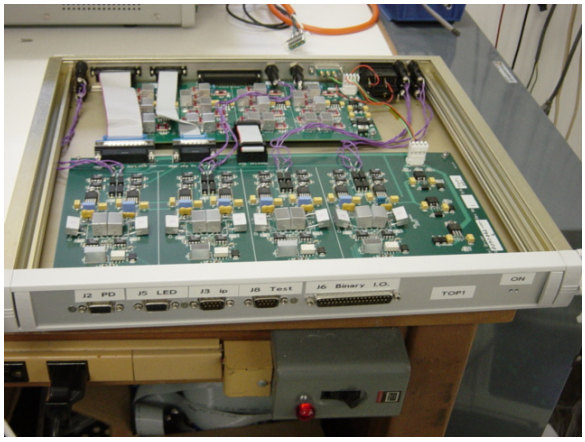
4.1 Schematics

LASTI Noise Prototype Controls Wiring (UK Electronics installed)—D080180-00-C
AdL AA and AI Filter (3rd order 10KHz, 65536 notch for 65536 sample rate)—D070081-01-C
UK TOP Coil Driver—drawing number TBD
UK UIM Coil Driver—drawing number TBD
UK PUM Coil Driver—drawing number TBD
UK Satellite Amplifier—drawing number TBD

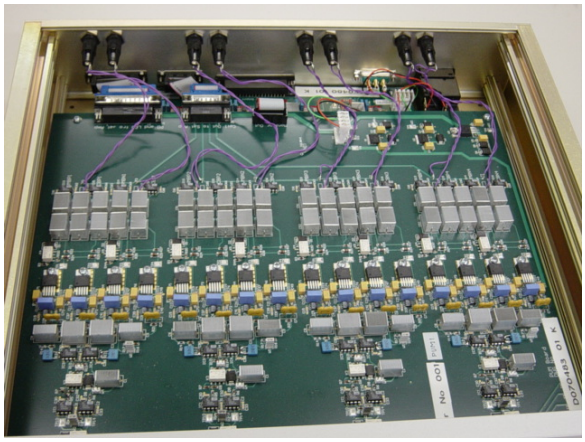
4.2 System and Chassis Photos

The picture below shows the UK Satellite Amplifier removed from the box.

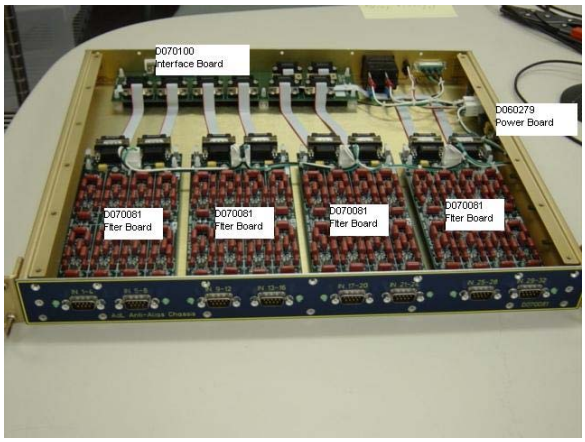
The picture below shows the TOP Coil Driver chassis with the top cover removed.



The picture below shows the Penultimate Coil Driver Chassis with the top cover removed.



The picture below shows the Anti-Alias Chassis with the top cover removed.



The picture below shows the Anti-Image Chassis with the top cover removed.