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CONVERTER BACKPLANE

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1 Introduction and Overview

This document describes the enclosure (crate), form factor and backplane of the new converter design.

2 Form Factor

2.1 Crate

We use an EMI compatible enclosure and follow the eurocrate standard as described by IEEE 1101.1/1101.10. This is basically the familiar VME type chassis, but we include keyable guide rails with ground pins and ESD clip and type IV injector/extractor handles. An example crate assembly can be found at http://www.kaparel.com (Ripac Vario EMC).

The total crate height will either be 7U or 8U to support circulating air both above and below the boards. This additional space will also be used to add a power switch and a series of LEDs indicating the status of the supply voltages.

Cooling is envisioned to be internal by circulating cool air from below the boards, up and down again behind the backplane. A water cooled heat exchanger is used to cool the air behind the backplane. A set of low noise slow rotating fans below the heat exchanger blowing downward may be required to keep the air flow going.

2.2 Slot Assignment

The width of a board assembly will be 6 HP (30.48 mm). This allows 14 slots in a full width crate. The slot to the most left (position 1) is dedicated as the power controller board. It contains voltage and current monitors, flow indication for the water cooling, temperature readouts and the fan controllers. The next board in slot 2 is timing fan-out board. There are 4 dedicated controller slots

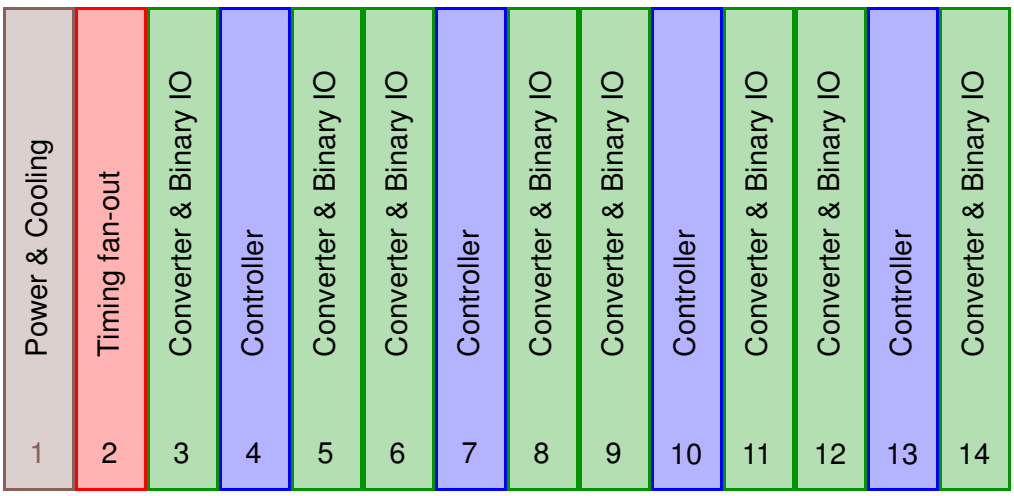

Figure 1: Slot assignment.

in position 4, position 7, position 10 and position 13. All others slots are used for converter and interface boards. Slots are keyed to prevent wrong insertion.

The back plane is split: Slots 1 and are stand alone, slots 3 through 8 and slots 9 through 14 are two separate but identical backplanes. Converter boards are connected to the closest controller slot through the backplane. The two controller slots of a backplane are also connected through the backplane. The controller boards come in two versions: either as a simple filter engine board or as a filter engine board together with an uplink. A single uplink board can exchange data with any converter board within the same backplane.

2.3 Board Dimensions

The board height is 6U or 233 mm. The board width has been set to 280 mm (120 mm deeper than a standard VME type board). Board assemblies are 6 HP wide or 30.48 mm. The clearance below the board is then 1 HP + 2.5 mm (7.6 mm) total. The bottom surface of a board can be used for components such as bypass capacitors. With a board thickness of 1.6 mm the maximum component height on the top surface is 18.8 mm—leaving a 2.5 mm gap to the next board.

2.4 Connectors

Converter boards use two standard 96-pin DIN 41612 connectors (P1 at the top and P2 at the bottom). This gives a total number of 192 individual connections. Connectors are mounted at the same position as on a standard VME board.

The controller boards use the same connectors as the VME64x standard. P1 and P3 are 5 row 160 pin connectors, whereas P0 is a (5+2) row 133 pin 2 mm hard metric connectors (IEC 61076-4-101). Only 5 rows can be used for signals.

3 Signal Convention

The connector pin assignments are given in Section 5.

3.1 Converter Interface

The signals between the converter boards and the controller boards are LVDS. There are 7 dedicated clock lines and 21 data lines for a total of 28 differential pairs. The direction of the lines depends on the board. There are also a couple of pins dedicated for the configuration EEPROM.

3.2 FPGA Interconnect

The signals between the controller boards and the signals between the FPGAs which are used for the filter engine and the uplink, respectively, are LVDS. They are divided into downstream and upstream signals. Each direction has 3 dedicated clock lines and 12 data lines for a total of 30 differential pairs. Clock 1A and data lines 1A through 6A are meant to interface the filter engine of the first converter board, whereas clock 1B and data lines 1B through 6B are meant to interface the filter engine of the second converter board. The downstream clock 2 is always driven by the synchronization output of an uplink FPGA.

Data lines are driven serially. The data rate is 2^{26} Hz (~67 MHz). Each data line is time multiplexed with 4 ADC or DAC channels. Using 32 bits for each ADC or DAC word this yields a sampling rate of 2^{19} Hz (~524 kHz). Four data lines are necessary to interface a 16 channel converter board. The direction of a data link depends on whether the converter board is an ADC or a DAC. An upstream data line is an input when it interfaces an ADC, and it is an output when it interfaces a DAC. On the other hand, a downstream data line is an output when driven by an ADC and an input when controlling a DAC.

An uplink FPGA connects to 4 filter engines: two are implemented on the same board and two can be reached through the backplane. For the on-board filter engines the interface consists of half the interface data lines—basically only the upstream half is implemented together with the downstream clock lines as well as the downstream data lines which are used for status information. The upstream data lines to the local filter engines are mirrored onto the downstream data lines on the backplane. Since the downstream and upstream lines are crossed-over in the backplane, an uplink FPGA on the other end will see the downstream data lines as upstream ones. Figure 2 shows a link diagram.

3.3 TIMING

The timing receiver is integrated into the uplink FPGA. The main clock signal is propagated to the filter engine FPGAs through downlink clock lines 1A and 1B. The clock is also used as the data clock. The synchronization signal (1 PPS) is sent through the downlink clock line 2. The uplink clock lines 1A and 1B can then be used as the data clocks for the return signals. The presence of a synchronization pulse on the uplink clock line 2 is an indication that the other end is an uplink FPGA rather than two separate filter engine FPGAs.

3.4 GIGABIT INTERFACE

Each uplink implements 2 gigabit ethernet ports.

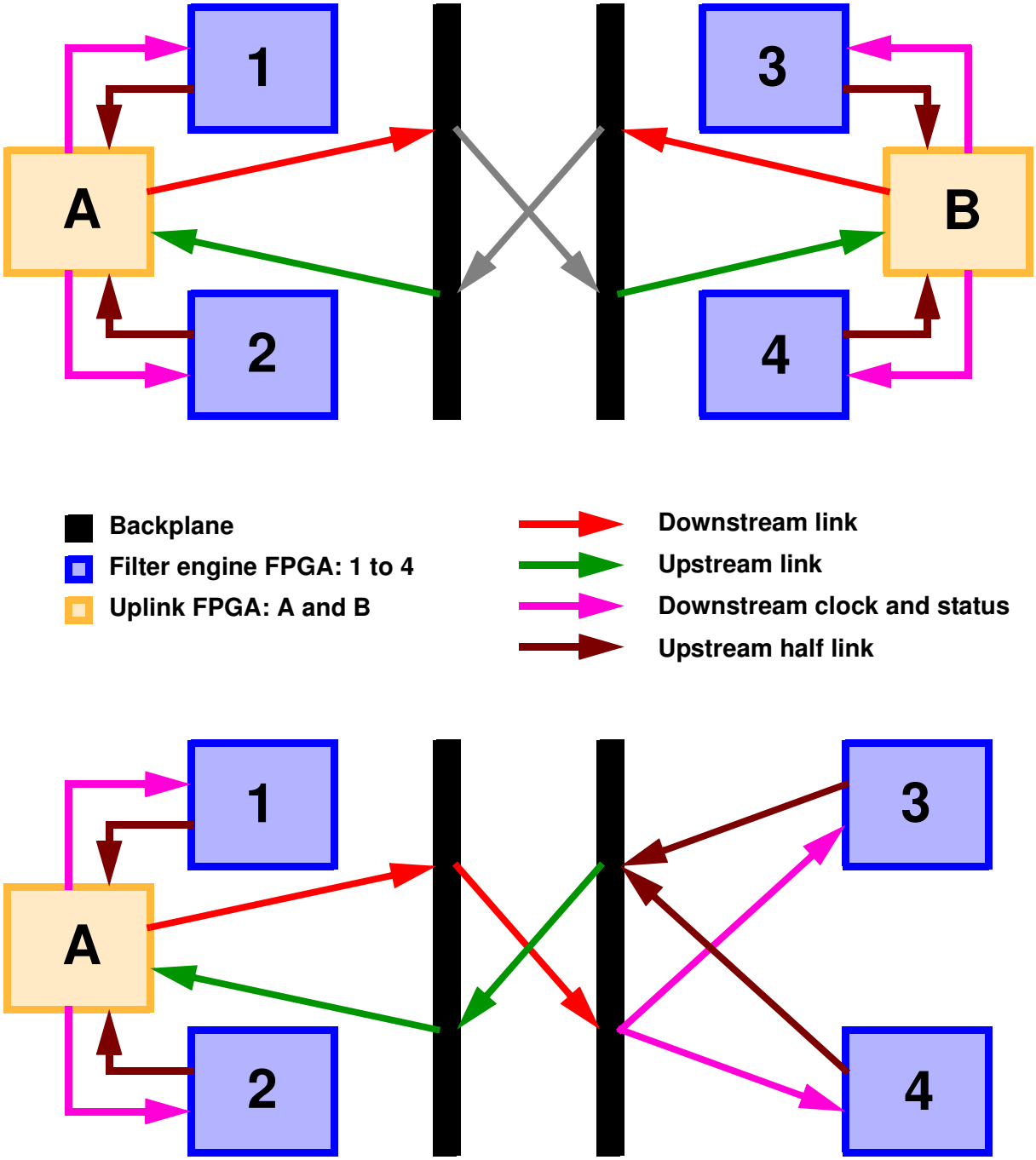

Figure 2: Link diagram between filter engines and uplink FPGAs. The top diagram shows two controller boards with uplinks interfacing each other. Each filter engine interfaces its corresponding converter board (not shown). The bottom diagram shows a controller board with uplink interfacing one without an uplink. The arrows indicate upstream and downstream direction. They are only indicating the data flow for ADC data. DAC data flows the opposite way.

4 Power Supplies

A sketch of the power supply components is shown in Figure 3. The power supplies are mounted at the back of the rack behind the heat exchanger. The back of the crate will employ a cool plate on which the regulators and converters can be mounted. In the current sketch all voltages are derived from 48V DC using low noise switching regulators. Both input EMI filters and output ripple filters are used to suppress noise. The total power provided to the backplane cannot exceed the thermal rating of the crate.

Alternatively, power is provided from an external supply.

4.1 Analog Supplies

Analog supplies are provided to the converter boards only. The analog supply voltages are meant to be regulated to 5.0V and 15.0V, respectively, using low drop-out linear regulators. Due to the sad state of low drop-out negative voltage regulators an additional ±24V is provided, so that a suitable supply voltage will be available for an on-board controller circuit.

Table 1: Analog Supplies

Name	Voltage	Tolerance	Current	Board
+AV1	+6.5V	±0.3V	10A	Converter
–AV1	–6.5V	±0.3V	10A	Converter
+AV2	+16.5V	±0.8V	10A	Converter
–AV2	–16.5V	±0.8V	10A	Converter
+AV3	+24V	±1.0V	2A	Converter
–AV3	–24V	±1.0V	2A	Converter

Since there are 10A of current available for each major analog rail, each converter board has a maximum rating of 1.25A per rail.

4.2 Digital Supplies

Only a +12V supply is provided to the controller boards. Local regulators are used to generate +5V, +3.3V and any other required digital voltage. The controller boards extend the +5V and the +3.3V digital supply to the converter boards. Converter boards may generate their digital supply which is most likely +3.3V from the +5V by use of a linear voltage regulator.

The 20A of current for the +12V supply is distributed over the two controller boards and possibly the timing fan-out. This gives a maximum rating of 10A per board. DV1 and DV2 are generated on the controller boards and a maximum of 6A is provided for the converter boards, yielding a maximum rating of 3A per board and rail. Since these voltages are derived from the +12V rail, one has to be careful not to exceed the maximum rating for the +12V supply.

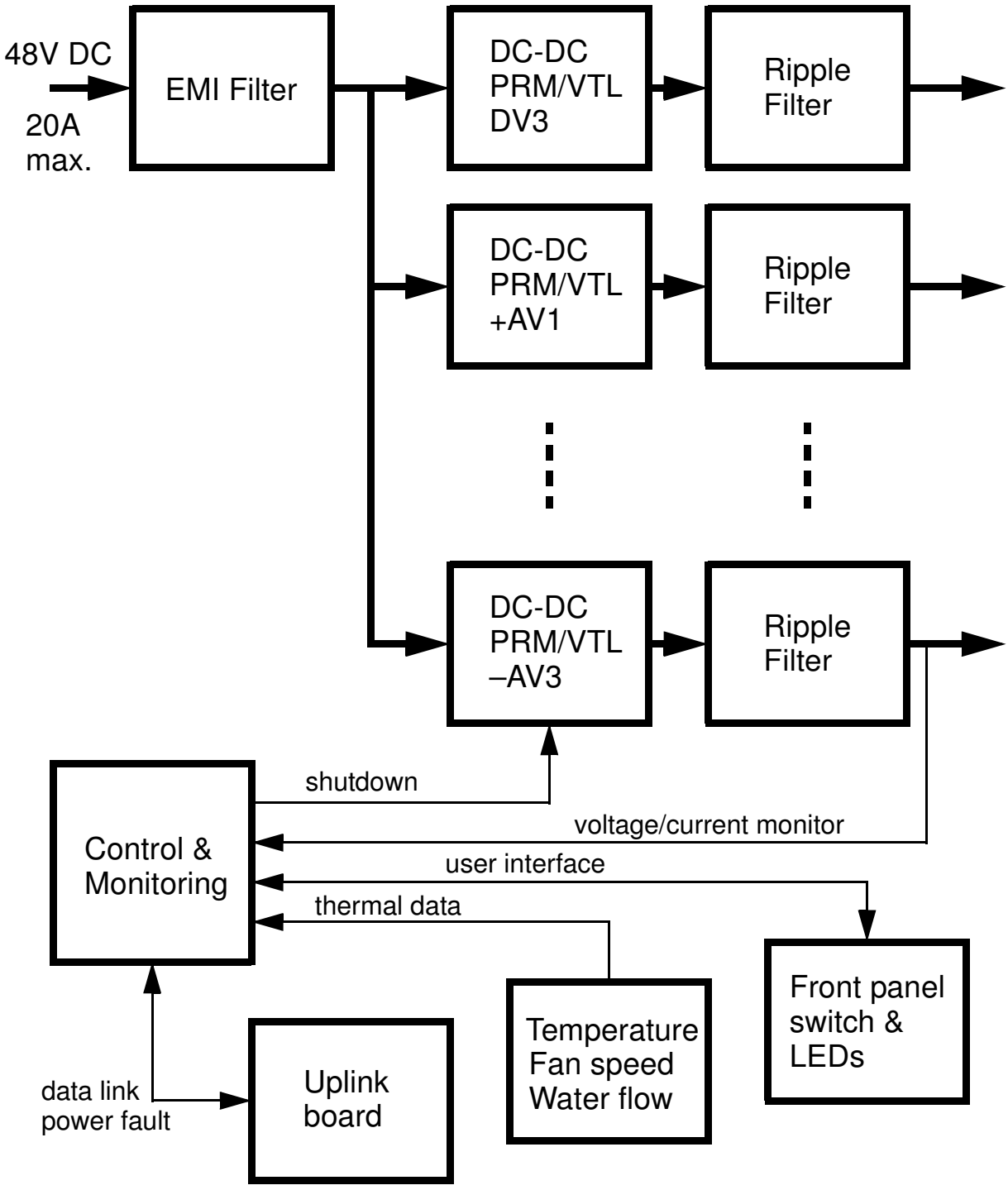

Figure 3: Sketch of power supply components.

Table 2: Digital Supplies

Name	Voltage	Tolerance	Current	Board
DV1	+5.0V	±0.3V	6A	Converter
DV2	+3.3V	±0.16V	6A	Converter
DV3	+12V	±0.6V	20A	Controller/Uplink
DV4	+48V	±1.2V	—	Auxiliary and stand-by power (not switched)

4.3 Control and Monitoring

The main power which is provided by the +48V input voltage is used for powering the power and cooling board. All other supplies in the back of the crate will have a thermal shutdown when the internal temperature exceeds 70°C, upon a fan failure or when the water flow in the cooling systems is interrupted. A front panel on-off switch can also be used to switch these DC-DC regulators in the back of the crate. The front panel switch does not disconnect the power supply but rather uses the shutdown control of the DC-DC converters. A true power switch is provided in the back to disconnect the 48V DC feed. Access to a set of fuses protecting each individual power rail as well as the 48V DC feed are also located in the back.

The power and cooling board reads both voltage and current from each power rail. The front panel of the power and cooling board consists of a power switch, a series of LEDs indicating the status of each supply line, and it has tip jacks (mini banana jacks) to hook up a DVM. Fan speed, probes to measure the crate temperatures and a water flow indicator are all made available by the power and cooling board. In the case of fan failures or high temperature alarm the power supplies will shut down automatically.

The control and monitoring board has its own voltage regulator derived form the +48V. This allows to switch off the main power supplies without loosing the control and monitoring functionality. This control and monitoring board also interfaces with the timing, so it can derive the switching frequencies for the synchronous buck regulators.

If the power is supplied externally, no control and monitoring board may be needed.

5 PIN ASSIGNMENT

Table 3: Signal Names

Signal	Description
DV1	Converter board digital power supply, +5V
DV2	Converter board digital power supply, +3.3V
DV3	Controller/uplink board digital power supply, +12V
DV4	Power and cooling board, +48V
GND	Digital ground
+AV1	Converter board analog power supply, +6V
–AV1	Converter board analog power supply, –6V
+AV2	Converter board analog power supply, +16.5V
–AV2	Converter board analog power supply, –16.5V
+AV3	Converter board analog power supply, +24V
–AV3	Converter board analog power supply, –24V
AGND	Converter board analog ground
Sx_P/Sx_N	28 LVDS signals between converter boards and a controller board
Ux_P/Ux_N	Uplink between controller boards; 3 clock lines and 12 LVDS signals
Dx_P/Dx_N	Downlink between controller boards; 3 clock lines and 12 LVDS signals
CFG_VCC/CFG_GND	Power supply for serial configuration EEPROM
CFG_CLK	Clock for serial configuration EEPROM
CFG_SI/CFG_SO	Serial input and output of configuration EEPROM
CFG_CS	Chip select for serial configuration EEPROM
CFG_RDY	Board present bit (must be connected to CFG_GND on converter and controller boards)

Analog ground (AGND) and digital ground (GND) are connected together in the backplane.

Table 4: Converter board P1

position	row a	row b	row c
1	GND	GND	DV1
2	S1_N	GND	DV1
3	S1_P	GND	DV1
4	GND	GND	DV1
5	S2_P	GND	DV1
6	S2_N	GND	DV1
7	GND	GND	DV2
8	S3_N	GND	DV2
9	S3_P	GND	DV2
10	GND	GND	DV2
11	S4_P	GND	DV2
12	S4_N	GND	DV2
13	GND	GND	DV3
14	S5_N	GND	DV3
15	S5_P	GND	
16	GND	GND	
17	S6_P	GND	
18	S6_N	GND	
19	GND	GND	
20	S7_N	GND	
21	S7_P	GND	
22	GND	GND	
23	S8_P	GND	
24	S8_N	GND	
25	S9_N	GND	+AV1
26	S9_P	GND	+AV1
27	S10_P	GND	+AV1
28	S10_N	GND	+AV1
29	S11_N	GND	–AV1
30	S11_P	GND	–AV1
31	S12_P	GND	–AV1
32	S12_N	GND	–AV1

Table 5: Converter board P2

position	row a	row b	row c
1	S13_N	GND	+AV2
2	S13_P	GND	+AV2
3	S14_P	GND	+AV2
4	S14_N	GND	+AV2
5	S15_N	GND	–AV2
6	S15_P	GND	–AV2
7	S16_P	GND	–AV2
8	S16_N	GND	–AV2
9	S17_N	GND	+AV3
10	S17_P	GND	+AV3
11	S18_P	GND	–AV3
12	S18_N	GND	–AV3
13	S19_N	GND	
14	S19_P	GND	
15	S20_P	GND	
16	S20_N	GND	
17	S21_N	GND	
18	S21_P	GND	
19	S22_P	GND	
20	S22_N	GND	
21	S23_N	GND	
22	S23_P	GND	
23	S24_P	GND	
24	S24_N	GND	
25	S25_N	GND	
26	S25_P	GND	CFG_GND
27	S26_P	GND	CFG_CLK
28	S26_N	GND	CFG_VCC
29	S27_N	GND	CFG_CS
30	S27_P	GND	CFG_SI
31	S28_P	GND	CFG_SO
32	S28_N	GND	CFG_RDY

Table 6: Controller board P1

position	row z	row a	row b	row c	row d
1	DV1	GND	GND	GND	DV1
2	DV1	S1A_N	GND	S1B_N	DV1
3	DV1	S1A_P	GND	S1B_P	DV1
4	DV1	GND	GND	GND	DV1
5	DV1	S2A_P	GND	S2B_P	DV1
6	DV1	S2A_N	GND	S2B_N	DV1
7	DV2	GND	GND	GND	DV2
8	DV2	S3A_N	GND	S3B_N	DV2
9	DV2	S3A_P	GND	S3B_P	DV2
10	DV2	GND	GND	GND	DV2
11	DV2	S4A_P	GND	S4B_P	DV2
12	DV2	S4A_N	GND	S4B_N	DV2
13	DV3	GND	GND	GND	DV3
14	DV3	S5A_N	GND	S5B_N	DV3
15	DV3	S5A_P	GND	S5B_P	DV3
16	DV3	GND	GND	GND	DV3
17	DV3	S6A_P	GND	S6B_P	DV3
18	DV3	S6A_N	GND	S6B_N	DV3
19	DV3	GND	GND	GND	DV3
20	DV3	S7A_N	GND	S7B_N	DV3
21	DV3	S7A_P	GND	S7B_P	DV3
22	GND	GND	GND	GND	GND
23	GND	S8A_P	GND	S8B_P	GND
24	GND	S8A_N	GND	S8B_N	GND
25	GND	S9A_N	GND	S9B_N	GND
26	GND	S9A_P	GND	S9B_P	GND
27	GND	S10A_P	GND	S10B_P	GND
28	GND	S10A_N	GND	S10B_N	GND
29	GND	S11A_N	GND	S11B_N	GND
30	GND	S11A_P	GND	S11B_P	GND
31	GND	S12A_P	GND	S12B_P	GND
32	GND	S12A_N	GND	S12B_N	GND

Table 7: Controller board P0 (type B)

position	row a	row b	row c	row d	row e
1	GND	GND	GND	GND	GND
2	DCLK1A_P	GND	DCLK2_P	GND	UCLK1A_P
3	DCLK1A_N	GND	DCLK2_N	GND	UCLK1A_N
4	GND	GND	GND	GND	GND
5	DCLK1B_P	GND	UCLK2_P	GND	UCLK1B_P
6	DCLK1B_N	GND	UCLK2_N	GND	UCLK1B_N
7	GND	GND	GND	GND	GND
8	D1A_P	D2A_P	GND	U1A_P	U2A_P
9	D1A_N	D2A_N	GND	U1A_N	U2A_N
10	D3A_P	D4A_P	GND	U3A_P	U4A_P
11	D3A_N	D4A_N	GND	U3A_N	U4A_N
12	D5A_P	D6A_P	GND	U5A_P	U6A_P
13	D5A_N	D6A_N	GND	U5A_N	U6A_N
14	D1B_P	D2B_P	GND	U1B_P	U2B_P
15	D1B_N	D2B_N	GND	U1B_N	U2B_N
16	D3B_P	D4B_P	GND	U3B_P	U4B_P
17	D3B_N	D4B_N	GND	U3B_N	U4B_N
18	D5B_P	D6B_P	GND	U5B_P	U6B_P
19	D5B_N	D6B_N	GND	U5B_N	U6B_N

Table 8: Controller board P2

position	row z	row a	row b	row c	row d
1	GND	S13A_N	GND	S13B_N	GND
2	GND	S13A_P	GND	S13B_P	GND
3	GND	S14A_P	GND	S14B_P	GND
4	GND	S14A_N	GND	S14B_N	GND
5	GND	S15A_N	GND	S15B_N	GND
6	GND	S15A_P	GND	S15B_P	GND
7	GND	S16A_P	GND	S16B_P	GND
8	GND	S16A_N	GND	S16B_N	GND
9	GND	S17A_N	GND	S17B_N	GND
10	GND	S17A_P	GND	S17B_P	GND
11	GND	S18A_P	GND	S18B_P	GND
12	GND	S18A_N	GND	S18B_N	GND
13	GND	S19A_N	GND	S19B_N	GND
14	GND	S19A_P	GND	S19B_P	GND
15	GND	S20A_P	GND	S20B_P	GND
16	GND	S20A_N	GND	S20B_N	GND
17	GND	S21A_N	GND	S21B_N	GND
18	GND	S21A_P	GND	S21B_P	GND
19	GND	S22A_P	GND	S22B_P	GND
20	GND	S22A_N	GND	S22B_N	GND
21	GND	S23A_N	GND	S23B_N	GND
22	GND	S23A_P	GND	S23B_P	GND
23	GND	S24A_P	GND	S24B_P	GND
24	GND	S24A_N	GND	S24B_N	GND
25	GND	S25A_N	GND	S25B_N	GND
26	CFG_GND	S25A_P	GND	S25B_P	CFG_GND
27	CFG_CLK	S26A_P	GND	S26B_P	CFG_CLK
28	CFG_VCC	S26A_N	GND	S26B_N	CFG_VCC
29	CFG_CS	S27A_N	GND	S27B_N	CFG_CS
30	CFG_SI	S27A_P	GND	S27B_P	CFG_SI
31	CFG_SO	S28A_P	GND	S28B_P	CFG_SO
32	CFG_RDY	S28A_N	GND	S28B_N	CFG_RDY

Table 9: Power and Cooling board P1

position	row a	row b	row c
1	12VCC	GND	12VCC
2	12VCC	GND	12VCC
3	SYNC12	GND	SYNC24
4	RUN	GND	GND
5	I12P	GND	I24P
6	GND	GND	I24N
7	V12P	GND	V24P
8	GND	GND	V24N
9	LED12P	GND	LED24P
10	GND	GND	LED24N
11	12VCC	GND	12VCC
12	12VCC	GND	12VCC
13	SYNC7	GND	SYNC17
14	GND	GND	GND
15	I7P	GND	I17P
16	I7N	GND	I17N
17	V7P	GND	V17P
18	V7N	GND	V17N
19	LED7P	GND	LED17P
20	LED7N	GND	LED17N
21	GND	GND	GND
22	T1P	GND	T1N
23	T2P	GND	T2N
24	T3P	GND	T3N
25	GND	GND	GND
26	V48P	GND	P24V
27	FAN1P	GND	FAN2P
28	FAN1N	GND	FAN2N
29	FAN1S	GND	FAN2S
30	FAN3P	GND	FLOWP
31	FAN3N	GND	FLOWN
32	FAN3S	GND	FLOWS

Table 10: Power and Cooling board P2

position	row a	row b	row c
1		GND	PWRFAIL
2		GND	
3		GND	
4		GND	
5		GND	
6		GND	
7		GND	
8		GND	
9	GND	GND	
10	S1_N	GND	
11	S1_P	GND	
12	GND	GND	
13	S2_P	GND	
14	S2_N	GND	
15	GND	GND	
16	S3_N	GND	
17	S3_P	GND	
18	GND	GND	
19	S4_P	GND	
20	S4_N	GND	
21	GND	GND	
22	S5_N	GND	
23	S5_P	GND	
24	GND	GND	
25	S6_P	GND	
26	S6_N	GND	CFG_GND
27	GND	GND	CFG_CLK
28	S7_N	GND	CFG_VCC
29	S7_P	GND	CFG_CS
30	GND	GND	CFG_SI
31	S8_P	GND	CFG_SO
32	S8_N	GND	CFG_RDY