LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number T040142-00-C	June 28, 2004
ELECTRO-OPTICAL DATA LINK		
S. Liu		

Distribution of this draft: NSF reviewers, LIGO scientists
This is an internal working note of the LIGO Laboratory

California Institute of Technology
LIGO Project – MS 18-33
Pasadena, CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project – MS 20B-145
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

www: http://www.ligo.caltech.edu/

ELECTRO-OPTICAL DATA LINK

INTRODUCTION

In a laboratory enviroment, external electromagnetic interference (EMI) often corrupts signal integrity when sent from one location to another through long wires. If the same signal were transmitted through optical fibers , we not only gain complete EMI immunity but also higher speed in data transfer. Recent test result indicates that optical fibers are a good candidate for the LIGO's timing system design.

BRIEF OVER VIEW

Advantages of fiber optic cable over wire:

Speed: Can operate at speed up to gigabits.

Bandwidth: Large carrying capacity

Distance: Signals can be transmitted further without needing repeaters.

EMI immunity: Greater resistance to radios, motors or other nearby cables "noise".

Maintenance: Costs much less to maintain.

THEORY OF OPERATION

A fiber-optic system uses light pulses to transmit information down a fiber cable instead of using electronic pulses down a copper line as shown in Figure 1 below:

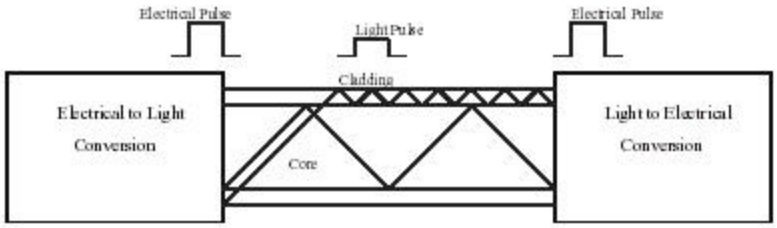


Figure 1. Basic fiber-optic system (electro-optical link)

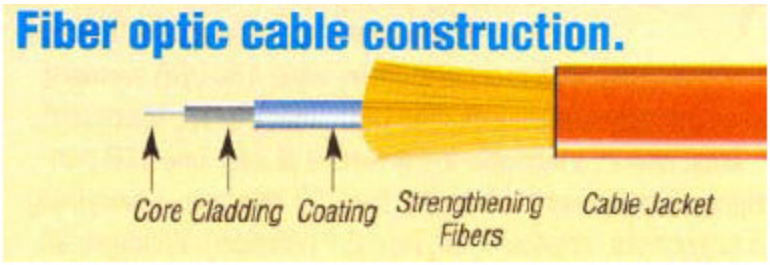


Figure 2. A typical fiber optic cable construction

At the transmitter end, electronic pulses are translated into light pulses using a light-emitting diode (LED) or a laser diode (LD). These light pulses are then "guided" through total internal reflection down the fiber optic to the receiver where they are converted back into electrical pulses.

CIRCUIT DESIGN

Electro-optical transmitter

The transmitter section consists of an AND gate peripheral driver and an Agilent HFBR-1412 optical transmitter. Pull up resistor R9 sets up the AND gate for proper operation. Resistor R10 limits current through the LED in the optical transmitter to prevent diode damage. The rest of the components (L, C) filters power supply noise.

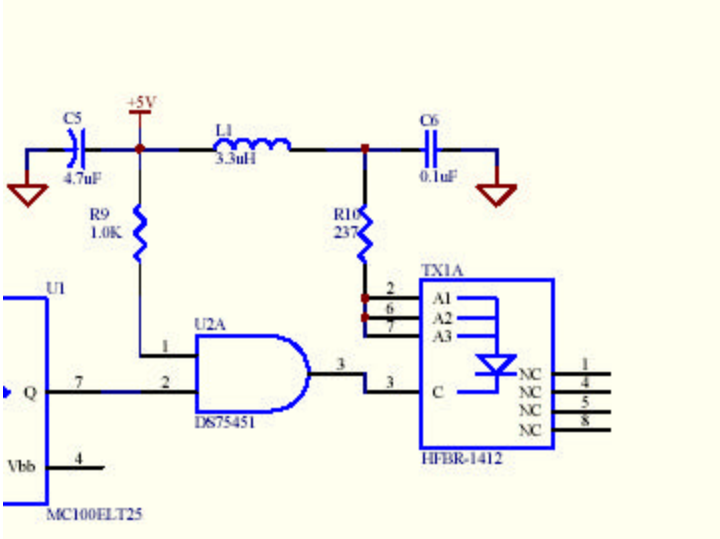


Figure 3. Electro-optical transmitter

Electro-optical receiver

The receiver section consists of an Agilent HFBR-2412 optical receiver and a pull up resistor R13 for proper interfacing with Transistor-Transistor Logic (TTL) family devices.

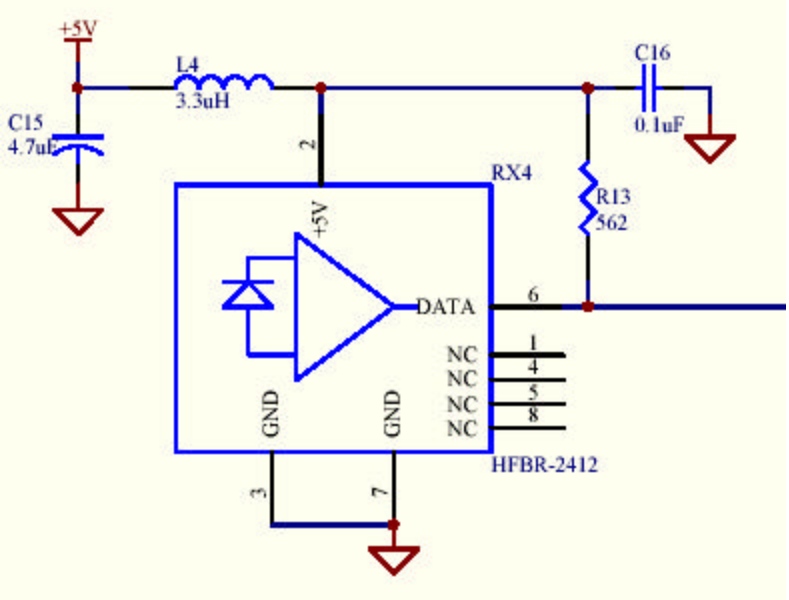


Figure 5. Electro-optical Receiver

Emitter coupled logic (ECL) to TTL interface

The resistor network, R1 through R4, provide line termination for the incoming differential ECL signals that source current in both HIGH and LOW states. (Voh ~ -1.9V, Vol ~ -0.9V). The MC100ELT25 logic level translator shifts the incoming signal into TTL level (Voh > 2.4V, Vol < 0.8V) for data processing.

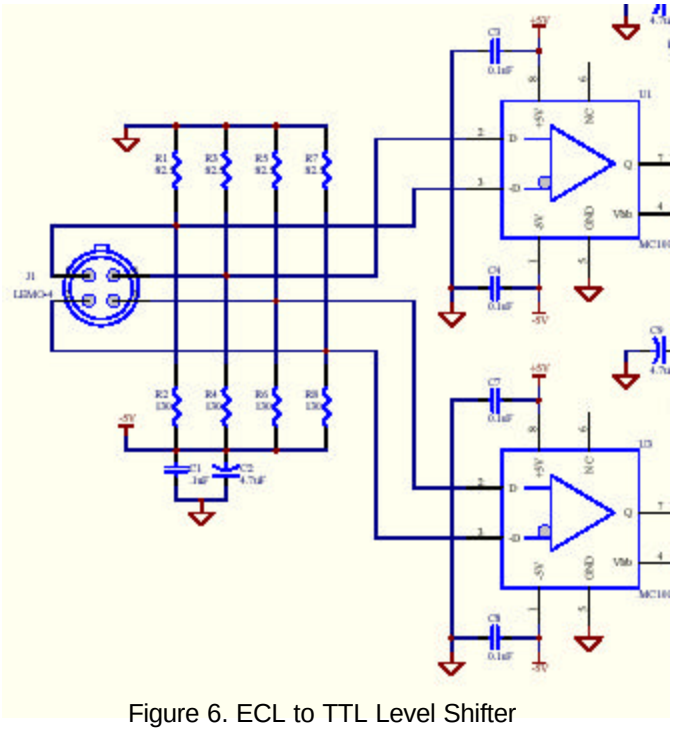
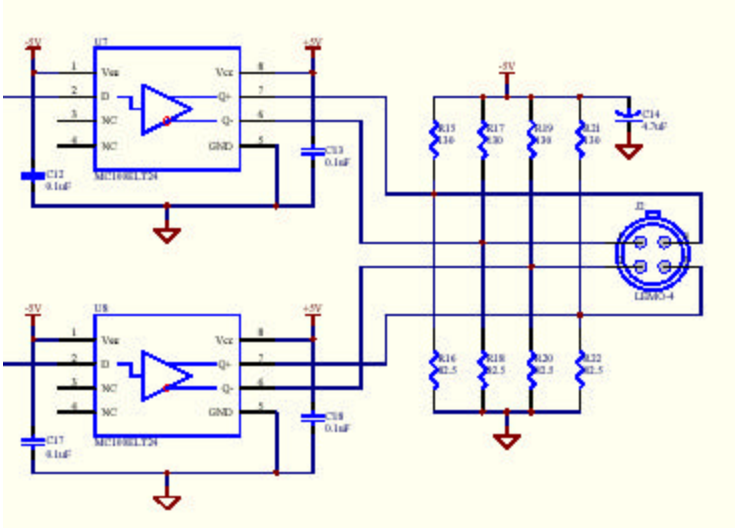


Figure 6. ECL to TTL Level Shifter

TTL to Differential ECL Driver

The output stage of the Electro-Optical (EO) DataLink consist of the MC100ELT24 TTL to ECL level translator and the line termination resistor network formed by resistor R15 through R18. Theoretically, the termination network should be located at the input of the receiver board down stream. It was added here, just in case, to prevent transmission line effects.



Fighre 7. TTL to ECL Driver

Frequency Divider

The receiver board contain a frequency divider network (1, 1/2, 1/4, 1/8 ; switch selectable) to provide lower clock pulse as needed.

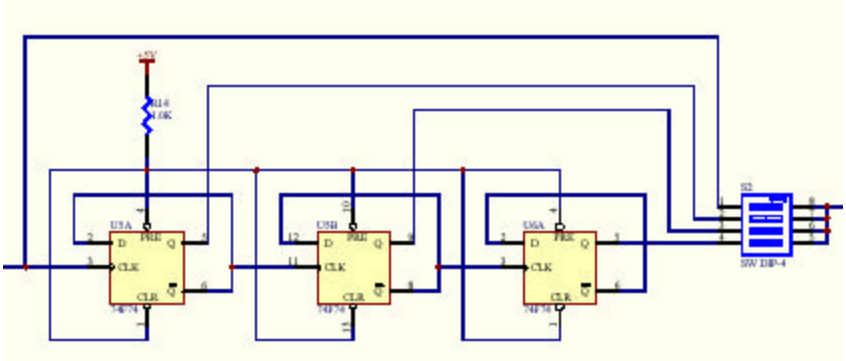


Figure 8. Frequency Divider

Complete schematics for the EO Data Link and the prototype printed circuit boards built are shown in Figures 9 through 12 below:

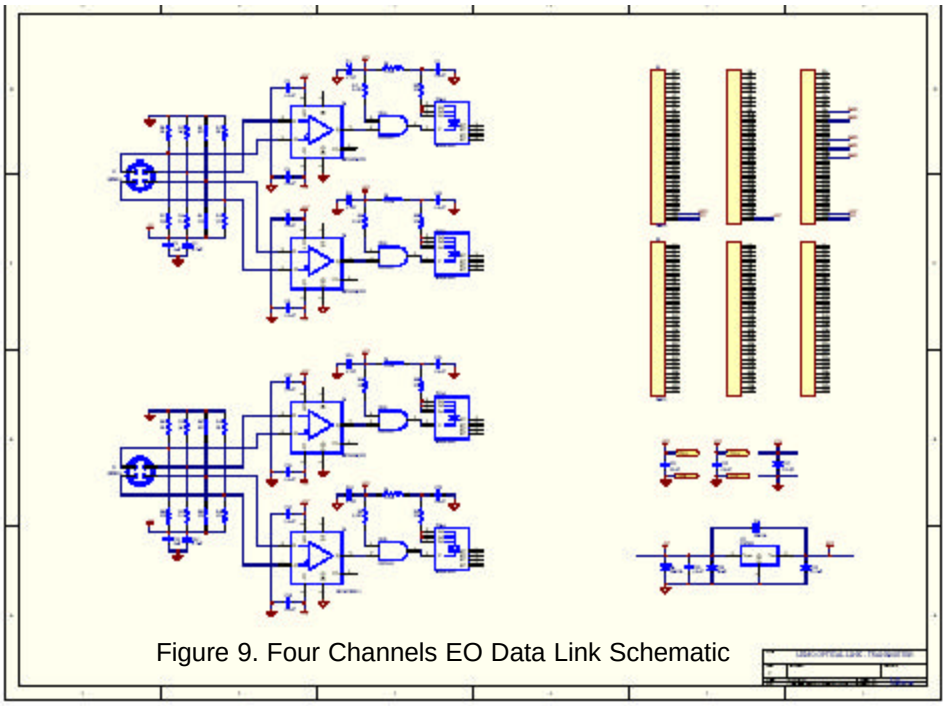


Figure 9. Four Channels EO Data Link Schematic

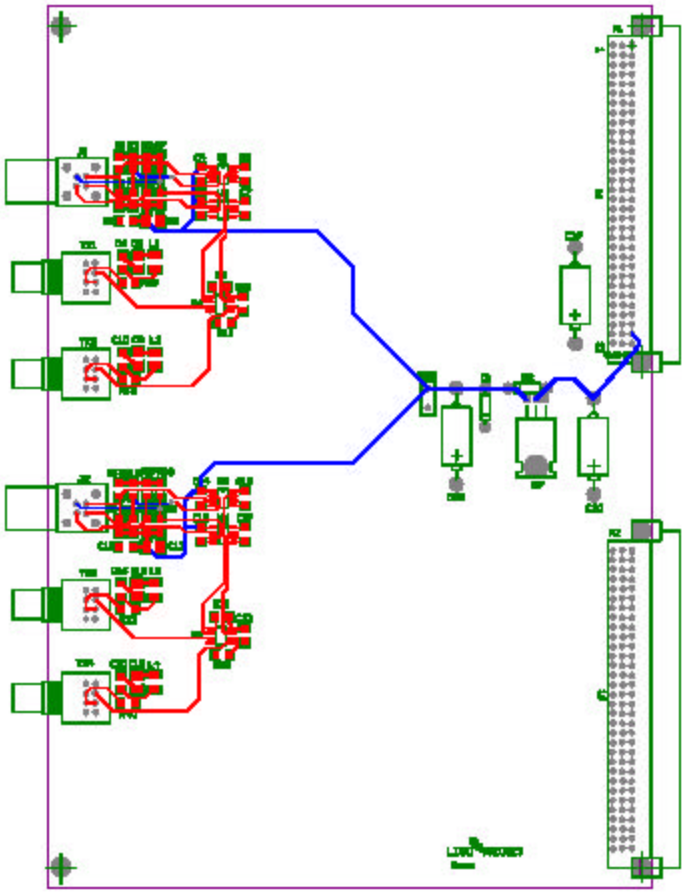


Figure 10. 4 Channel EO Data Link Transmitter Board.

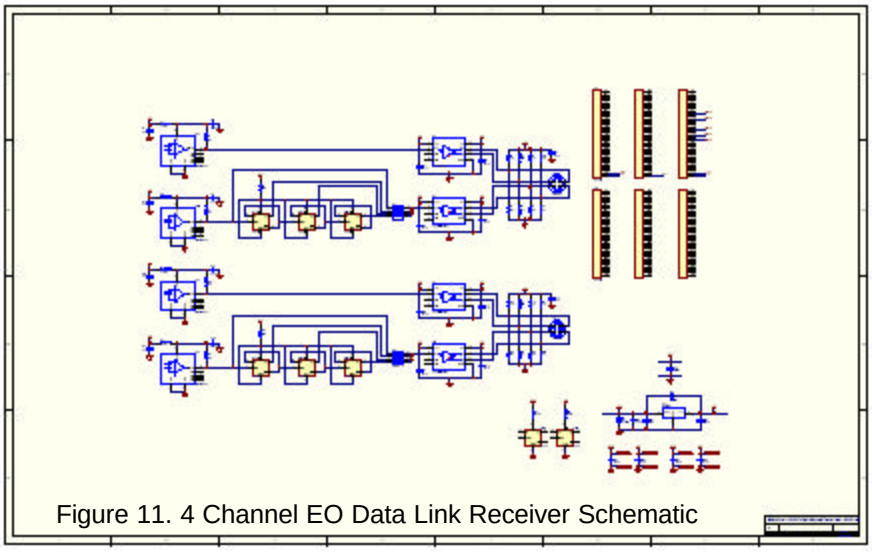


Figure 11. 4 Channel EO Data Link Receiver Schematic

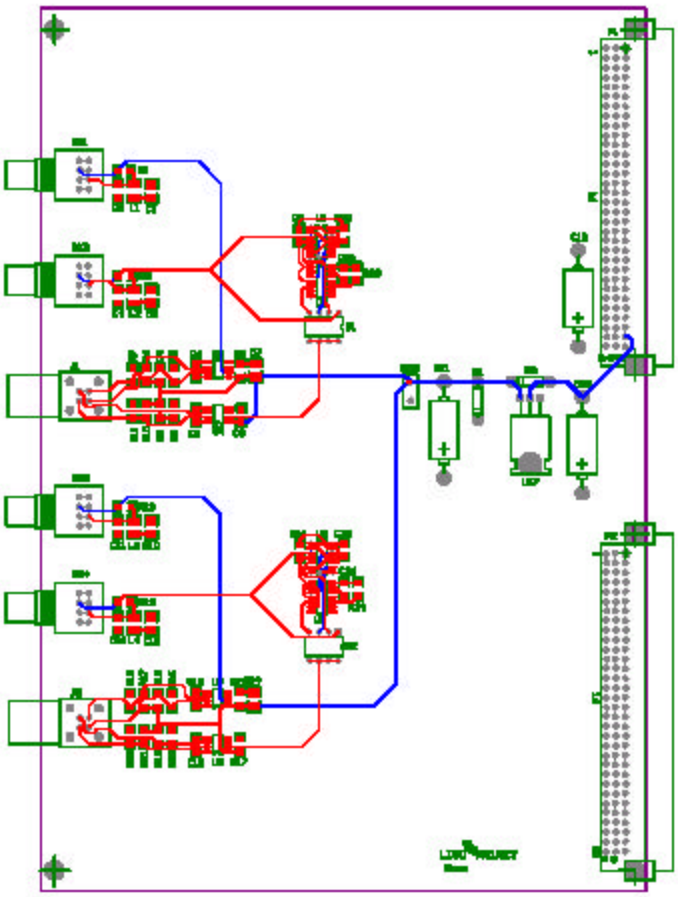


Figure 12. 4 Channel EO Data Link Receiver Board.

EXPERIMENTAL SETUP

The new EO Data Link Transmitter (Tx) and Receiver (Rx) boards were tested using both the Tracewell T-Frame VME board tester as well as a home grown VME board tester. The T-Frame tester was populated with the following VME cards:

1.0 Motorola 162PA Central Processor Unit (CPU).

2.0 jxi2 VME-SyncClock32 Global Positioning System (GPS) board.

3.0 D980362 Clock Fanout Board.

4.0 Tx transmitter Board

5.0 Rx Receiver Board

6.0 D990194 ISC Fanout Board

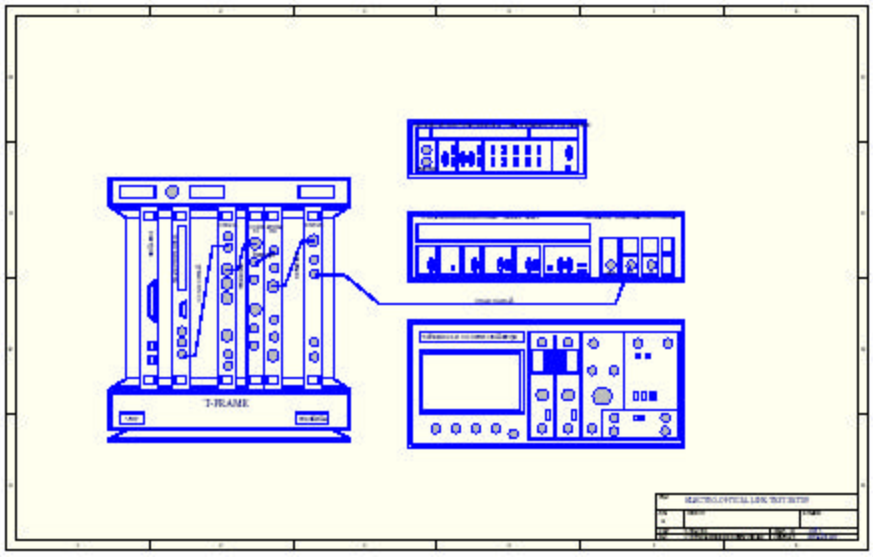


Figure 13. EO Data Link Test Setup

EQUIPEMENTS:

1.0 Stanford Research SR620 Universal Interval Counter.

2.0 Stanford Research DS345 30 MHz Synthesized Function Generator.

3.0 Tektronix 2465 300 MHz Oscilloscope.

TEST PROCEDURE:

1.0 Functional test of the GPS's 1 PPS sync pulse and the 4 MHz clock with the Tektronix oscilloscope.

2.0 Measure the 4 MHz clock jitter from the GPS board with the SR620 counter.

3.0 Connect both outputs of the GPS board to the D980362 Clock Fanout board through couple of coax cables.

4.0 Connect output of one D980362 channel to the Tx board with a short twisted pair cable.

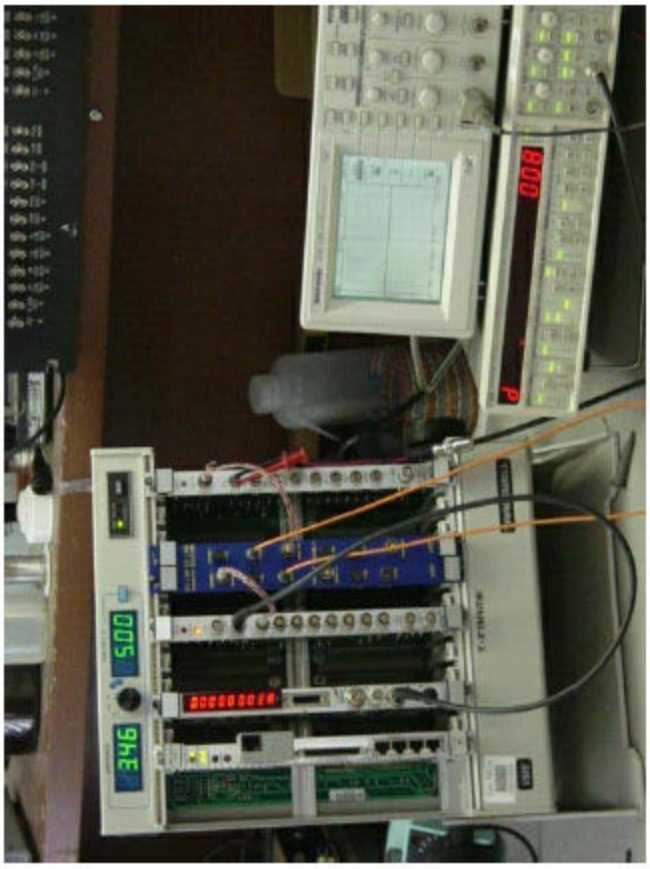
5.0 Connect output of Tx to the Rx board with couple of multimode fiber optic cable.

6.0 Connect output of the Rx board to the D990194 ISC Fanout board.

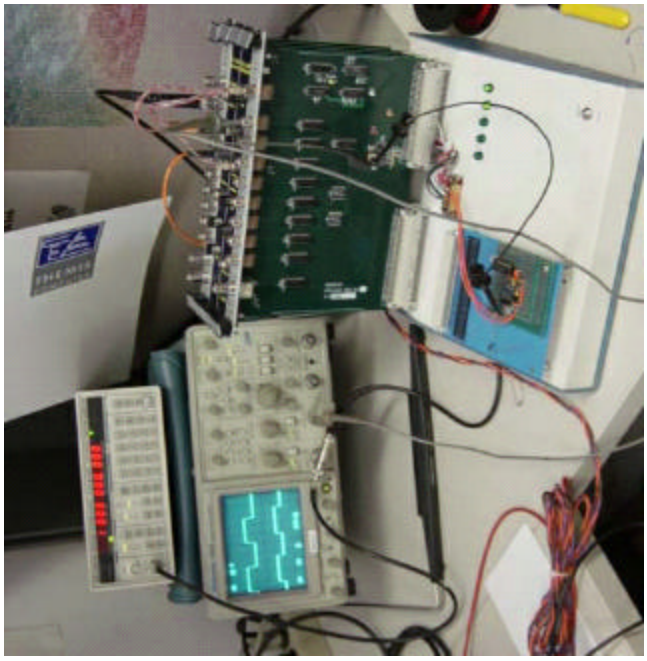
7.0 Functional test of both the 1 PPS synch pulse as well as the 4MHz clock pulse with the oscilloscope.

8.0 Measure jitter on the 4 MHz clock with the SR620 counter.

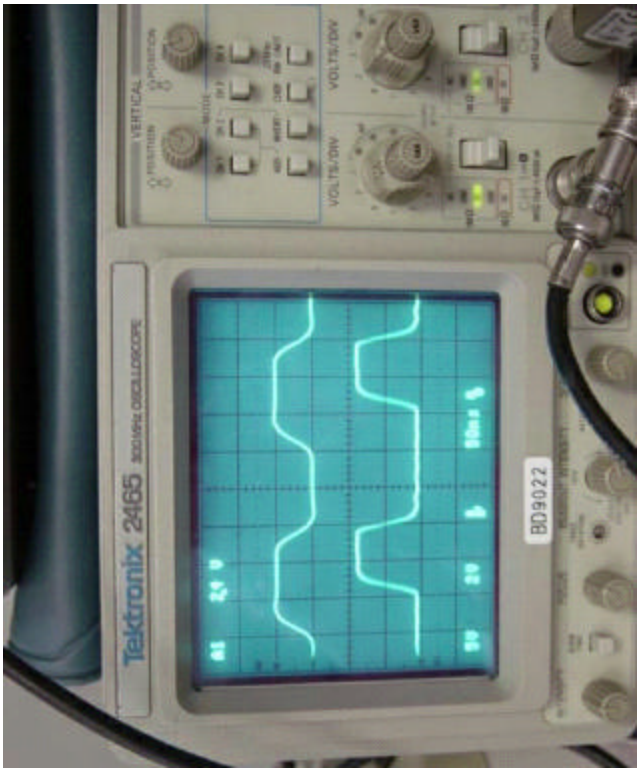
When measured directly, jitter of the 4 MHz clock from the GPS board varies between 11 to 13 picoseconds. After passing through the EO Data Link, the jitter fell below the random "noise" level or 8 to 10 picoseconds of the SR620 counter as indicated of the picture below:.



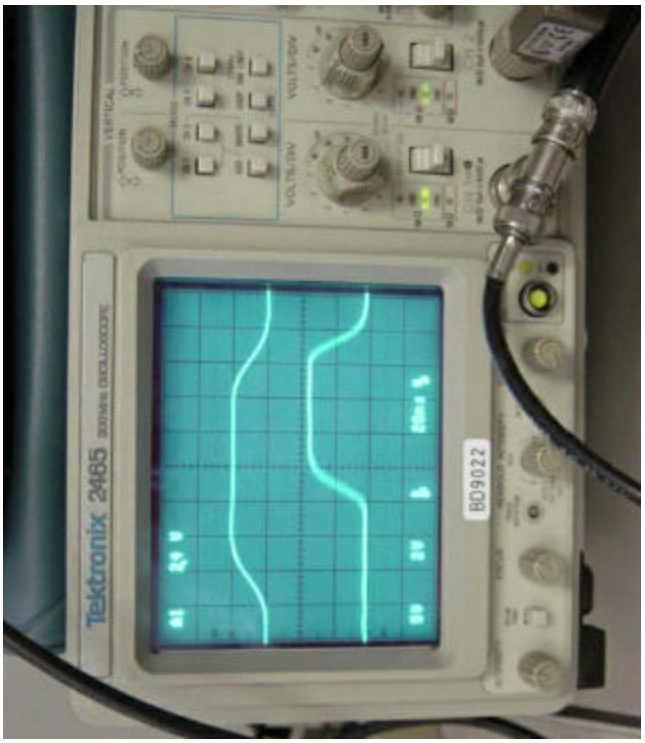
The four boards: D980362, Tx, Rx and D990194 were then transferred to the stand-alone VME tester using the DS345 as input as shown in the picture below:



No increase in noise level was observed from input to output of the system. The following picture shows the system running at 4 MHz.



Increasing the time base of the oscilloscope, a time delay of approximate 60 nano seconds was measured at this frequency as shown in the picture below:



CONCULSION

Using electro-optical data link not only simplifies timing system circuit design, but also improve system EMI immunity.

Most of the circuitries on the Tx and Rx board serve to properly interface with the Emitter-Coupled-Logic (ECL) used in the existing fanout and driver boards and will not be required for any new timing system design. The actual EO Data Link hardware is rather simple and well behaving.