**PZT Driver -Quick Start Guide**
**LIGO-T070063-00-C**
**R. Abbott, Caltech**
**15 March, 2007**

**Hardware Revision Applicability – Revision B. Unit complies with T060123, LIGO Standard Electrical Interfaces.**

## 1. Overview

1.1. The PZT driver (LIGO-D060283-B) provides the high voltage (0 to 300V) drive for Piezo Transducers. **This chassis contains potentially lethal voltages. Extreme care must be used.** Each unit can be tailored for use over a specific operating voltage range.

1.2. The piezo drive can be modulated for dither locking at frequencies from 2 to 20 kHz. Dither modulation can be applied from a DAC (Digital to Analog) interface, or from a front panel BNC.

1.3. The piezo output drive has two separate voltage monitors – a DC coupled monitor, and an AC coupled monitor.

## 2. Electrical Interfaces

2.1. All **front panel inputs** are true-differential, bipolar +/- 10 volt range. The input impedance is 10k ohms on all inputs. Inputs voltages should be limited to +/- 15 volts to avoid damage.

2.2. All **front panel outputs** are fully differential +/- 10 volt range. Load impedances should be greater than 1k ohm.

2.3. The required **low voltage power supply** is nominally +/- 18 VDC @ 0.2 amps. A range of voltages from +/-16 to +/- 24 is acceptable.

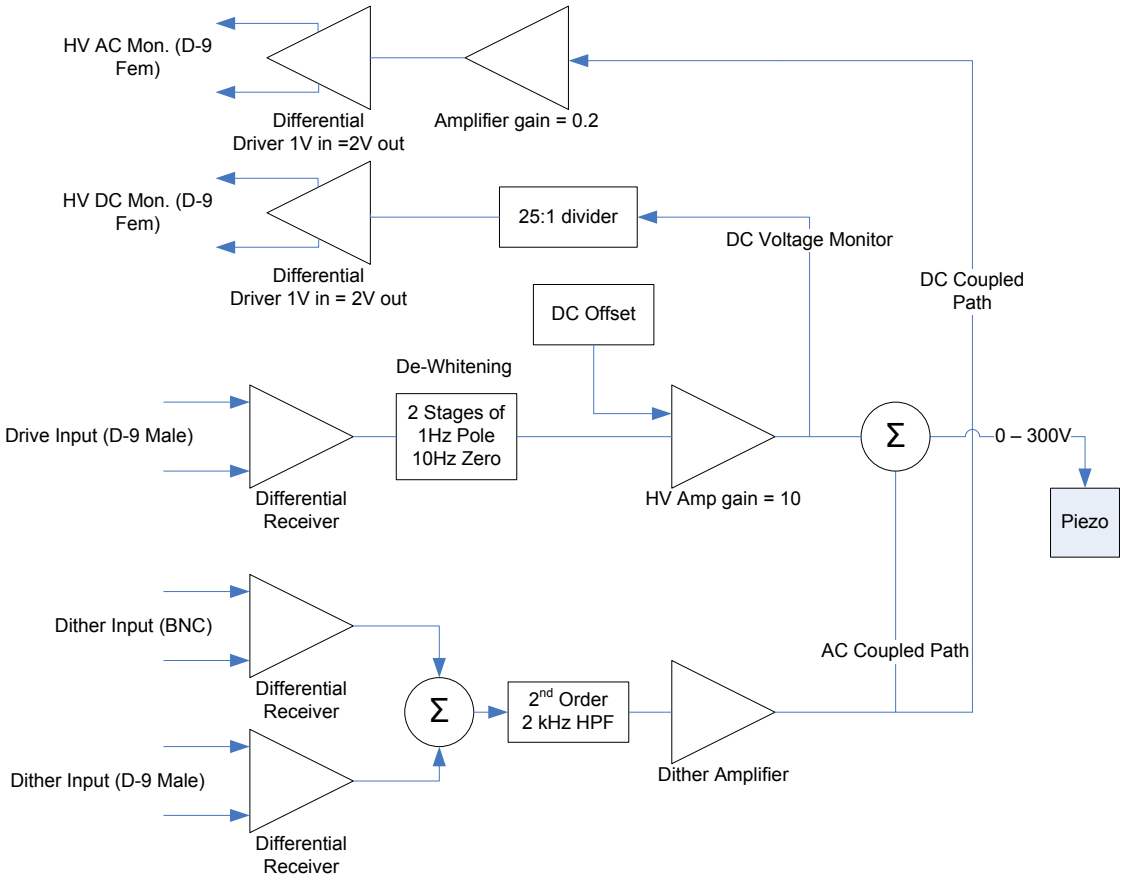
2.4. The required **high voltage power supply** is up to 300 VDC +/- 5% with a current capacity of at least 10mA. The unit shipped to the squeezing experiment at MIT in March were set for a 150VDC power supply

2.5. The nominal **piezo load capacity** is 0.22 uF +/- 20%, but there is no real restriction due to damage provided the user is aware of the circuit output impedance effects.

2.6. Detailed **electrical schematics** are available in LIGO document D060283-B

3. **Figure 1** shows an overview of the PZT Driver

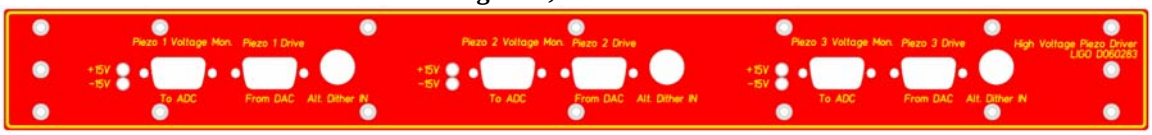
Figure 1



4. Figure 2 and Figure 3 show the front and rear of the PZT driver chassis. A functional description of each connector is provided.

### 4.1. **Front Panel diagram**

**Figure 2, Front Panel**




### 4.2. Front Panel Functions

4.2.1. **Piezo Voltage Mon** – Monitoring for the high voltage output. 1V at the DC monitor is 25V at the HV output. The other path is configurable, but the MIT prototype had a DC gain of 0.2 amplifier that was intended for looking at the dither signal. No internal filtering of signal on DC path.

4.2.2. **Alt. Dither IN** – A BNC input that provides an alternate path for injecting a 2 kHz to 20 kHz modulation signal used to dither-lock a particular axis. Path includes a second order, 2 kHz high-pass filter.

4.2.3. **Piezo Drive** – A D-9, male input for differential voltage drive to the OMC Length Piezo. Two DAC output channels are interfaced by this connector.

4.2.3.1. One channel is used for the length-control function, and other channel is used for a dither function at higher frequencies (identical to section 4.2.2 for the BNC dither input).

4.2.3.2. A 1 volt signal at this input changes the voltage across the piezo by 20 volts. The quiescent high voltage output voltage drive rests at 150V +/-5% when there is no input (0V).

4.2.3.3. A de-whitening filter consisting of 2 poles at 1 Hz and 2 zeros at 10 Hz is included in this path.

4.2.3.4. The current at each HV output is limited internally to 4mA +/- 5%, and is short-circuit-protected.

4.3. **Rear Panel Diagram**

**Figure 3, Rear Panel**


4.4. Rear Panel Functions

4.4.1. **DC IN** – A three terminal input in a D-15 shell. This input supplies the DC power to the chassis. The nominal input is +/- 18 VDC @ 0.2 amps, but a range from +/- 16 to +/- 24 VDC is acceptable. This range allows sufficient overhead for the internal low-dropout regulators, but is not so high as to cause a thermal dissipation issue with the regulators.

4.4.2. **+15 & -15 volt LEDs** – When lit, indicate the presence of DC power at the output of the internal regulator board. The power regulator has Poly-fuses that are rated at 2 amps. Cycling power to the chassis via the DC On/Off switch will reset the Poly-fuse provided the fault condition is clear

4.4.3. **DC On/Off** – Switch to turn power on and off. Switch removes power from the input of the power regulator board only.

4.4.4. **HV Output Signals** – D-25, female connector providing interface to three Piezos. ***Potentially lethal high voltages (150VDC) are present on this connector***. Extreme care must be employed when working with this connection. The signal pairings for Piezo 1,2 and 3 are pins 1/6, 2/7, 3/8 for +/- signals respectively.

4.4.5. **HV Input** – This is the high voltage power supply input to the chassis. Up to 300 VDC @ ≥10 mA is required. Pin 1 is positive, pin 2 is negative.