# LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY -LIGO-CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Document Type	DCC Number	Date	
Test Procedure and Results	LIGO-T0900346-v2	16 July, 2009	
STS-2 Seismometer Chassis Test Procedure			
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### LIGO-T0900346-v1

Performed by:	
Date:	
Board Serial Number:	_

### 1. Overview

The HEPI STS-2 Seismometer Interface Chassis provides power and control channels for a single STS-2 seismometer. The chassis receives 6 differential signals from the seismometer that are sent as outputs to the AdL Anti-Alias Chassis for ultimate transmission to the ADCs. A summary of functions for the STS-2 Seismometer Interface are:

- 1.1 DC power to the remotely located STS-2 seismometer
- 1.2 Receives 6 channels of differential signals from the STS-2 seismometer
- 1.3 Interfaces analog signals to the AdL Anti-Alias Chassis by differential interface
- 1.4 Provides local front panel switches and remote PCIX based control of STS-2 functions

The function of this procedure is to check each channel from its input to the respective output, test binary controls and to verify proper DC power consumption.

### 2. Test Equipment

- **2.1** Power Supply capable of +/- 18 volts
- **2.2** Function generator (Stanford Research DS360 or the like)
- 2.3 Oscilloscope

## 3. Preliminaries

- **3.1** Perform visual inspection on board to check for missing components or solder deficiencies
- **3.2** Before connecting the power to the chassis, set power supplies to +/- 18 Volts, and then turn them off. Connect the power supplies to the chassis under test at the back panel 3-pin power connector.

#### 4. DC Tests

**4.1** Turn on the power supplies to the system under test and record the total current. The specification assumes all inputs are not driven and the front panel switches are clicked down.

Total Current	Specification	Observation
+18V Supply	110mA +/- 10mA	
-18V Supply	100mA +/- 10mA	
Power LEDs	Lit with equal brightness	

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### 5. Dynamic Tests

- **5.1** The following tests verify the proper gain, for each signal channel. The test consists of applying a 100 Hz signal to test the channel gain
- **5.2** Using a function generator and an oscilloscope, enter **0.1V** p-p (**HI-Z**) sine wave on the function generator and apply to the prescribed input and observe the amplitude at the designated output (either the Anti Alias signals on J7, the onboard testpoints, or the front panel BNC). For differential outputs, use two scope probes in "differential mode" that is probe 1 minus probe 2.

SIS-2 Response Data			
INPUT	OUTPUT	NOMINAL	MEAS. MAG.
(+, -)	POINTS	<b>MAG (100HZ)</b>	(100HZ)
50 pin D-sub	STS2-X,	Pins 4&12: 4V p-p	Pins 4&12:
pin 3/36	J7 pins 4&12	+/- 0.5V	
or TP15/TP14	or TP4&TP12		BNC:
	& X-MON BNC	BNC: 2v p-p +/-0.5V	
50 pin D-sub	STS2-Y,	Pins 5&13: 4V p-p	Pins 5&13:
pin 20/4	J7 pins 5&13	+/- 0.5V	
or TP15/TP14	or TP4&TP12		BNC:
	& Y-MON BNC	BNC: 2v p-p +/-0.5V	
50 pin D-sub	STS2-Z,	Pins 6&14: 4V p-p	Pins 6&14:
pin 37/21	J7 pins 6&14	+/- 0.5V	
or TP15/TP14	or TP4&TP12		BNC:
	& Z-MON BNC	BNC: 2v p-p +/-0.5V	

**STS-2 Response Data** 

**5.3** Enter **10V** p-p (**HI-Z**) on the function generator and use only the positive output relative to GND. This requires referencing the common of the function generator to STS-2 GND.

INPUT	OUTPUT	NOMINAL	MEAS. MAG.
(+, -)	POINTS	MAG (100HZ)	(100HZ)
50 pin D-	MASSPOS-U	Pins 1&9: 20v p-p	Pins 1&9:
sub pin	J7 pins 1&9	+/- 0.5v	
41/GND	TP2&TP3		BNC:
	BNC U/X Pos	BNC: 10V +/- 0.5V	
50 pin D-	MASSPOS-V	Pins 2&10: 20v p-p	Pins 2&10:
sub pin	J7 pins 2&10	+/- 0.5V	
8/GND	TP2&TP3		BNC:
	BNC V/Y Pos	BNC: 10V +/- 0.5V	
50 pin D-	MASSPOS-W	Pins 3&11 20v p-p	Pins 3&11:
sub pin	J7 pins 3&11	+/- 0.5V	
24/GND	TP2&TP3		BNC:
	BNC W/Z Pos	BNC: 10V +/- 0.5V	

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5.4 Using a piece of cable to short the indicated pins together, or by actuating the front panel switches, verify the operation of the following binary functions (FP indicates Front Panel, RP indicates Rear Panel). For the rear panel (Binary I/O) functions to operate normally, it is necessary to have all the front panel toggle switches toggled down:

INPUT	OUTPUT	EXPECTED RESPONSE	ACTUAL RESPONSE
CAL switch from	CAL LED, J6	LED is lit, J6 pin 38 = 15V	
NORM to CAL			
FP			
Basis switch from	J6 pin 22	Transition from 0 to 15V	
XYZ to UVW <b>FP</b>			
Period switch	J6 pin 6	Transition from 0 to 15V	
from 120SEC to			
1SEC <b>FP</b>			
Push AZ button	AZ LED, J6	LED is lit, J6 pin $5 = 15V$	
FP			
Binary I/O	CAL LED, J6	LED is lit, J6 pin 38 = 15V	
Interface			
pin 1 to 6 <b>RP</b>			
Binary I/O	J6 pin 22	Transition from 0 to 15V	
Interface	UVW		
Pin 2 to 7 <b>RP</b>			
BinaryI/O	J6 pin 6	Transition from 0 to 15V	
Interface	PERIOD		
pin 3 to8 <b>RP</b>			
Bin I/O Interface	AZ LED, J6	LED is lit, J6 pin 5 = 15V	
pin 4 to 9 <b>RP</b>			