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PUM Drive Unit Design Description

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of the Advanced LIGO Project, prepared by members of the UK team.

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DESIGN AND MANUFACTURE OF THE PUM DRIVER UNIT

CONTENTS

1. INTRODUCTION

This document describes the philosophy and methods used to produce the PUM Coil Drive Electronics Unit for Advanced LIGO. Estimates of the performance are given, together with performance measurements from the pre-production units.

1.1 Context

The PUM Driver unit contains four channels of amplification and filtering. The outputs from the unit control the position of the PUM stage in the Advanced LIGO Quad Suspension.

The output currents from the unit energise four coils which attract magnets mounted on the PUM section of the suspension, giving a force which moves the PUM section to the desired position.

Protection circuits are incorporated to protect the OSEMs against prolonged over current situations.

Monitoring circuits are also included in the unit to monitor its activity. The monitor circuits are housed on a separate PCB within the unit.

2. MONITORS

2.1 Specification

The specification [1] requires the following circuits:-

(1) Output voltage monitors which cover the full dynamic range of the outputs.

(2) Monitors capable of seeing the noise floor of the outputs for 10Hz<freq<1 KHz

(3) Monitors of fast instantaneous measurement of the output current.

(4) Monitors of the RMS current with a time constant of 1 second capable of monitoring the full current range of the drivers

(5) Status (position) monitors/read backs for all switches used in the design.

2.2 Monitors Provided

(1) The Output Voltage Monitor. A monitor which measures the voltage between the two output operational amplifiers is provided. It has a gain of 1/3, so the highest possible output voltage within the constraints of the power rails (+/- 15v) gives a monitor output of 10v.

(2) The Noise Monitor. This is a high gain AC coupled amplifier with a low noise front end. The corner frequency of each of the stages is 5 Hz.

(3) The Output Current monitor. This is a four input summing amplifier which measures the sum of the voltages across the two output resistors. It has a gain of 1/3.

(4) The R.M.S monitor. A true RMS integrated circuit is used to convert the output of the current monitor into an RMS value. Its overall gain is 1, which combined with the current monitor gain, gives an overall gain of 1/3.
The settling time of this circuit varies with the applied input voltage.
The outputs from the r.m.s circuit are used as the inputs to the protection circuit, as the heating effect in the OSEM depends on the r.m.s current flowing through them.

(5) Status outputs for all switches. In the case of the filter relay, a spare relay contact is used to indicate the position of the relay. In the case of the test relay, all the contacts on the relay are already used, so a transistor circuit was added to monitor the state of the test relay coil voltage.

2.3 Monitor Design Details

2.3.1 Voltage Monitor

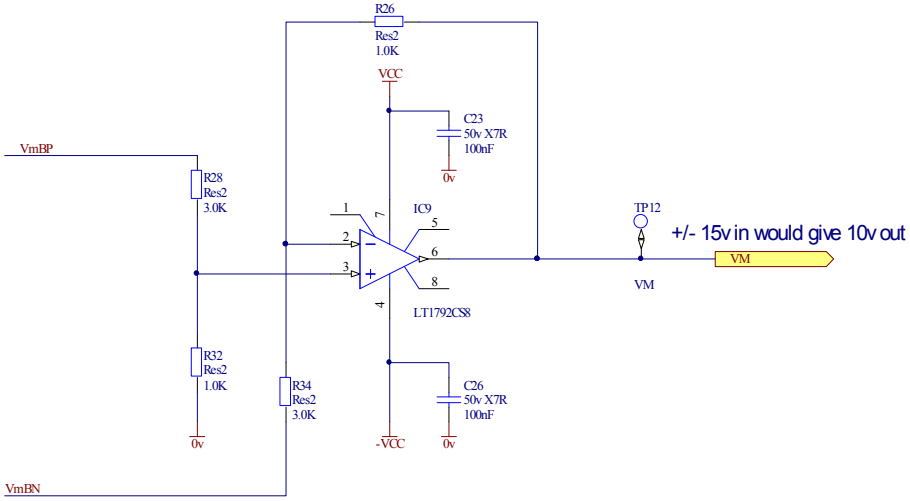

Fig 1 The Voltage Monitor Circuit

The Voltage Monitor Circuit consists of a summing amplifier, which subtracts the positive amplifier output from the negative amplifier output. This gives the total output voltage. The voltage gain of the circuit is ⅓ , which means that if the inputs are at their maximum voltage, +/-15v (rail voltage) the output is +10v.
There is one Voltage Monitor circuit per Drive Amplifier channel.

2.3.2 Current Monitor and R.M.S Circuit
Current Monitor

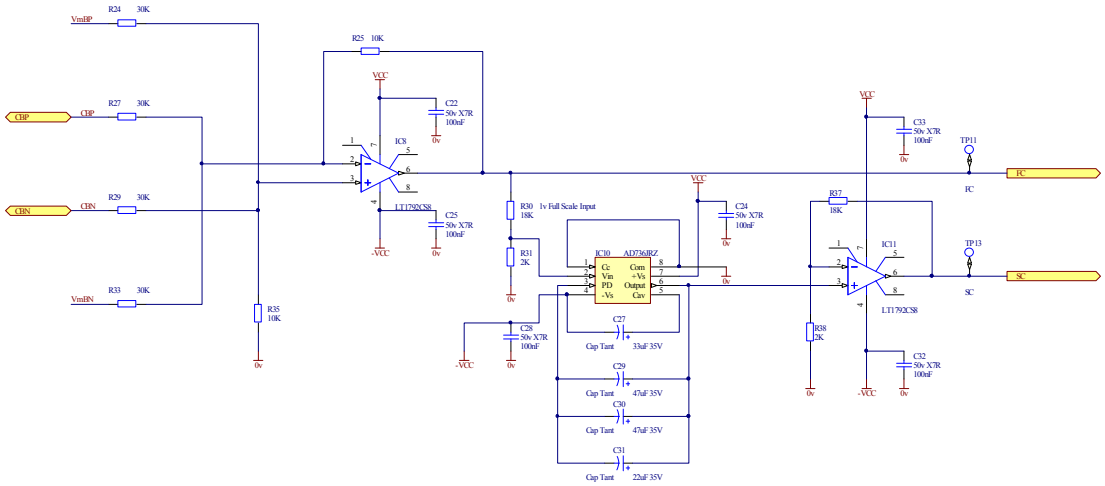

Fig 2 The Current Monitor and RMS circuit

The Current Monitor section consists of a 4 input Summing Amplifier. This calculates the voltages across the two output resistors, as this is proportional to the instantaneous output current. The sum performed is:

(Pos. Amplifier Output – Pos. Coil Voltage) + (Neg. Coil Voltage - Neg. Amplifier Output).

The gain of the amplifier is set to ⅓, which means that if the inputs are at their maximum possible voltage, the output is +10v.

1 volt out of the current monitor represents 1.5 volts across each driver output resistor.
As the output resistors are each 15 Ohms, this represents a current of 100mA. An output current of 10mA would therefore give a current monitor voltage of 150mV.

RMS Circuit

The r.m.s circuit uses a true r.m.s convertor integrated circuit type AD736, to convert the output signal from the Current Monitor into an r.m.s measurement. As large signals into the AD736 results in a reduced accuracy, the circuit is preceded by a 10:1 attenuator and followed by a 10x gain stage. This gives the r.m.s circuit the same overall gain as the current monitor. The settling time of this circuit varies with the applied voltage:

IC Input Voltage	Output from the Amplifier	Settling time
10mV	0.1 volt	1 Second
100mV	1 volt	100milliseconds
1V	10 volts	10 milliseconds

There is one current monitor and r.m.s circuit per Drive Amplifier channel, and there are four channels in each PUM Drive Unit.

2.3.3 Noise Monitor

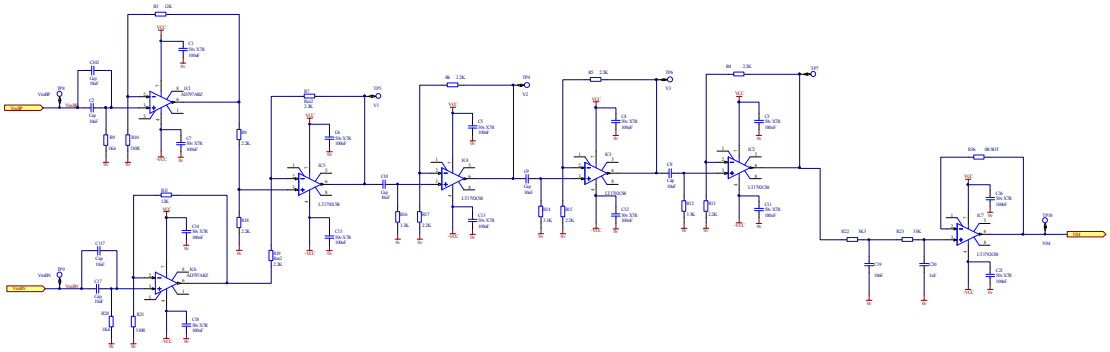

Fig 3 The Noise Monitor circuit

The Noise Monitor circuit is designed to amplify the ac noise voltage across the Drive Amplifier output, while rejecting dc signals.

An ac coupled, low noise differential amplifier front end is followed by a series of 3 gain stages, each ac coupled. Each stage has a gain of 2, and a corner frequency of 5Hz. These high pass stages are followed by a two pole low pass filter stage, each stage having a corner frequency of 5 KHz.

3. COIL DRIVE CIRCUITS

3.1 Specification

3.1.1 Input Signals
The specification [1] defines the following:

Input signals: Voltage Range: +/-10V ($20V_{p-p}$)
Noise Voltage: 100nV/√Hz over the frequency range of interest for the coil driver.

3.1.2 Noise requirements
The noise requirements depend on the operating mode.
In the RUN mode and SRD mode, the noise requirements are:

Frequency	Current Noise Requirement
1 Hz	20 nA/√Hz
10 Hz	4 pA/√Hz
100 Hz	5 nA/√Hz
1000 Hz	1000 nA/√Hz

In the acquisition mode, the noise requirements are not defined.

3.1.3 Dynamic Range
In the Run mode and SRD mode, the maximum output current for each PUM coil driver is required to be +/-16mA continuous between 200 Hz and 5 KHz. This is based on an output current of 800uA, with a safety margin of a factor of 20 to allow for current peaks. This specification applied between 200 Hz and 5 KHz

3.1.4 Protection Circuits
In the Acquisition Mode the noise requirements are not defined, but a continuous output current capability of 400mA is required. In addition the OSEMs need to be protected against excessive currents for extended periods, because excessive temperatures in the OSEM may cause unacceptable levels of out-gassing, and may damage the OSEMs.

4. COIL DRIVER DESIGN PHILOSOPHY

4.1 Dynamic range – Acquisition mode

Achieving the required dynamic range when in the Acquisition Mode requires a high current driver chip to supply the required continuous current of +/- 400mA. As switched mode operation is not suitable, the power dissipation of the output devices will be considerable. As noise is temperature dependant, the choice was made to limit temperature rises by conducting heat to the chassis via an aluminium bar.

Type OPA548 drivers are used. This device has a maximum continuous output current of 3 Amps. As only 400 mA is required, this leaves a large margin, which will make for reliable operation. The devices also features a current limit terminal, which is used to switch the driver off if excessive currents are drawn for prolonged periods. The device is housed in a convenient 7 lead TO220 package.

As driver devices are all fairly noisy, the OPA548 is enclosed in a feedback loop with an AD8671 low noise amplifier, to reduce the output noise. A bandwidth limiting compensating capacitor is connected in the feedback path of the AD8671 to ensure stability.

When the circuit is in Acquisition mode, the normal output network is bypassed by 50uF of capacitance, presenting a low impedance at high frequencies, and allowing the required drive of 400mA. The r.m.s current monitor signal is routed back from the monitor board to the protection circuit on the Drive board.

4.2 Dynamic range – Run or SRD mode

In Run or SRD mode, acquisition mode the relay is open, and the output impedance is greatly increased. This reduces the output noise while providing the lower output current required.

The output impedance in this mode consists of a 2.2K resistor in parallel with a 220 Ohm resistor in series with 5.5uF. This arrangement boosts the dynamic range at frequencies above 200 Hz.

4.3 Noise
The main difficulty in meeting the noise specification is the noise requirement at 10 Hz in the SRD mode. The noise level is required to be less than 4pA/√Hz.

Noise will emanate from several different sources.

The main noise sources are:
(1) Input noise
(2) Ground noise
(3) EMC
(4) Component Noise

(1) Input Noise
As a high dynamic range is required below 1 Hz, but a low noise level is required at 10Hz, input noise at 10 Hz is attenuated by means of a low pass filter stage. The filter stage may be remotely switched in or out as required, permitting a low noise mode or a high dynamic range mode to be selected.
The low pass filter incorporates a bypass capacitor which increases the dynamic range at 200 Hz and above. When the filter is switched out, the response becomes flat at all frequencies.

(2) Ground noise
Ground noise is always a problem in large complex low noise systems, particularly when there are long cable runs. LIGO is a very large, very complex system with extremely long cable runs, and very tight noise requirements.

This problem is avoided by keeping the signals independent of ground. As the input signals are symmetrical about ground, it is possible to engineer a true four wire system, by using two independent chains of amplifiers. This design also avoids any ground noise problems internal to the unit.

(3) EMC
EMC pick up on the amplifier outputs might also be a problem. The risk of this potential problem has been reduced, as the balanced outputs have identical output impedances. Any noise voltages induced by EMC should be almost entirely common mode, appearing equally across both coil terminals, and so resulting in no noise current in the coils.

(4) Component Noise
Component noise will be generated by all components in the unit. Resistors will unavoidably generate Johnson noise. Low noise metal film resistors are used in these units to minimise voltage dependant noise.

The operational amplifier types used in this design are carefully selected for their low noise specifications.

Ceramic capacitors are not used in the signal paths, as they are considered to be a possible source of microphonic noise.

5. DESIGN DETAILS
5.1 The Coil Drive Circuit

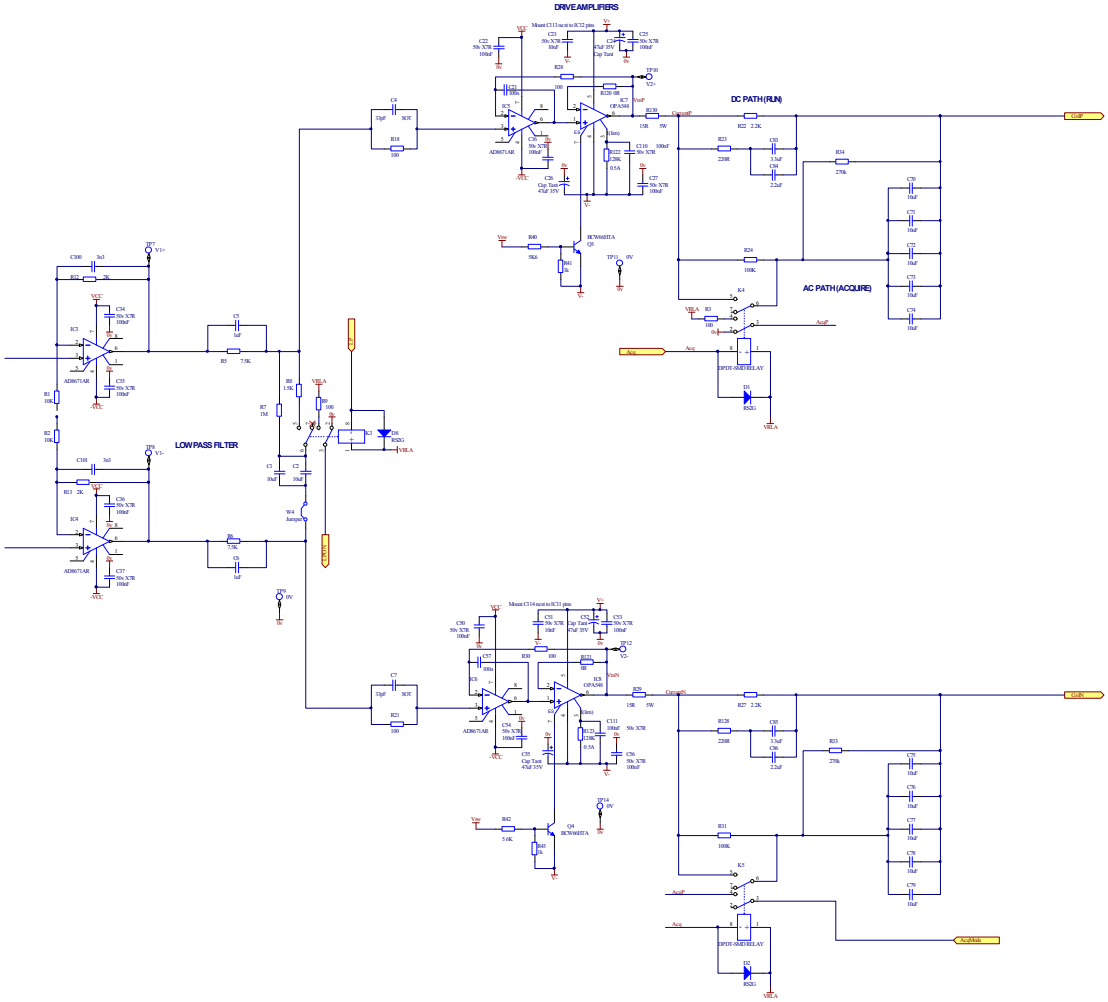

Fig 4 A PUM Driver Channel.

The above diagram shows the active section of a channel of a PUM Driver. There are four such channels in each PUM Driver Unit.

The circuit consists of a buffer amplifier with a gain of 1.2. This is followed by a switchable filter section, which behaves as a modified low pass filter with a 1 hz corner frequency. As the Requirements Document [(1),] specify, the pole in the filter is followed by a zero at 10 Hz.

This low pass filter is modified by the addition of a capacitor in parallel with the input resistor. When the filter is switched in, this increases the gain above 200 Hz. When the filter is switched out, both the low pass and high pass sections cease to operate, and the characteristic of the filter is essentially flat.

The output stage incorporates the circuitry needed for the Acquisition Mode, which is switched in place as required.

5.2 The Protection Circuit

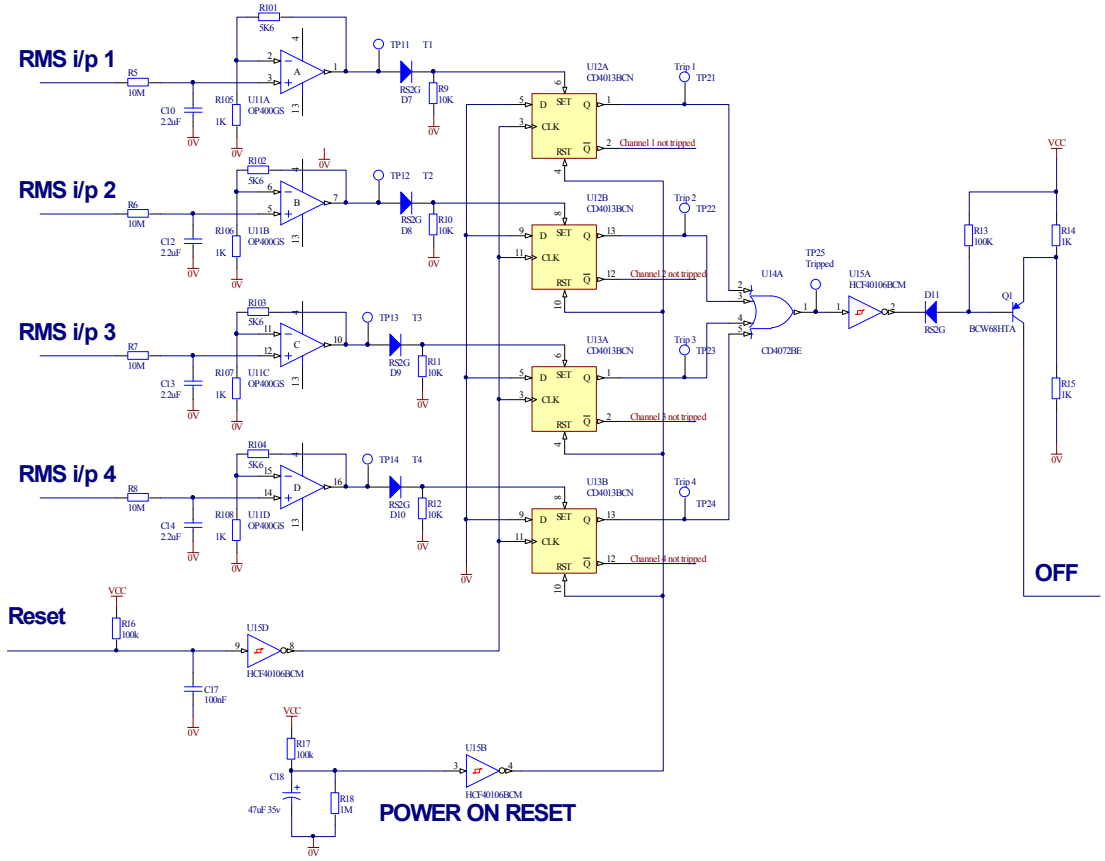

Fig 5 The Protection Circuit

The protection circuit is designed to shut down all the Drive circuits if the r.m.s current from any channel is too high for an excessive period. The over current circuits are latched to prevent oscillation. The latches may be reset by command, and are automatically reset at power on.

The protection circuit works as follows. The outputs from the r.m.s monitors are “integrated” by RC circuits. The “integrated” signal is then amplified and applied to the ‘set’ terminals of ‘D’ type flip-flop. If the threshold level of one of the flip-flop ‘set’ inputs is exceeded, its output becomes logic 1. The four flip flop outputs are combined in an OR gate which drives a transistor level shifter circuit. This then switches off the power drivers.

The state of the flip-flops may be monitored by telemetry. This feature allows the cause of tripping to be tracked down.

6. THEORETICAL PERFORMANCE

6.1. Dynamic range – Acquisition mode

During Acquisition mode, the output impedance of the circuit is effectively 15 Ohms in series with 50uF.

By simulation, the output current at 200 Hz with +/-10 volts applied to the amplifier input is 405 mA (assuming a LIGO OSEM).
This exceeds the 400mA requirement.

6.2 Dynamic range: Non – Acquisition Modes

When not in acquisition mode, the output impedance is 2K2 in parallel with 5.5uF and 220 Ohms in series.

6.2.1 Non – Acquisition Modes – filter switched out

By simulation, with the filter switched off, the output current is:

100 Hz	25.5 mA r.m.s
200 Hz:	33.9 mA r.m.s
1 KHz:	40.1 mA r.m.s
5 KHz	40.4 mA r.m.s

This exceeds the 16mA at 200 Hz – 5 KHz requirement.

6.2.2 Non – Acquisition modes – filter switched in

With the filter stage switched in, the current will be:

100 Hz	10.1 mA r.m.s
200 Hz	22.3 mA r.m.s
1 KHz	39.0 mA r.m.s
5 KHz	40.3 mA r.m.s

This exceeds the 16mA at 200 Hz – 5 KHz requirement.

6.3 Noise

The permitted noise current at 10 Hz is 4 pA/√Hz in the non-acquisition mode.

(1) Input Noise

According to the specification, the input noise is 100 nV/√Hz.

By simulation, the attenuation of the first stage at 10 Hz is 0.133.

The differential output noise voltage resulting from the input noise is therefore 100 nV/√Hz x 0.133 = 13.3 nV/√Hz.

The effective total output impedance is 4.42 K (including the 20 Ohm OSEM)
The output noise current will therefore be:
13.3/4.42 = **3 pA/√Hz**

(2) Ground Noise
As already mentioned, each channel functions is a true 4 terminal system. The input signals are balanced about ground. The bias currents for the inputs to this circuit are supplied by the input signals, and each subsequent stage is biased by the previous one. The dc voltages to ground are therefore defined throughout the circuit.
As the signals are not referred to any other ground line, there is no possibility of noise from external grounds being injected into the system.
The test input should never be left floating, as this may result in large offsets in the Test Mode. Instead, a dummy connector must be used to terminate it, with all pins connected together. This grounds the inputs in Test Mode, as pin 5 on the test connector is connected to local power supply 0v.

(3) EMC noise
The enclosure will act as a Gaussian screen. The box, as supplied, is floating, as the grounding scheme should be decided on a system basis.

(4) Component Noise
Calculation of component noise show that the output noise current is:
2.327 pA/√Hz

∑ Input derived noise & Component noise
=> **3.8 pA/√Hz**

This is within specification.

More details are given in Appendix 1.

7. MEASURED PERFORMANCE

7.1 Dynamic Range-Acquisition Mode

The results of the Dynamic Range tests on PUM1 in Acquisition Mode follow:

100Hz

	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	296 mA		Not Specified
Ch2	296 mA		Not Specified
Ch3	296 mA		Not Specified
Ch4	296 mA		Not Specified

200Hz

	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	399.5 mA	**400mA**	Marginally low
Ch2	399.5 mA	**400mA**	Marginally low
Ch3	399.5 mA	**400mA**	Marginally low
Ch4	398 mA	**400mA**	Marginally low

1K Hz

	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	477 mA	**400mA**	Pass
Ch2	477 mA	**400mA**	Pass
Ch3	478 mA	**400mA**	Pass
Ch4	477 mA	**400mA**	Pass

5K Hz

	Io pk. (Vo/20)	Specification	Pass/Fail
Ch1	487 mA	**400mA**	Pass
Ch2	487 mA	**400mA**	Pass
Ch3	487 mA	**400mA**	Pass
Ch4	487 mA	**400mA**	Pass

Notes:

(1) The output at 100 Hz is not defined in the specifications.

(2) The readings at 200 Hz were marginally below the specification.

It would be possible to increase the gain of the amplifier marginally to bring the 200 Hz readings within specification. However the existing measurements might be considered to meet the specification for practical purposes.

7.2.1 Non-Acquisition Mode- with the filter switched out.

The results of the Dynamic Range tests on PUM1 in Non-Acquisition Mode with the filter switched out follow**:**

100Hz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	24.5 mA	Not Specified	
Ch2	24.5 mA	Not Specified	
Ch3	24.5 mA	Not Specified	
Ch4	24.5 mA	Not Specified	

200Hz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	32.5 mA	**16mA**	Pass
Ch2	32.5 mA	**16mA**	Pass
Ch3	32.5 mA	**16mA**	Pass
Ch4	32.5 mA	**16mA**	Pass

1KHz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	37.5 mA	**16mA**	Pass
Ch2	37.5 mA	**16mA**	Pass
Ch3	37.5 mA	**16mA**	Pass
Ch4	37.5 mA	**16mA**	Pass

5KHz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	37.5 mA	**16mA**	Pass
Ch2	38 mA	**16mA**	Pass
Ch3	38 mA	**16mA**	Pass
Ch4	38 mA	**16mA**	Pass

It will be seen that the specification is exceeded by a good margin.

7.2.2 Non-Acquisition Mode- with the filter switched in.

The results of the Dynamic Range tests on PUM1 in Non-Acquisition Mode with the filter switched in follow**:**

100Hz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	9.5 mA	Not Specified	
Ch2	9.5 mA	Not Specified	
Ch3	9.5 mA	Not Specified	
Ch4	9.5 mA	Not Specified	

200Hz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	20 mA	**16mA**	Pass
Ch2	20 mA	**16mA**	Pass
Ch3	21 mA	**16mA**	Pass
Ch4	20 mA	**16mA**	Pass

1KHz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	36.5 mA	**16mA**	Pass
Ch2	36.5 mA	**16mA**	Pass
Ch3	36.5 mA	**16mA**	Pass
Ch4	36.5 mA	**16mA**	Pass

5KHz

	Io r.m.s (Vo/20)	**Specification**	**Pass/Fail**
Ch1	37.5 mA	**16mA**	Pass
Ch2	38 mA	**16mA**	Pass
Ch3	38 mA	**16mA**	Pass
Ch4	38 mA	**16mA**	Pass

It will be seen that the specification is exceeded by a good margin.

7.3 Noise
Noise measurements were made as follows:

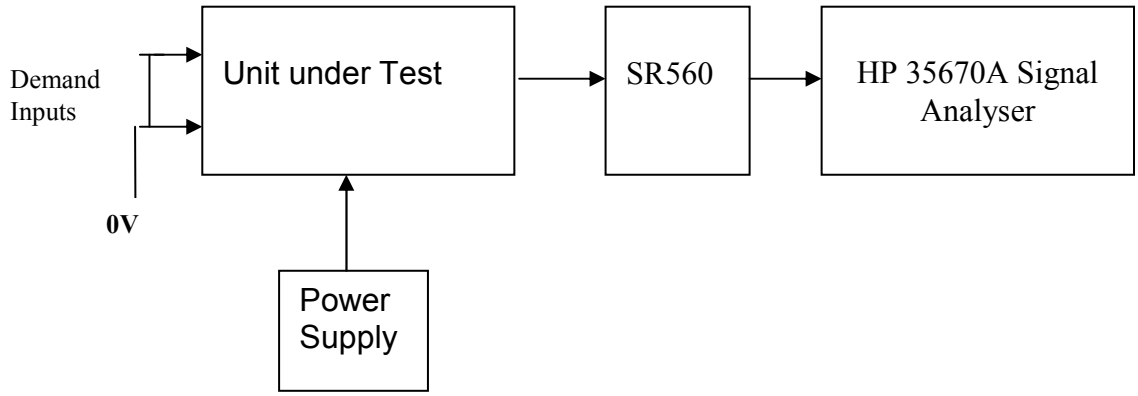

Fig 6 The PUM Noise Test Arrangement

The gain of the SR560 was set to 100, with a corner frequency of 100 Hz, and a roll off of 12 dB per decade. Readings were taken after 5pm when stray EMC was at a low level. Noise was measured at 10 Hz. Measurements were made on PUM1.

	Spec in dB V/√Hz	Measured @ 10Hz	-60dB =
Ch1	-155.1	-122 dB	-162 dB
Ch2	-155.1	-123 dB	-163 dB
Ch3	-155.1	-122 dB	-162 dB
Ch4	-155.1	-121 dB	-161 dB

All channels were measured as being well within specification.

Notes:
Specified noise output current at 10 Hz = 4pA/root Hz
Total resistance at 10Hz, in Low noise mode = 4.4K
Amplifier noise voltage should therefore be = 17.6 nV/√Hz
17.6 nV/√Hz = -155.1 dB/√Hz
The noise floor is about -133dB.

8. CONCLUSION
The PUM design has been shown to meet the requirements by simulation, and by measurements on the PUM1 unit.

9. REFERENCES
(1) T060067-00-C AdL Quad Suspension UK Coil Driver Design requirements

10. APPENDIX
Calculation of 10 Hz noise

First stage:
/side: AD8671 => Vn 2nV/√Hz
In 0.5nV/√Hz
10K||2k = 1.66 => 5.15 nV/√Hz

Total 5.55 /side: Total = 7.84 nV/√Hz

Filter attenuation = 0.133

=> Effective differential first stage noise = **1.04 nV/√Hz**

Filter:
1.5K gives 4.89 nV/√Hz
7.5K x 2 => 15K => 15.5 nV/√Hz
Noise current = 1.033 pA/√Hz
Into 1.5K => 1.55 nV/√Hz
Filter total @ 10 Hz = **5.13 nV/√Hz**

Output Stage:
/side: AD8671 => Vn 2nV/√Hz
In 0.45nV/√Hz
=> 2.05 nV/√Hz /side
=> **2.9 nV/√Hz** total

Total noise voltage out therefore equals:
6 nV/√Hz
Through 4.42 K gives **1.357 pA/√Hz**

Output resistor noise:
4.4k gives 8.39 nV/√Hz
=> a noise current of **1.89 pA/√Hz**

Total noise due to components therefore =
2.327 pA/√Hz

Input noise & component noise =>
∑ Input derived noise & Component noise
=> **3.8 pA/√Hz**