LIGO Laboratory / LIGO Scientific Collaboration

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UIM Coil Driver Board Test Plan

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This is an internal working note
of the Advanced LIGO Project, prepared by members of the UK team.

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UIM COIL DRIVER BOARD
TEST PLAN

Unit……Serial No ……
Test Engineer ……
Date ……

Contents

1. Description

The UIM Driver will be used to control the mirror position in the Advanced LIGO Gravity wave experiment.

It controls the current in the coil which provides the magnetic force which controls the position of the UIM mirror in a Quad assembly. It works in conjunction with the OSEM coil and position sensor units. One UIM board controls four OSEMs.

The UIM Coil Drive Board is mounted, together with a monitor board, inside a UIM unit.

The UIM Driver board also passes the amplified signals from the Photodiodes which detect the position of the UIM mirror back to the control electronics without processing them in any way.

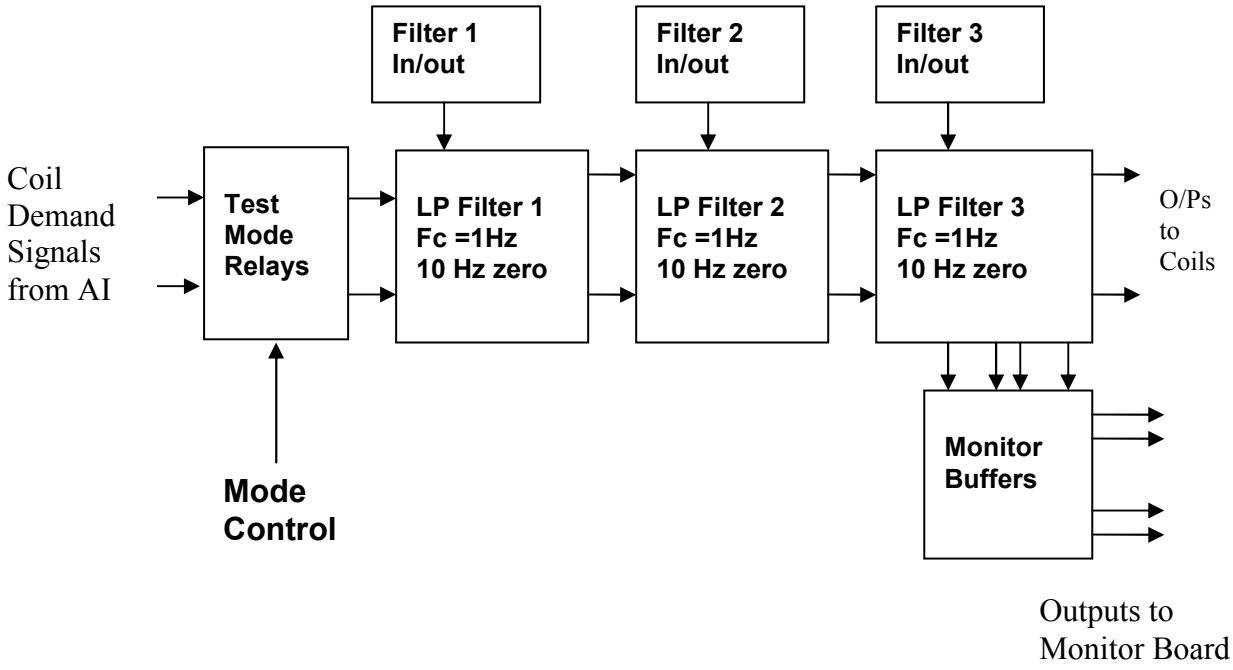

FIG. 1 UIM Driver Channel Block Diagram

Each UIM Driver board consists of four identical channels, one of which is shown above. Three power regulators (not shown), which provide regulated power to the four channels, are also mounted on the board.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. The forth block is again similar, except that it has a gain of 0.248. The overall gain of the UIM driver is 1.2. The extra gain is needed to compensate for the losses in the switching circuits due to the 1 megohm bypass resistors and associated capacitors.

Finally, the outputs from the driver stage, and the voltage across the coil, are buffered by unity gain voltage followers before being fed to the monitor circuit.

Each filter may be switched in and out as required by its own control relay, and a talkback signal confirms the position of each relay.

A Test Mode relay is provided on the front end which enables the amplifier inputs to be switched to a Test input.

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2. Test Equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment:

Links:

Check that links W3, W4 and W5 are present. If not, connect them.

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4. Continuity Checks

Use a multi-meter to check the connections below exist

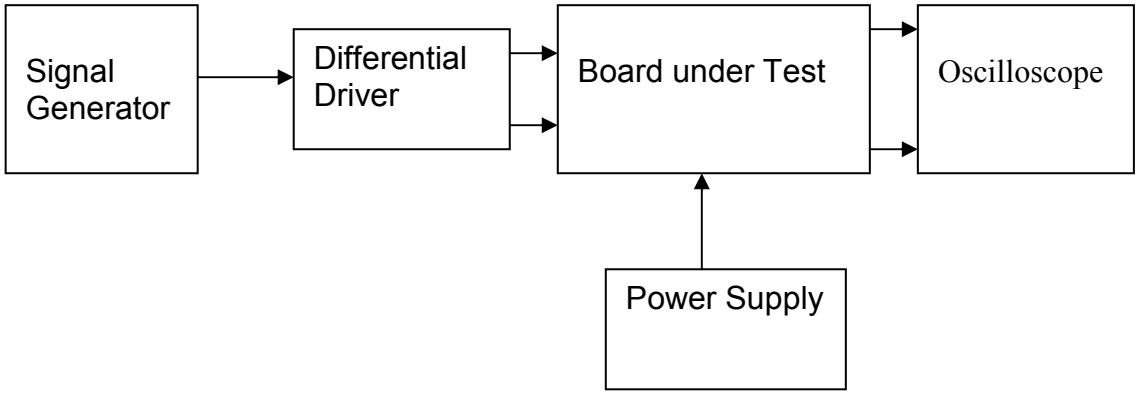
J2 PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	
2	PD2P	Photodiode B+	2	
3	PD3P	Photodiode C+	3	
4	PD4P	Photodiode D+	4	
5	0V			
6	PD1N	Photodiode A-	14	
7	PD2N	Photodiode B-	15	
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	

J5 PIN	SIGNAL	Monitors:	To J1 PIN	OK?
1	Imon1P	Current Source 1+	5	
2	Imon2P	Current Source 2+	6	
3	Imon3P	Current Source 3+	7	
4	Imon4P	Current Source 4+	8	
5	0V			
6	Imon1N	Current Source 1-	18	
7	Imon2N	Current Source 2-	19	
8	Imon3N	Current Source 3-	20	
9	Imon4N	Current Source 4-	21	

Power Supply to Satellite box

J1 PIN	SIGNAL	DESCRIPTION	OK?
9	V+	+17v Supply	
10	V+	+17v Supply	
11	V-	-17v Supply	
12	V-	-17v Supply	
13	0V	Return	
22	0V	Return	
23	0V	Return	
24	0V	Return	
25	0V	Return	

5. TEST SET UP



Note:
(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground

Power
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v

Outputs

Ch1+ = J4 pin 1	Ch1- = J4 pin 9
Ch2+ = J4 pin 3	Ch2- = J4 pin 11
Ch3+ = J4 pin 5	Ch3- = J4 pin 13
Ch4+ = J4 pin 7	Ch4- = J4 pin 15

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6. Power

Check the polarity of the wiring: 3 Pin Power Connector

Set the power supply outputs to zero.
Connect power to the unit
Increase the voltages on the supplies to +/-3V.
Determine that the supply polarities are correct.
Increase input voltages to +/- 16.5v.
Record the output voltage, measured on a 4 digit DVM, from each regulator
Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

Regulator	Test Point	Output voltage	Noise p/p
+12v	TP5		
+15v	TP4		
-15v	TP6		

All Outputs smooth DC, no oscillation?	

Record Power Supply Currents

Supply	Current
+16.5v	
-16.5v	

If outputs are satisfactory, (nominal +/- 0.5v), and there is no oscillation on any of the power rails, proceed to next section.

Check for Overheating.

Front Panel and monitor LEDs On?

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7. Relay Operation

Operate each relay stage in turn.
Observe its operation

Connect the test unit to J6 and J7.

Operate switches and see if LEDs are on when the relays are switched on, and off when they are switched off:

Relay	LED Operation					
	Filter 1		Filter 2		Filter 2	
	ON	OFF	ON	OFF	ON	OFF
Ch1						
Ch2						
Ch3						
Ch4						

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8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 0.1Hz.
Switch out all the filter stages.
Measure and record the Peak to Peak output between TP7 and TP11
At 1Hz, 10Hz and 100Hz for each channel

	1Hz	10Hz	100Hz	Specification	Pass/Fail
Ch1				4.8v to 5v	
Ch2				4.8v to 5v	
Ch3				4.8v to 5v	
Ch4				4.8v to 5v	

Switch in each filter in turn and measure, then again measure and record the output.
Repeat for 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz

0.1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1				4.9 to 5.1v	
Ch2				4.9 to 5.1v	
Ch3				4.9 to 5.1v	
Ch4				4.9 to 5.1v	

1Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1				3.3v to 3.7v	
Ch2				3.3v to 3.7v	
Ch3				3.3v to 3.7v	
Ch4				3.3v to 3.7v	

10Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1				0.48 to 0.75v	
Ch2				0.48 to 0.75v	
Ch3				0.48 to 0.75v	
Ch4				0.48 to 0.75v	

100Hz

	F1	F2	F3	Specification	Pass/Fail
Ch1				0.4v to 0.5v	
Ch2				0.4v to 0.5v	
Ch3				0.4v to 0.5v	
Ch4				0.4v to 0.5v	

1 KHz

	F1	F2	F3	Specification	Pass/Fail
Ch1				0.4v to 0.5v	
Ch2				0.4v to 0.5v	
Ch3				0.4v to 0.5v	
Ch4				0.4v to 0.5v	

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9. Monitor Outputs

Switch out the filters.
With a 3K9 dummy load on each channel, apply a 1v peak input at 10Hz and measure the differential output voltage between the monitor pins.

Channel	Monitor Connector	Parameter	Theoretical Value	Measured Value	Pass/ Fail
1	Pin 1 to Pin 2	Voltage Mon	4.9v to 5.1v		
	Pin 3 to Pin 4	Coil Mon	1.6v to 1.7v		
2	Pin 5 to Pin 6	Voltage Mon	4.9v to 5.1v		
	Pin 7 to Pin 8	Coil Mon	1.6v to 1.7v		
3	Pin 9 to Pin 10	Voltage Mon	4.9v to 5.1v		
	Pin 11 to Pin 12	Coil Mon	1.6v to 1.7v		
4	Pin 13 to Pin 14	Voltage Mon	4.9v to 5.1v		
	Pin 15 to Pin 16	Coil Mon	1.6v to 1.7v		

10. Distortion

No filters. Increase input voltage to 10v peak, f = 1KHz. Dummy 39 Ohm loads. Observe the voltage across each load with an analogue oscilloscope.

	Distortion Free?
Ch1	
Ch2	
Ch3	
Ch4	

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

	J3 pins 1,6		J3 pins 2,7		J3 pins 3,8		J3 pins 4,9	
	Ch1 o/p	Ch1 stable ?	Ch2 o/p	Ch2 stable ?	Ch3 o/p	Ch3 stable ?	Ch4 o/p	Ch4 stable ?
-10v								
-7v								
-5v								
-1v								
0v								
1v								
5v								
7v								
10v								

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12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		

12.2 Quick Test

Apply an input to each channel in turn from the signal generator, while grounding the unused channels. Monitor the other channel outputs using the HP Dynamic Signal Analyser.

INPUT CHANNEL	OUTPUT CHANNEL	Maximum Output	@ Frequency
Channel 1	Channel 2		
Channel 2	Channel 1		
Channel 2	Channel 3		
Channel 3	Channel 2		
Channel 3	Channel 4		
Channel 4	Channel 3		