LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

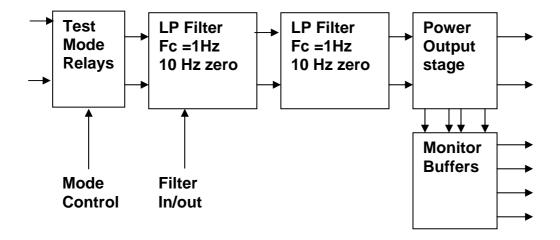
| Unit | Q_TOP46P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 9/3/10 | | |

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- 6. Power
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- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP46P | .Serial No |
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| | Xen | |
| Date | 9/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

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3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Also, replaced U3.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP46P | .Serial No |
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4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

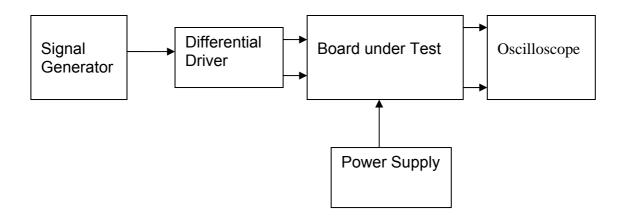
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|-----|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | |
| 4 | Imon4P | 8 | |
| 5 | 0V | | |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | V |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

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6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.01 | 1mV | |
| +15v TP4 | 14.91 | 1mV | |
| -15v TP6 | -15.06 | 5mV | V |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP46P | .Serial No |
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7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | $\sqrt{}$ |

Test Switches

| Channel | Indio | Indicator | |
|---------|-------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | $Q_{}$ | _TOP46P | Serial No | |
|---------------|--------|---------|-----------|--|
| Test Engineer | | | | |
| Date | | | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.35 | 3.3v to 3.7v | √ |
| Ch2 | 3.35 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.66 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.66 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.46 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | Q_TOP46P | Serial No |
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8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | √ |
| Ch2 | 0.48 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | √ |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | \checkmark |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP46P | .Serial No |
|------|----------|------------|
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9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.207 | Pin 1 to Pin 2 | 1.205 | |
| 2 | 1.16-1.28 | 1.206 | Pin 5 to Pin 6 | 1.205 | |
| 3 | 1.16-1.28 | 1.206 | Pin 9 to Pin 10 | 1.205 | |
| 4 | 1.16-1.28 | 1.206 | Pin 13 to Pin 14 | 1.205 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.398 | Pin 7 to Pin 8 | 0.398 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP46P | Serial No | |
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| Date | 9/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.4 | V | -24.3 | V | -24.3 | V | -24.3 | |
| -7v | -17.2 | V | -17.0 | V | -17.1 | V | -17.1 | V |
| -5v | -12.3 | V | -12.2 | V | -12.2 | V | -12.3 | V |
| -1v | -2.41 | V | -2.4 | V | -2.41 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.42 | V | 2.42 | V | 2.42 | $\sqrt{}$ | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.1 | V |
| 10v | 24.3 | V | 24.3 | V | 24.3 | V | 24.5 | √ |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP46P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 9/3/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|------------------|-----------|-----|-----------|--------------|
| Not Climping? | $\sqrt{}$ | V | $\sqrt{}$ | \checkmark |
| Clipping? | • | , | , | , |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.58 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.55 | V |

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

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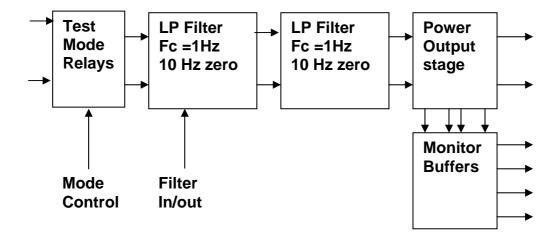
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Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1 Hz, followed by a complimentary zero at 10 Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1 Hz, the attenuation increases at a rate of 10dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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|----------------|---------|-----------|--|
| Test Engineer. | | | |
| Date | 21/1/10 | | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| Signal analyzer | Agilent | 35670A | |
| Pre-amplifier | Stanford Systems | SR560 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP1P | Serial No | |
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| Date | 21/1/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP1P | Serial No | |
|-------------|---------|-----------|--|
| Test Engine | erXen | | |
| Date | 21/1/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|------------------|--------------|-----|
| 1 | PD1P | Photodiode A+ | 1 | |
| 2 | PD2P | Photodiode B+ | 2 | |
| 3 | PD3P | Photodiode C+ | 3 | |
| 4 | PD4P | Photodiode D+ | 4 | |
| | 5 | 0V | \checkmark | |
| 6 | PD1N | Photodiode A- | 14 | |
| 7 | PD2N | Photodiode B- 15 | | |
| 8 | PD3N | Photodiode C- 16 | | |
| 9 | PD4N | Photodiode D- | 17 | |

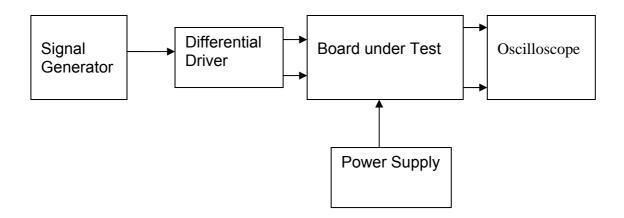
J5

| PIN | SIGNAL | | To J1 PIN | OK? |
|-----|--------|----|-----------|-----------|
| 1 | Imon1P | | 5 | |
| 2 | Imon2P | | 6 | |
| 3 | Imon3P | | 7 | $\sqrt{}$ |
| 4 | Imon4P | | 8 | |
| | 5 | 0V | √ | |
| 6 | Imon1N | | 18 | |
| 7 | Imon2N | | 19 | |
| 8 | Imon3N | | 20 | V |
| 9 | Imon4N | | 21 | V |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP1P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | | | |
| Date | 21/1/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| i to oo a roganatto. Oatpato. | | | | | |
|-------------------------------|----------------|--------------|-------------------|--|--|
| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? | | |
| +12v TP5 | 11.95 | 1mV | | | |
| +15v TP4 | 14.96 | 1mV | V | | |
| -15v TP6 | -14.98 | 5mV | V | | |

| All Outputs smooth DC, no oscillation? | | |
|--|--|--|
|--|--|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP1P | Serial No |
|---------------|---------|-----------|
| Test Engineer | | |
| Date | 21/1/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|----------|-----|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | $\sqrt{}$ | V | V |
| Ch4 | V | V | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|------|-----------|---|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | V |
| Ch3 | V | | V |
| Ch4 | | | V |

| Unit | Q_TOP1P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| | | | |

Date21/1/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|-----|------|-------|---------------|--------------|
| Ch1 | 4.8 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.8 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.8 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.8 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz, and 1KHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | V |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | |
| Ch2 | 0.66 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | V |

| Unit | Q_TOP1P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 21/1/10 | | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.25 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | √ |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | |
| Ch2 | 0.48 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | √ |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | √ |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP1P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 21/1/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 Ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.205 | Pin 1 to Pin 2 | 1.205 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.205 | Pin 5 to Pin 6 | 1.205 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.205 | Pin 9 to Pin 10 | 1.205 | \checkmark |
| 4 | 1.16-1.28 | 1.205 | Pin 13 to Pin 14 | 1.205 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.398 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.398 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz with dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | V |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP1P | Serial No |
|-------------|---------|-----------|
| Test Engine | erXen | |
| Date | 21/1/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | $\sqrt{}$ | -24.5 | |
| -7v | -17.1 | V | -17.2 | V | -17.2 | $\sqrt{}$ | -17.2 | |
| -5v | -12.2 | V | -12.3 | V | -12.3 | $\sqrt{}$ | -12.3 | V |
| -1v | -2.41 | V | -2.4 | V | -2.42 | $\sqrt{}$ | -2.42 | V |
| 0v | 0 | V | 0 | V | 0 | $\sqrt{}$ | 0 | V |
| 1v | 2.42 | V | 2.42 | V | 2.42 | \checkmark | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | $\sqrt{}$ | 12.2 | |
| 7v | 17.2 | V | 17.0 | V | 17.1 | $\sqrt{}$ | 17.0 | V |
| 10v | 24.5 | V | 24.5 | V | 24.5 | V | 24.5 | √ |

| Unit | Q_TOP1P | Serial No |
|-----------------|---------|-----------|
| Test Engineer . | Xen | |
| Date | 21/1/10 | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the outputs in dBs at 10Hz on adjacent channels. Record maximum output and the frequency at which this occurs (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|-------------|--------|
| Channel 1 | Channel 2 | -127dB | -114dB | 525Hz |
| Channel 2 | Channel 1 | -140dB | -113dB | 363Hz |
| Channel 2 | Channel 3 | -136dB | -113dB | 871Hz |
| Channel 3 | Channel 2 | -133dB | -111dB | 457Hz |
| Channel 3 | Channel 4 | -139dB | -111dB | 661Hz |
| Channel 4 | Channel 3 | -126dB | -109dB | 347Hz |

| Unit | Q TOP1P | Serial No |
|------|---------|-----------|
| | Xen | |
| Date | 21/1/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range.

Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|----------|
| Not | \checkmark | \checkmark | \checkmark | √ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

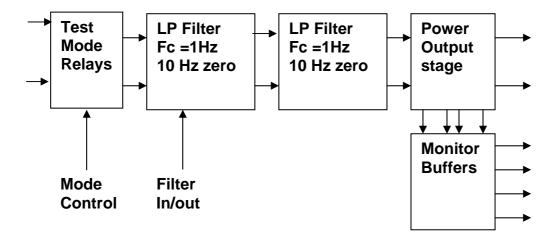
| Unit | .Q TOP1P | .Serial No |
|---------------|----------|------------|
| Test Engineer | .Xen | |
| Date | .28/1/10 | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
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- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP1P | .Serial No |
|---------------|---------|------------|
| Test Engineer | | |
| Date | 28/1/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q_TOP1P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 28/1/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP1P | Serial No | |
|-------------|---------|-----------|--|
| Test Engine | erXen | | |
| Date | 28/1/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | V |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | |
| | 5 | 0V | $\sqrt{}$ | |
| 6 | PD1N | Photodiode A- | 14 | V |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

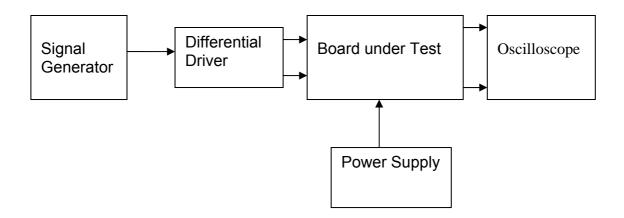
J5

| PIN | SIGNAL | | To J1 PIN | OK? |
|-----|--------|----|-----------|--------------|
| 1 | Imon1P | | 5 | \checkmark |
| 2 | Imon2P | | 6 | \checkmark |
| 3 | Imon3P | | 7 | \checkmark |
| 4 | Imon4P | | 8 | $\sqrt{}$ |
| | 5 | 0V | $\sqrt{}$ | |
| 6 | Imon1N | | 18 | \checkmark |
| 7 | Imon2N | | 19 | \checkmark |
| 8 | Imon3N | | 20 | $\sqrt{}$ |
| 9 | Imon4N | | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----|
| 9 | V+ (TP1) | +17v Supply | |
| 10 | V+ (TP1) | +17v Supply | |
| 11 | V- (TP2) | -17v Supply | |
| 12 | V- (TP2) | -17v Supply | |
| 13 | 0V (TP3) | | |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP1P | Serial No |
|---------------|---------|-----------|
| Test Engineer | Xen | |
| Date | 28/1/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | |
| +15v TP4 | 14.91 | 1mV | |
| -15v TP6 | -14.97 | 5mV | V |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP1P | .Serial No |
|---------------|----------|------------|
| Test Engineer | .Xen | |
| Date | .28/1/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | V | V | V |
| Ch4 | V | V | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|-----------|
| | ON | OFF | |
| Ch1 | √ | V | V |
| Ch2 | V | | |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | √ | √ | |

| Unit | Q TOP1P | Serial No | |
|---------------|---------|-----------|------|
| Test Engineer | Xen | | |
| Date | 28/1/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7 to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.35 | 3.3v to 3.7v | \checkmark |
| Ch4 | 3.4 | 3.3v to 3.7v | \checkmark |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP1P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .28/1/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.25 | 3v to 3.4v | |
| Ch2 | 3.2 | 3v to 3.4v | V |
| Ch3 | 3.2 | 3v to 3.4v | V |
| Ch4 | 3.2 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.46 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | √ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output Specification | | Pass/Fail |
|-----|----------------------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP1P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 28/1/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | V |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP1P | Serial No |
|-------------|---------|-----------|
| Test Engine | eerXen | |
| Date | 28/1/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.2 | V | -17.2 | V | -17.2 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | V |
| -1v | -2.42 | V | -2.42 | V | -2.42 | V | -2.42 | |
| 0v | 0 | V | 0 | $\sqrt{}$ | 0 | V | 0 | $\sqrt{}$ |
| 1v | 2.42 | V | 2.42 | V | 2.41 | V | 2.42 | V |
| 5v | 12.0 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.1 | V | 17.0 | V | 17.1 | V |
| 10v | 24.3 | V | 24.5 | V | 24.3 | V | 24.5 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP1P | Serial No |
|------|---------|-----------|
| | neerXen | |
| Date | 28/1/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.57 | |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.57 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

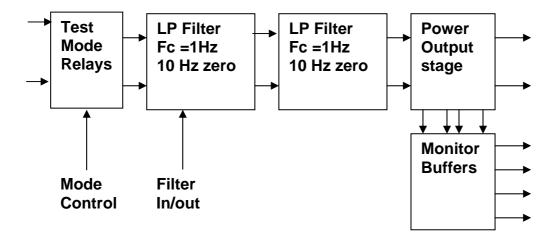
| Unit | .Q TOP3P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .28/1/10 | |

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- 2. Test Equipment
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- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP3P | .Serial No |
|---------------|---------|------------|
| Test Engineer | | |
| Date | 28/1/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP3P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | | | |
| Date | 28/1/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP3P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 28/1/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|------------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | √ |
| 4 | PD4P | Photodiode D+ 4 | | √ |
| | 5 | 0V √ | | |
| 6 | PD1N | Photodiode A- | 14 | |
| 7 | PD2N | Photodiode B- 15 | | |
| 8 | PD3N | Photodiode C- 16 | | √ |
| 9 | PD4N | Photodiode D- | 17 | √ |

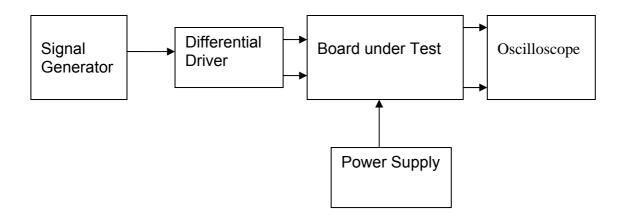
J5

| PIN | SIGNAL | | | To J1 PIN | OK? |
|-----|--------|----|---|-----------|--------------|
| 1 | Imon1P | | | 5 | \checkmark |
| 2 | Imon2P | | | 6 | \checkmark |
| 3 | Imon3P | | | 7 | \checkmark |
| 4 | Imon4P | | | 8 | $\sqrt{}$ |
| | 5 | 0V | | $\sqrt{}$ | |
| 6 | Imon1N | | | 18 | \checkmark |
| 7 | Imon2N | | | 19 | \checkmark |
| 8 | Imon3N | | | 20 | $\sqrt{}$ |
| 9 | Imon4N | | • | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | $\sqrt{}$ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP3P | Serial No | |
|------|---------|-----------|--|
| | erXen | | |
| Date | 28/1/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.79 | 1mV | \checkmark |
| -15v TP6 | -15.08 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | 1 | 1 |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP3P | Serial No |
|------|---------|-----------|
| | neerXen | |
| Date | 28/1/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|----------|-----------|---|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | | V |
| Ch3 | V | $\sqrt{}$ | |
| Ch4 | V | V | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|------|--------------|---|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | V |
| Ch3 | V | | |
| Ch4 | | \checkmark | |

| Unit | Q_TOP3P | Serial No | |
|-------------|---------|-----------|--|
| Test Engine | erXen | | |

Date28/1/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.35 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP3P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .28/1/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.2 | 3v to 3.4v | √ |
| Ch3 | 3.25 | 3v to 3.4v | V |
| Ch4 | 3.2 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP3P | Serial No | |
|-----------------|---------|-----------|------|
| Test Engineer . | Xen | | |
| Date | 28/1/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.399 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | √ |

| Unit | .Q TOP3P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | .28/1/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | V |
| -7v | -17.1 | V | -17.2 | V | -17.2 | V | -17.1 | V |
| -5v | -12.2 | V | -12.3 | V | -12.3 | V | -12.3 | V |
| -1v | -2.4 | $\sqrt{}$ | -2.42 | $\sqrt{}$ | -2.42 | $\sqrt{}$ | -2.4 | $\sqrt{}$ |
| 0v | 0 | √ | 0 | √ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.42 | \checkmark | 2.42 | $\sqrt{}$ | 2.4 | $\sqrt{}$ | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.1 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.1 | V |
| 10v | 24.4 | V | 24.5 | V | 24.3 | V | 24.5 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP3P | Serial No |
|------|---------|-----------|
| | neerXen | |
| Date | 28/1/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.57 | V |
| Ch4 | 5v to 6v | 5.57 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

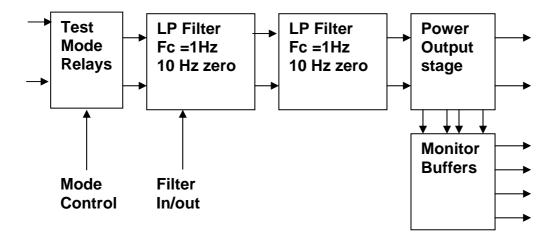
| Unit | Q TOP4P | Serial No |
|---------------|---------|-----------|
| Test Engineer | | |
| Date | | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q_TOP4P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | | | |
| Date | 29/1/10 | | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Unit (e.g. DVM) Manufacturer | | Serial Number |
|------------------|------------------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | .Q TOP4P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .28/1/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP4P | Serial No |
|------|---------|-----------|
| | neerXen | |
| Date | 28/1/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|------------------|-----------|-----|
| 1 | PD1P | Photodiode A+ | 1 | |
| 2 | PD2P | Photodiode B+ | 2 | |
| 3 | PD3P | Photodiode C+ | 3 | |
| 4 | PD4P | Photodiode D+ | 4 | |
| | 5 | 0V | $\sqrt{}$ | |
| 6 | PD1N | Photodiode A- | 14 | |
| 7 | PD2N | Photodiode B- 15 | | |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | V |

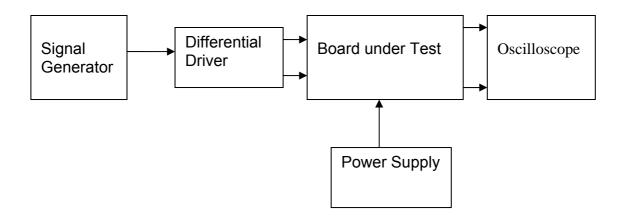
J5

| PIN | SIGNAL | | To J1 PIN | OK? |
|-----|--------|----|--------------|--------------|
| 1 | Imon1P | | 5 | \checkmark |
| 2 | Imon2P | | 6 | \checkmark |
| 3 | Imon3P | | 7 | \checkmark |
| 4 | Imon4P | | 8 | \checkmark |
| | 5 | 0V | \checkmark | |
| 6 | Imon1N | | 18 | \checkmark |
| 7 | Imon2N | | 19 | \checkmark |
| 8 | Imon3N | | 20 | V |
| 9 | Imon4N | | 21 | V |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP4P | Serial No |
|------|---------|-----------|
| | erXen | |
| Date | 28/1/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | √ |
| +15v TP4 | 14.81 | 1mV | √ |
| -15v TP6 | -15.04 | 5mV | √ |

| All Outputs smooth DC, no oscillation? √ |
|--|
|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP4P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .28/1/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----------|-----|
| | ON | OFF | |
| Ch1 | | | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | | $\sqrt{}$ | V |
| Ch4 | $\sqrt{}$ | | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|-----------|
| | ON | OFF | |
| Ch1 | √ | V | V |
| Ch2 | V | | |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | √ | √ | |

| Unit | Q_TOP4P | Serial No | |
|--------------|---------|-----------|--|
| Test Enginee | erXen | | |

Date28/1/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | 1 | Hz | |
|---|-----|----|--|
| v | ••• | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.35 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP4P | Serial No |
|---------------|----------|-----------|
| Test Engineer | .Xen | |
| Date | .28/1/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.25 | 3v to 3.4v | \checkmark |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | |
| Ch2 | 0.5 | 0.4v to 0.5v | |
| Ch3 | 0.49 | 0.4v to 0.5v | V |
| Ch4 | 0.49 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q_TOP4P | Serial No |
|---------------|---------|-----------|
| Test Engineer | Xen | |
| Date | 28/1/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | \checkmark |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.398 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | $\sqrt{}$ |
| Ch3 | $\sqrt{}$ |
| Ch4 | |

| Unit | Q_TOP4P | Serial No |
|-------------|---------|-----------|
| Test Engine | eerXen | |
| Date | 29/1/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | $\sqrt{}$ | -24.3 | $\sqrt{}$ | -24.3 | $\sqrt{}$ | -24.5 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.1 | V | -17.1 | V | -17.1 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.41 | V | -2.41 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.41 | V | 2.41 | V | 2.42 | V | 2.41 | $\sqrt{}$ |
| 5v | 12.1 | V | 12.1 | V | 12.2 | V | 12.1 | √ |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.2 | V | 24.3 | V | 24.3 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP4P | Serial No |
|------|---------|-----------|
| | erXen | |
| Date | 28/1/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|----------|--------------|-----|
| Not | \checkmark | √ | \checkmark | V |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | V |
| Ch3 | 5v to 6v | 5.57 | V |
| Ch4 | 5v to 6v | 5.57 | |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

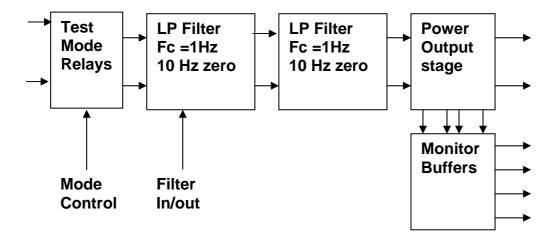
| Unit | .Q TOP5P | Serial No | |
|---------------|----------|-----------|------|
| Test Engineer | | | |
| Date | .29/1/10 | | |

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- 1. Description
- 2. Test Equipment
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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP5P | .Serial No |
|---------------|---------|------------|
| Test Engineer | | |
| Date | 29/1/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q_TOP5P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | | | |
| Date | 29/1/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP5P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 29/1/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

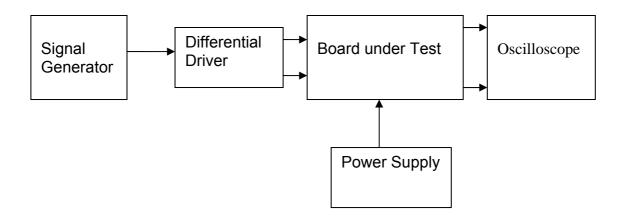
| PIN | SIGNAL | To J1 PIN | N OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | √ |
| 8 | Imon3N | 20 | V |
| 9 | Imon4N | 21 | √ |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | \checkmark |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP5P | Serial No | |
|------|---------|-----------|--|
| | erXen | | |
| Date | 29/1/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.07 | 1mV | √ |
| +15v TP4 | 14.91 | 1mV | √ |
| -15v TP6 | -15.05 | 5mV | √ |

| All Outputs smooth DC, no oscillation? √ |
|--|
|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP5P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 29/1/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | V |
| Ch3 | V | | V |
| Ch4 | $\sqrt{}$ | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|-----|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP5P | Serial No |) | |
|---------------|---------|-----------|---|--|
| Test Engineer | Xen | | | |

Date29/1/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | 1 | Ш- |
|---|---|-----|
| U | | 112 |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.35 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.66 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP5P | Serial No |
|---------------|----------|-----------|
| Test Engineer | .Xen | |
| Date | .29/1/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | V |
| Ch2 | 3.25 | 3v to 3.4v | |
| Ch3 | 3.25 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | √ |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.48 | 0.4v to 0.5v | |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP5P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 29/1/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | \checkmark |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | $\sqrt{}$ |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP5P | Serial No |
|------------|---------|-----------|
| Test Engin | eerXen | |
| Date | 29/1/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.4 | V | -24.5 | V |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.1 | V |
| -5v | -12.3 | $\sqrt{}$ | -12.3 | √ | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ |
| -1v | -2.42 | $\sqrt{}$ | -2.42 | √ | -2.42 | $\sqrt{}$ | -2.41 | $\sqrt{}$ |
| 0v | 0 | $\sqrt{}$ | 0 | √ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.41 | \checkmark | 2.42 | $\sqrt{}$ | 2.41 | $\sqrt{}$ | 2.42 | $\sqrt{}$ |
| 5v | 12.0 | V | 12.1 | V | 12.0 | V | 12.1 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.2 | V | 24.2 | V | 24.2 | V | 24.2 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP5P | Serial No | |
|------|---------|-----------|--|
| | ieerXen | | |
| Date | 29/1/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.57 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

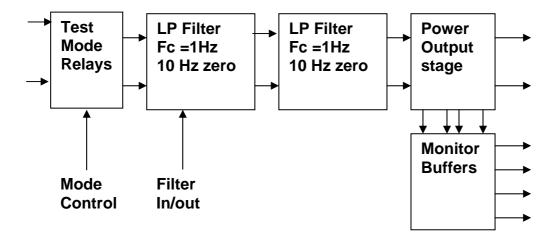
| Unit | Q TOP6P | Serial No |
|---------------|---------|-----------|
| Test Engineer | Xen | |
| Date | 1/2/10 | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP6P | .Serial No |
|---------------|----------|------------|
| Test Engineer | | |
| Date | 1/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP6P | Serial No |
|---------------|---------|-----------|
| Test Engineer | | |
| Date | 29/1/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP6P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 29/1/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

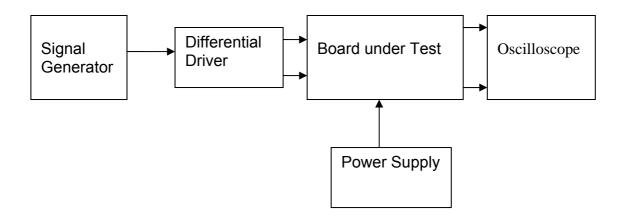
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | \checkmark |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | √ |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP6P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | ·Xen | | |
| Date | 1/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | \checkmark |
| +15v TP4 | 14.88 | 1mV | \checkmark |
| -15v TP6 | -15.03 | 5mV | \checkmark |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP6P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .1/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|-----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | $\sqrt{}$ | √ | √ |

Test Switches

| Channel | Indio | Indicator | |
|---------|-------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q TOP6P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 1/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 530 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | √ |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch/ | 1 85 | 4.7 to 5y | 1 |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.35 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP6P | Serial No |
|---------------|----------|-----------|
| Test Engineer | .Xen | |
| Date | 1/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | |
| Ch2 | 0.49 | 0.4v to 0.5v | |
| Ch3 | 0.48 | 0.4v to 0.5v | V |
| Ch4 | 0.49 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP6P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | Xen | | |
| Date | 1/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | \checkmark |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.399 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | .Q TOP6P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | .Xen | | |
| Date | .1/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.1 | V | -17.2 | V | -17.2 | V | -17.1 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.2 | |
| -1v | -2.4 | V | -2.41 | V | -2.42 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.1 | V | 17.0 | V | 17.0 | V |
| 10v | 24.5 | V | 24.5 | V | 24.3 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP6P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 1/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.57 | |
| Ch2 | 5v to 6v | 5.57 | V |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

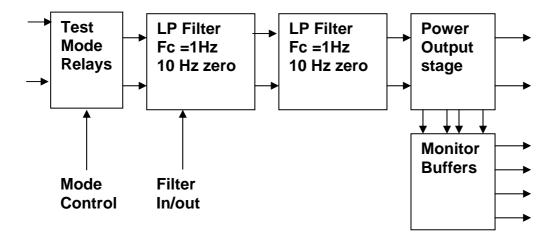
| Unit | .Q TOP7P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .1/2/10 | |

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- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP7P | .Serial No |
|---------------|----------|------------|
| Test Engineer | | |
| Date | 1/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP7P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | | | |
| Date | 1/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP7P | Serial No |
|------|---------|-----------|
| | neerXen | |
| Date | 1/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | √ |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

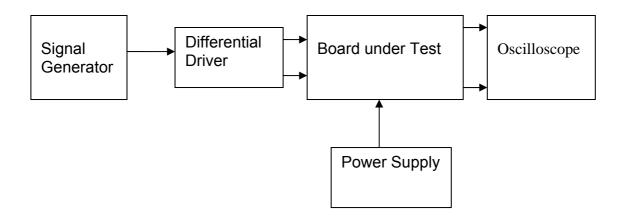
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | √ |
| 3 | Imon3P | 7 | √ |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | √ |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP7P | Serial No | |
|---------------|---------|-----------|--|
| Test Engineer | ·Xen | | |
| Date | 1/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.00 | 1mV | \checkmark |
| +15v TP4 | 14.78 | 1mV | \checkmark |
| -15v TP6 | -14.86 | 5mV | \checkmark |

| All Outputs smooth DC, no oscillation? √ |
|--|
|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP7P | Serial No |
|------|---------|-----------|
| | erXen | |
| Date | 1/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|---|
| | ON | OFF | |
| Ch1 | V | | |
| Ch2 | V | | |
| Ch3 | V | | V |
| Ch4 | | | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | V | V | V |
| Ch4 | V | V | V |

| Unit | Q TOP7P | Serial No | |
|-----------------|---------|-----------|------|
| Test Engineer . | | | |
| Date | 1/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | V |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4 85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch3 | 3.35 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.67 | 0.48 to 0.75v | \checkmark |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP7P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | 1/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.2 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch2 | 0.49 | 0.4v to 0.5v | V |
| Ch3 | 0.49 | 0.4v to 0.5v | V |
| Ch4 | 0.49 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q_TOP7P | Serial No | |
|---------------|---------|-----------|------|
| Test Engineer | Xen | | |
| Date | 1/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | \checkmark |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.397 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | .Q_TOP7P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | .Xen | | |
| Date | .1/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.4 | $\sqrt{}$ | -24.4 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.2 | V | -17.1 | V | -17.0 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.4 | V | -2.41 | V | -2.42 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.41 | V | 2.41 | V | 2.42 | |
| 5v | 12.2 | V | 12.0 | V | 12.0 | V | 12.2 | √ |
| 7v | 17.1 | V | 17.0 | V | 17.0 | V | 17.0 | √ |
| 10v | 24.3 | V | 24.2 | V | 24.2 | V | 24.2 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP7P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 1/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----|----------|
| Not Clipping? | $\sqrt{}$ | V | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.56 | |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

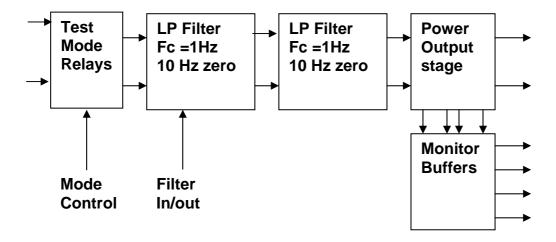
| Unit | .Q TOP8P | Serial No . | |
|---------------|----------|-------------|------|
| Test Engineer | | | |
| Date | .2/2/10 | | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
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- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP8P | .Serial No |
|---------------|----------|------------|
| Test Engineer | | |
| Date | 2/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP8P | Serial No |
|-----------------|---------|-----------|
| Test Engineer . | | |
| Date | 1/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Changed IC11, IC10 and IC5 on CH4.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP8P | Serial No |
|------|---------|-----------|
| | eerXen | |
| Date | 1/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

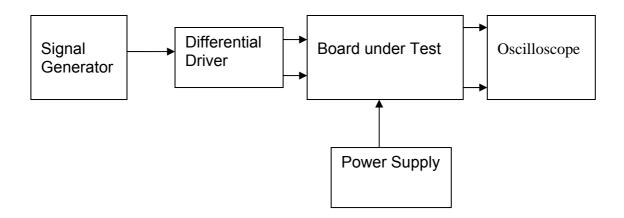
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | √ |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | √ |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP8P | Serial No | |
|--------------|---------|-----------|--|
| Test Enginee | erXen | | |
| Date | 2/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.07 | 1mV | |
| +15v TP4 | 14.93 | 1mV | |
| -15v TP6 | -14.89 | 5mV | |

| All Outputs smooth DC, no oscillation? | 1 | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP8P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .2/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|-----|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP8P | Serial No . | |
|-------------|---------|-------------|--|
| Test Engine | erXen | | |

Date2/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.3 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.66 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP8P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .2/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | |
| Ch2 | 0.5 | 0.4v to 0.5v | |
| Ch3 | 0.5 | 0.4v to 0.5v | V |
| Ch4 | 0.49 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP8P | Serial No |
|---------------|---------|-----------|
| Test Engineer | Xen | |
| Date | 2/2/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | \checkmark |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? | |
|-----|------------------|--|
| Ch1 | $\sqrt{}$ | |
| Ch2 | V | |
| Ch3 | V | |
| Ch4 | √ | |

| Unit | Q_TOP8P | Serial No |
|-------------|---------|-----------|
| Test Engine | eerXen | |
| Data | 2/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.2 | V | -17.2 | V | -17.0 | |
| -5v | -12.3 | V | -12.5 | V | -12.3 | V | -12.2 | |
| -1v | -2.42 | V | -2.42 | V | -2.4 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | √ |
| 7v | 17.0 | V | 17.1 | V | 17.2 | V | 17.0 | V |
| 10v | 24.3 | V | 24.5 | V | 24.5 | V | 24.3 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP8P | Serial No | |
|------|---------|-----------|--|
| | erXen | | |
| Date | 2/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|-----|-----|-----|-----|
| Not | | V | V | V |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | V |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.56 | V |

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LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

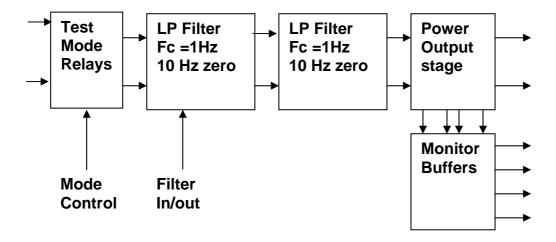
| Unit | Q TOP9P | Serial No |
|---------------|---------|-----------|
| Test Engineer | Xen | |
| Date | 3/2/10 | |

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- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP9P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .3/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP9P | Serial No |
|---------------|---------|-----------|
| Test Engineer | | |
| Date | 2/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP9P | Serial No |
|------|---------|-----------|
| | ieerXen | |
| Date | 2/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | $\sqrt{}$ |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | $\sqrt{}$ |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

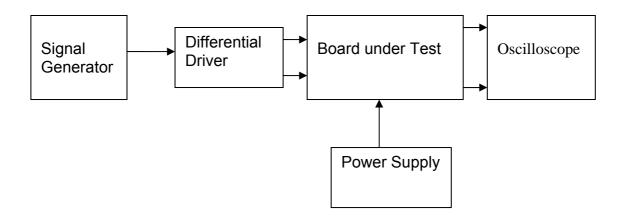
| PIN | SIGNAL | To J1 PIN | I OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | V |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | V |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP9P | Serial No | |
|------|---------|-----------|--|
| | erXen | | |
| Date | 2/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.05 | 1mV | |
| +15v TP4 | 14.89 | 1mV | |
| -15v TP6 | -15.06 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | 1 |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP9P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .2/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | V | V | V |
| Ch4 | | | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|--------------|---|
| | ON | OFF | |
| Ch1 | √ | | V |
| Ch2 | √ | | V |
| Ch3 | V | | V |
| Ch4 | | \checkmark | |

| Unit | .Q TOP9P | .Serial No |
|---------------|----------|------------|
| Test Engineer | | |
| Date | .2/2/10, | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | - 1 | Ш- |
|---|-----|-----|
| U | | 112 |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.35 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | |
| Ch4 | 3.35 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.66 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.46 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.46 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP9P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .2/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | V |
| Ch2 | 3.3 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | |
| Ch2 | 0.5 | 0.4v to 0.5v | |
| Ch3 | 0.5 | 0.4v to 0.5v | |
| Ch4 | 0.49 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP9P | Serial No |
|---------------|---------|-----------|
| Test Engineer | Xen | |
| Date | 2/2/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | √ |

| Unit | .Q TOP9P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .3/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ |
| -7v | -17.1 | $\sqrt{}$ | -17.2 | $\sqrt{}$ | -17.2 | $\sqrt{}$ | -17.2 | $\sqrt{}$ |
| -5v | -12.2 | $\sqrt{}$ | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ |
| -1v | -2.42 | $\sqrt{}$ | -2.4 | $\sqrt{}$ | -2.41 | $\sqrt{}$ | -2.41 | $\sqrt{}$ |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | \checkmark | 0 | $\sqrt{}$ |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | V |
| 5v | 12.1 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.4 | V | 24.4 | V | 24.3 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP9P | Serial No | |
|------|---------|-----------|--|
| | eerXen | | |
| Date | 2/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|-----------|-----|----------|--------------|
| Not | $\sqrt{}$ | √ | √ | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | V |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

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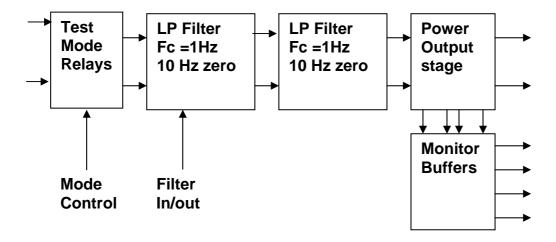
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| Test Engineer | | |
| Date | 4/2/10 | |

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Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| UnitC | TOP10P | Serial No |
|----------------|--------|-----------|
| Test EngineerX | | |
| Date4/ | /2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP10P | Serial No |
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| Date | 4/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

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Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP10P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 4/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

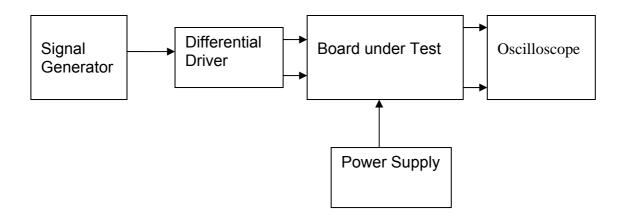
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | √ |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | √ |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP10P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .4/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.03 | 1mV | \checkmark |
| +15v TP4 | 14.82 | 1mV | \checkmark |
| -15v TP6 | -15.08 | 5mV | $\sqrt{}$ |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q_TOP10P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | .4/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|-----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | $\sqrt{}$ | √ | √ |

Test Switches

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | V | 1 | √ |

| UnitQ_10P1 | OPSerial No |
|------------------|-------------|
| Test EngineerXen | ••• |

Date4/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | - 1 | Ш- |
|---|-----|-----|
| U | | 112 |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | V |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.68 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP10P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .4/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | V |
| Ch2 | 3.3 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.5 | 0.4v to 0.5v | √ |
| Ch4 | 0.5 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP10P. | .Serial No | |
|-----------------|-----------|----------------|------|
| Test Engineer . | Xen | | |
| Date | 4/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | V |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | V |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP10P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 4/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.1 | V | -17.2 | V | -17.2 | V | -17.2 | |
| -5v | -12.2 | V | -12.2 | V | -12.2 | V | -12.2 | |
| -1v | -2.4 | V | -2.42 | V | -2.42 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.1 | V |
| 10v | 24.3 | V | 24.3 | V | 24.3 | V | 24.5 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP10P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 4/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.58 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.57 | √ |
| Ch4 | 5v to 6v | 5.55 | √ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

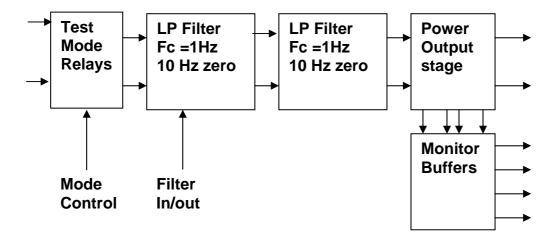
| Unit | .Q_TOP11P | Serial No | |
|---------------|-----------|-----------|--|
| Test Engineer | Xen | | |
| Date | .4/2/10 | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP11P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | 4/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP11P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 4/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP11P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 4/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | $\sqrt{}$ |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

J5

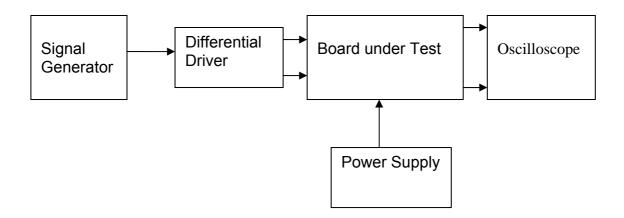
| PIN | SIGNAL | To J1 PI | N OK? |
|-----|--------|----------|--------------|
| 1 | Imon1P | 5 | $\sqrt{}$ |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | V |
| 8 | Imon3N | 20 | |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP11P | Serial No | |
|------|----------|-----------|------|
| | Xen | | |
| Date | 4/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.04 | 1mV | |
| +15v TP4 | 14.93 | 1mV | |
| -15v TP6 | -15.04 | 5mV | |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP11P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 4/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|-----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | $\sqrt{}$ | √ | √ |

Test Switches

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | V | | V |

| Unit | Q_TOP11P | Serial No | |
|---------------|----------|-----------|------|
| Test Engineer | Xen | | |

Date4/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | 1 | Hъ | |
|---|-----|----|--|
| v | ••• | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch3 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch4 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP11P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .4/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.2 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | V |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP11P | Serial No |) | |
|---------------|----------|-----------|---|--|
| Test Engineer | Xen | | | |
| Date | 4/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.397 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP11P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 4/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.5 | V |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.0 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.2 | V |
| -1v | -2.42 | $\sqrt{}$ | -2.42 | $\sqrt{}$ | -2.42 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.42 | | 2.4 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.0 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.3 | V | 24.3 | 1 | 24.2 | 1 |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP11P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 4/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----|----------|
| Not Clipping? | $\sqrt{}$ | V | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

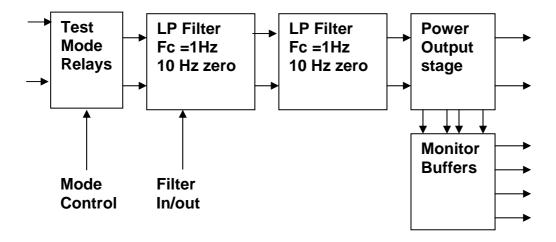
| Unit | Q_TOP12P | Serial No | |
|---------------|----------|-----------|------|
| Test Engineer | Xen | | |
| Date | .4/2/10 | | |

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- 2. Test Equipment
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- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP12P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | 4/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP12P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | 4/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP12P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 4/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

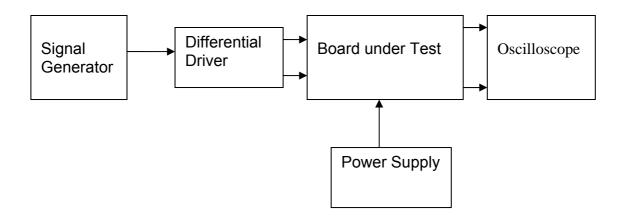
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | |
| 13 | 0V (TP3) | | |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP12P | Serial No | |
|------|----------|-----------|------|
| | Xen | | |
| Date | 4/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 11.95 | 1mV | |
| +15v TP4 | 14.93 | 1mV | |
| -15v TP6 | -14.96 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP12P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 4/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | $\sqrt{}$ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | .Q_TOP12P | Serial No | |
|---------------|-----------|-----------|--|
| Test Engineer | .Xen | | |

Date4/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | ✓ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| ^ | |
|---|--------|
| | 87 |
| | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.35 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP12P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .4/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.2 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP12P | Serial | No | |
|----------------|----------|--------|----|--|
| Test Engineer. | Xen | | | |
| Date | 4/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | V |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | V |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP12P | Serial No | |
|---------------|----------|---------------|------|
| Test Engineer | Xen | | |
| Date | 4/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.4 | V | -24.5 | V | -24.4 | V | -24.5 | |
| -7v | -17.1 | V | -17.2 | V | -17.0 | V | -17.2 | |
| -5v | -12.2 | V | -12.2 | V | -12.2 | V | -12.3 | |
| -1v | -2.4 | V | -2.42 | V | -2.4 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | 1 | 17.0 | V |
| 10v | 24.3 | V | 24.3 | V | 24.3 | V | 24.3 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP12P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 4/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.55 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

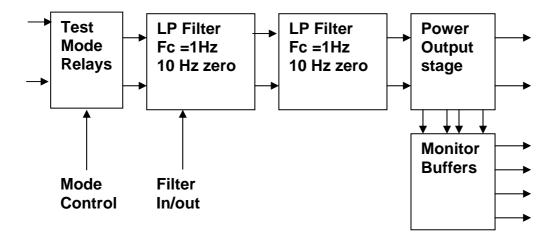
| Unit | Q_TOP13P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | 5/2/10 | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| UnitQ | TOP13P | .Serial No |
|----------------|--------|------------|
| Test EngineerX | | |
| Date5/2 | 2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP13P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP13P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 5/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

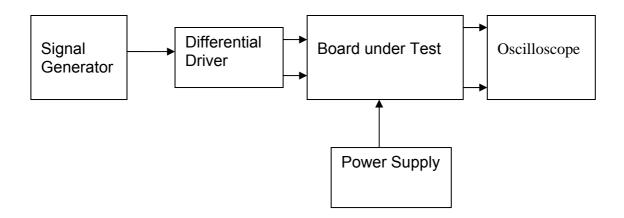
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | √ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP13P | Serial No | |
|---------------|----------|-----------|------|
| Test Engineer | | | |
| Date | 5/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.01 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.98 | 1mV | |
| -15v TP6 | -15.01 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP13P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | 5/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator O | |
|---------|------|-------------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | $\sqrt{}$ |

Test Switches

| Channel | Indio | Indicator | |
|---------|-----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | $\sqrt{}$ | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP13P | Serial No | |
|-----------------|----------|-----------|------|
| Test Engineer . | Xen | | |

Date5/2/10......

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| 0 | .1 | Hz |
|---|----|----|
| | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3.3v to 3.7v | |
| Ch2 | 3.3 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.66 | 0.48 to 0.75v | √ |
| Ch2 | 0.66 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.46 | 0.4v to 0.5v | |
| Ch2 | 0.46 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.46 | 0.4v to 0.5v | V |
| Ch2 | 0.46 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP13P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .5/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.25 | 3v to 3.4v | V |
| Ch3 | 3.2 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.48 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | V |
| Ch3 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP13P | Seria | ıl No | |
|-----------------|----------|-------|-------|--|
| Test Engineer . | Xen | | | |
| Date | 5/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | $\sqrt{}$ |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | √ |

| Unit | Q_TOP13P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Date | 5/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.2 | V | -17.2 | V | -17.2 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.5 | |
| -1v | -2.4 | V | -2.42 | V | -2.42 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | V | 17.2 | 1 | 17.1 | V |
| 10v | 24.5 | V | 24.3 | V | 24.5 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP13P | Serial No | |
|------|----------|-----------|--|
| | eerXen | | |
| Date | 5/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|-----------|-----------|-----------|--------------|
| Not | $\sqrt{}$ | $\sqrt{}$ | $\sqrt{}$ | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.55 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

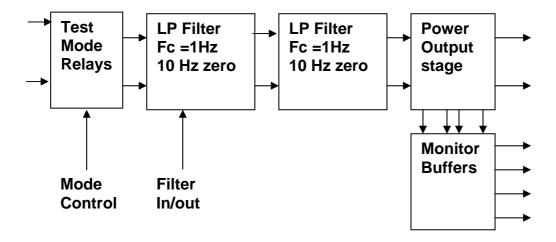
| Unit | .Q_TOP14P | Serial No | |
|---------------|-----------|-----------|------|
| Test Engineer | Xen | | |
| Date | .5/2/10 | | |

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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP14P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 5/2/10 | | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP14P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP14P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 5/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | V |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

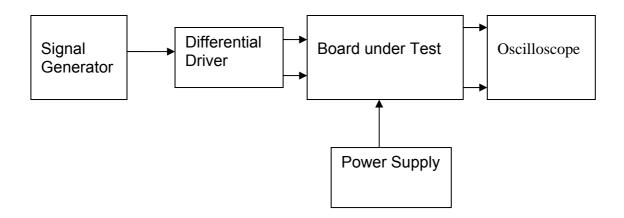
| PIN | SIGNAL | To J1 | PIN OK? |
|-----|--------|-------|-----------|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | V |
| 6 | Imon1N | 18 | $\sqrt{}$ |
| 7 | Imon2N | 19 | $\sqrt{}$ |
| 8 | Imon3N | 20 | √ √ |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | √ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP14P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.03 | 1mV | |
| +15v TP4 | 14.77 | 1mV | |
| -15v TP6 | -15.00 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP14P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 5/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | | √ | √ |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| UnitQ_ | OP14PSerial No |
|-----------------|----------------|
| Test EngineerXe | |
| | |

Date5/2/10......

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| D. | 1 | Н | Z | |
|----|---|---|---|--|
| | | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.66 | 0.48 to 0.75v | √ |
| Ch2 | 0.68 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q TOP14P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .5/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.25 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.48 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | |
| Ch4 | 0.5 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP14P | Seria | al No | |
|-----------------|----------|-------|-------|--|
| Test Engineer . | Xen | | | |
| Date | 5/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | $\sqrt{}$ |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| UnitQ | TOP14PS | Serial No |
|-----------------|---------|-----------|
| Test EngineerXe | en | |
| Date5/2 | 2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.1 | V | -17.1 | V | -17.2 | |
| -5v | -12.3 | V | -12.3 | V | -12.2 | V | -12.3 | |
| -1v | -2.4 | V | -2.41 | V | -2.4 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | √ |
| 7v | 17.1 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.4 | V | 24.5 | V | 24.3 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP14P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.54 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.55 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

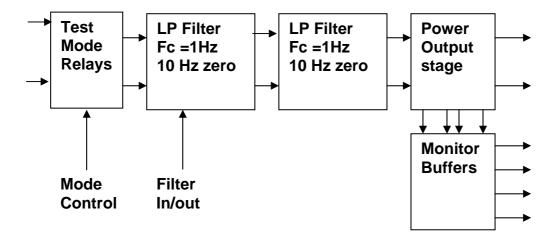
| Unit | Q_TOP15P | Serial No | |
|---------------|----------|-----------|------|
| Test Engineer | | | |
| Date | 15/2/10 | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Jnit | Q TOP15P | Serial No |
|------|----------|-----------|
| | eerXen | |
|)ate | 15/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP15P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 15/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP15P | .Serial No | |
|---------------|----------|------------|--|
| Test Engineer | Xen | | |
| Date | 15/2/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | |

J5

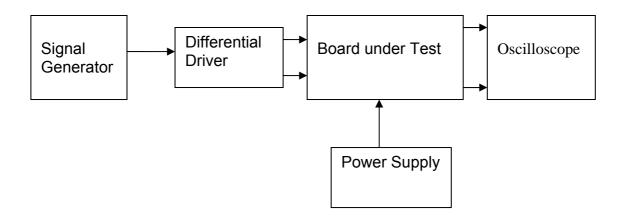
| PIN | SIGNAL | To J1 PI | N OK? |
|-----|--------|----------|--------------|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | V |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | √ |
| 9 | Imon4N | 21 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | \checkmark |
| 25 | 0V (TP3) | | $\sqrt{}$ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP15P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | .15/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.02 | 1mV | \checkmark |
| +15v TP4 | 14.82 | 1mV | |
| -15v TP6 | -15.14 | 5mV | V |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP15P | Serial No |
|------------|----------|-----------|
| Test Engir | neerXen | |
| Date | 15/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | $\sqrt{}$ | V | V |
| Ch3 | | V | V |
| Ch4 | V | V | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|------|-----------|---|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | V |
| Ch3 | V | | V |
| Ch4 | | | V |

| Unit | Q_TOI | P15P | Serial No | | |
|---------------|-------|------|---------------|------|------|
| Test Engineer | Xen | | | | |

Date15/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | √ |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.9 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | V |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP15P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .15/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.9 | 4.7v to 5v | |
| Ch4 | 4.85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | $\sqrt{}$ |
| Ch3 | 3.35 | 3v to 3.4v | $\sqrt{}$ |
| Ch4 | 3.3 | 3v to 3.4v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.5 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | V |
| Ch2 | 0.16 | 0.15v to 0.16v | √ |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP15P | Ser | ial No | |
|-----------------|----------|-----|--------|--|
| Test Engineer . | Xen | | | |
| Date | 15/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.203 | Pin 1 to Pin 2 | 1.203 | √ |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | √ |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.203 | |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | V |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| UnitG | <u> </u> | Serial No |
|----------------|----------|-----------|
| Test EngineerX | Cen | |
| Date1 | 5/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.0 | V | -17.2 | V | -17.2 | |
| -5v | -12.3 | V | -12.2 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.4 | V | -2.41 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.2 | V | 17.1 | 1 | 17.1 | V |
| 10v | 24.5 | V | 24.5 | V | 24.5 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP15P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 15/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|----------|
| Not | \checkmark | \checkmark | \checkmark | √ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|--------------|
| Ch1 | 5v to 6v | 5.55 | V |
| Ch2 | 5v to 6v | 5.56 | V |
| Ch3 | 5v to 6v | 5.54 | \checkmark |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

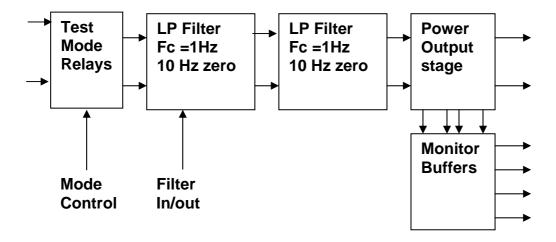
| Unit | .Q_TOP16P | Serial No | |
|---------------|-----------|-----------|------|
| Test Engineer | | | |
| Date | .16/2/10 | | |

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- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP16P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| • | 16/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP16P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 15/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP16P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Data | 15/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

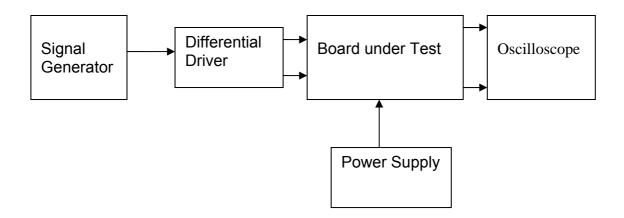
| PIN | SIGNAL | To J1 | PIN OK? |
|-----|--------|-------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ √ |
| 9 | Imon4N | 21 | $\sqrt{}$ |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP16P | Serial No | |
|------|----------|-----------|--|
| | ·Xen | | |
| Date | 15/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.04 | 1mV | \checkmark |
| +15v TP4 | 14.94 | 1mV | |
| -15v TP6 | -15.05 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP16P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .15/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | | | V |
| Ch2 | $\sqrt{}$ | | V |
| Ch3 | $\sqrt{}$ | | V |
| Ch4 | | | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q_TOP16P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | ·Xen | | |
| Date | 15/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | V |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.46 | 0.4v to 0.5v | √ |
| Ch2 | 0.46 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q TOP16P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .15/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5

Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | \checkmark |
| Ch3 | 3.3 | 3v to 3.4v | √ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | |
| Ch2 | 0.49 | 0.4v to 0.5v | V |
| Ch3 | 0.49 | 0.4v to 0.5v | V |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | V |
| Ch2 | 0.16 | 0.15v to 0.16v | V |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | V |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP16P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | .16/2/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.204 | Pin 1 to Pin 2 | 1.204 | \checkmark |
| 2 | 1.16-1.28 | 1.203 | Pin 5 to Pin 6 | 1.203 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.204 | Pin 9 to Pin 10 | 1.203 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.203 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP16P | .Serial No | |
|---------------|----------|------------|--|
| Test Engineer | Xen | | |
| Date1 | 16/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.4 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.4 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.2 | V | -17.2 | V | -17.2 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.42 | V | -2.42 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.41 | V | 2.42 | V | 2.42 | |
| 5v | 12.1 | V | 12.1 | V | 12.2 | V | 12.2 | √ |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.2 | V | 24.3 | V | 24.3 | V | 24.2 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP16P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 16/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|--------------|-----------|-----|-----|
| Not Clipping? | \checkmark | $\sqrt{}$ | V | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.54 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.55 | V |
| Ch3 | 5v to 6v | 5.55 | √ |
| Ch4 | 5v to 6v | 5.55 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

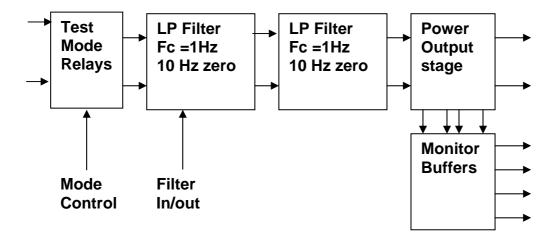
| Unit | Q TOP17P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 16/2/10 | | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
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- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
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- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP17P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | 16/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | .Q TOP17P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .16/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP17P | Serial No |
|-------------|----------|-----------|
| Test Engine | erXen | |
| Nata | 16/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

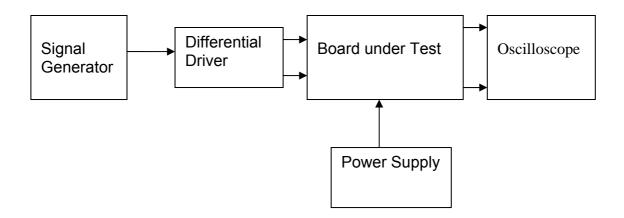
| PIN | SIGNAL | To J1 | PIN OK? |
|-----|--------|-------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | $\sqrt{}$ |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ √ |
| 9 | Imon4N | 21 | $\sqrt{}$ |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP17P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date1 | 6/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.01 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.97 | 1mV | |
| -15v TP6 | -14.94 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP17P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 16/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | V | √ | √ |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q_TOP17P | Serial No |
|---------------|----------|-----------|
| Test Engineer | Xen | |
| Date | 16/2/10 | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | V |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4 85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP17P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .16/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | V |
| Ch3 | 3.35 | 3v to 3.4v | √ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.5 | 0.4v to 0.5v | |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP17P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 16/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.398 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.397 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q TOP17P | Serial | No | |
|-----------------|----------|--------|----|--|
| Test Engineer . | Xen | | | |
| Date | 16/2/10 | | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.3 | V | -24.3 | |
| -7v | -17.2 | V | -17.0 | V | -17.0 | V | -17.1 | |
| -5v | -12.3 | V | -12.2 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.4 | V | -2.4 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | 1 | 17.0 | V |
| 10v | 24.3 | V | 24.3 | V | 24.2 | V | 24.2 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP17P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 16/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.57 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

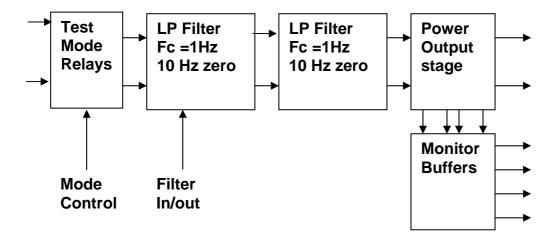
| Unit | Q_TOP18P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | .16/2/10 | | |

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- 2. Test Equipment
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- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit(| Q TOP18P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date1 | 16/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP18P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 16/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP18P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 16/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | $\sqrt{}$ |
| 3 | PD3P | Photodiode C+ | 3 | $\sqrt{}$ |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | V |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | V |
| 8 | PD3N | Photodiode C- | 16 | √ |
| 9 | PD4N | Photodiode D- | 17 | |

J5

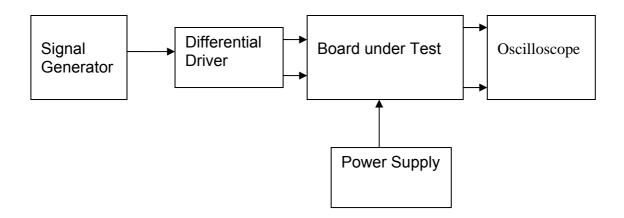
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP18P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | 16/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.00 | 1mV | |
| +15v TP4 | 14.81 | 1mV | |
| -15v TP6 | -15.05 | 5mV | |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP18P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | .Xen | |
| Date | .16/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | |
| Ch4 | | √ | $\sqrt{}$ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q TOP18P | Serial N | 0 | |
|-----------------|----------|----------|---|--|
| Test Engineer . | Xen | | | |
| Date | 16/2/10 | | | |

8. Corner frequency tests

Ch4

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | √ |

4.9

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.45 | 3.3v to 3.7v | √ |
| Ch3 | 3.45 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

4.7 to 5v

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.7 | 0.48 to 0.75v | √ |
| Ch3 | 0.7 | 0.48 to 0.75v | √ |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP18P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .16/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.25 | 3v to 3.4v | V |
| Ch2 | 3.3 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch2 | 0.49 | 0.4v to 0.5v | V |
| Ch3 | 0.49 | 0.4v to 0.5v | V |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP18P | Serial No |
|---------------|----------|-----------|
| Test Engineer | Xen | |
| Date | 16/2/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.395 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.397 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP18P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 16/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.4 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.0 | V | -17.1 | V | -17.1 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.41 | V | -2.41 | V | -2.4 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | |
| 7v | 17.0 | V | 17.0 | $\sqrt{}$ | 17.0 | V | 17.1 | $\sqrt{}$ |
| 10v | 24.2 | V | 24.3 | V | 24.3 | V | 24.5 | |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP18P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 16/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | √ |
| Ch4 | 5v to 6v | 5.55 | √ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

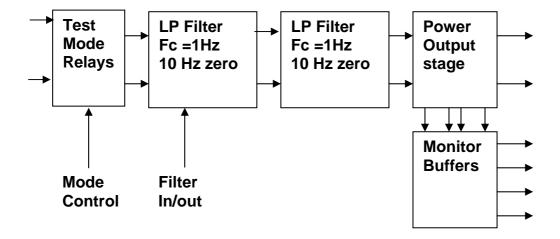
| Unit | Q TOP19P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 16/2/10 | |

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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP19P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 16/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
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| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP19P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 16/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP19P | Serial No |
|-------------|----------|-----------|
| Test Engine | erXen | |
| Data | 16/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | $\sqrt{}$ |
| 3 | PD3P | Photodiode C+ | 3 | $\sqrt{}$ |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | V |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | V |
| 8 | PD3N | Photodiode C- | 16 | √ |
| 9 | PD4N | Photodiode D- | 17 | |

J5

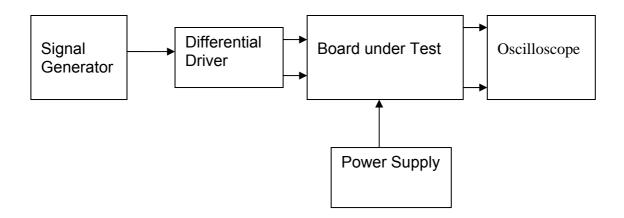
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | \checkmark |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP19P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | 16/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 11.94 | 1mV | |
| +15v TP4 | 14.97 | 1mV | |
| -15v TP6 | -15.05 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP19P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | .Xen | |
| Date | .16/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | V | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP19P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 16/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch4 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP19P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .16/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.2 | 3v to 3.4v | \checkmark |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | V |
| Ch2 | 0.48 | 0.4v to 0.5v | V |
| Ch3 | 0.49 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP19P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 16/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | V |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | √ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | √ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP19PS | Serial No |
|----------------|-----------|-----------|
| Test Engineer> | Ken | |
| Date1 | 6/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.2 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.4 | V | -2.41 | V | -2.42 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.2 | V | 17.1 | V | 17.1 | 1 | 17.0 | V |
| 10v | 24.5 | V | 24.4 | V | 24.4 | V | 24.3 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP19P | Serial No |
|------|----------|-----------|
| | erXen | |
| Date | 16/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

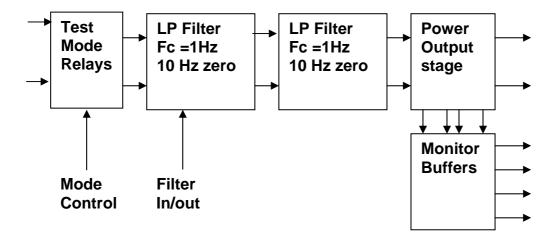
| Unit | Q TOP20P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | 17/2/10 | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
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- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP20P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 17/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | .Q TOP20P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | 17/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP20P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Data | 17/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|-----------|
| 1 | PD1P | Photodiode A+ | 1 | $\sqrt{}$ |
| 2 | PD2P | Photodiode B+ | 2 | |
| 3 | PD3P | Photodiode C+ | 3 | |
| 4 | PD4P | Photodiode D+ | 4 | V |
| 5 | 0V | | | V |
| 6 | PD1N | Photodiode A- | 14 | V |
| 7 | PD2N | Photodiode B- | 15 | $\sqrt{}$ |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | V |

J5

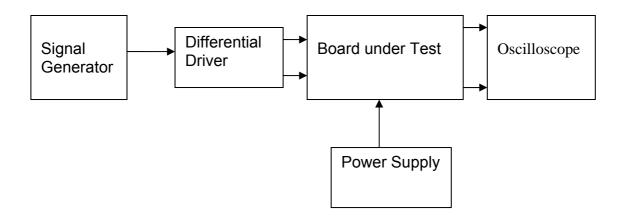
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | √ |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | √ |
| 6 | Imon1N | 18 | $\sqrt{}$ |
| 7 | Imon2N | 19 | $\sqrt{}$ |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | √ |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP20P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 11.99 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.95 | 1mV | |
| -15v TP6 | -15.00 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP20P | Serial No |
|---------------|--------------|-----------|
| Test Engineer | _ | |
| Date | .17/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | $\sqrt{}$ |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q TOP20P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 17/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | 1 | Ш- |
|---|---|-----|
| U | | 112 |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | |
| Ch4 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.46 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP20P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .17/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.25 | 3v to 3.4v | V |
| Ch2 | 3.3 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | √ |
| Ch2 | 0.5 | 0.4v to 0.5v | √ |
| Ch3 | 0.5 | 0.4v to 0.5v | √ |
| Ch4 | 0.48 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP20P | Serial No | |
|-----------------|----------|-----------|------|
| Test Engineer . | Xen | | |
| Date | 17/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.394 | Pin 11 to Pin 12 | 0.396 | V |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | V |
| Ch2 | V |
| Ch3 | V |
| Ch4 | \checkmark |

| Unit | Q_TOP20P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 17/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.1 | V | -17.1 | V | -17.1 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.42 | V | -2.42 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | | 2.42 | V | 2.42 | |
| 5v | 12.2 | V | 12.2 | √ | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | V | 17.0 | 1 | 17.1 | V |
| 10v | 24.5 | V | 24.3 | √ | 24.3 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP20P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 17/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|--------------|----------|----------|-----|
| Not Clipping? | \checkmark | √ | √ | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | V |
| Ch3 | 5v to 6v | 5.54 | V |
| Ch4 | 5v to 6v | 5.56 | |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

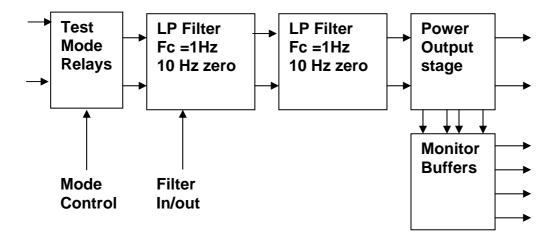
| Unit | Q TOP21P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 17/2/10 | |

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- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP21P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 17/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP21P | Serial No | |
|------|----------|-----------|--|
| | rXen | | |
| Date | 17/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP21P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Data | 17/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

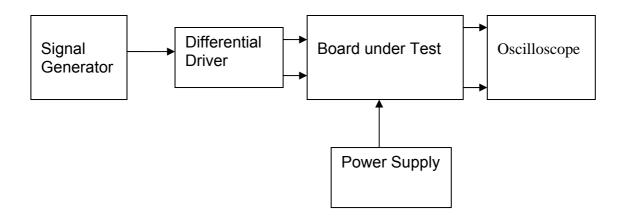
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP21P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 17/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.02 | 1mV | |
| +15v TP4 | 14.96 | 1mV | |
| -15v TP6 | -15.06 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP21P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 17/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | | |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | V |
| Ch4 | | | |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q TOP21P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | rXen | | |
| Date | 17/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| 0 | ď | 1 | H | 1 | Z | |
|---|---|---|---|---|---|--|
| | | | | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.35 | 3.3v to 3.7v | √ |
| Ch4 | 3.34 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP21P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .17/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | |
| Ch2 | 0.49 | 0.4v to 0.5v | |
| Ch3 | 0.49 | 0.4v to 0.5v | |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP21P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 17/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? |
|-----|-----------|------------------------|------------------|--------------------|----------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | (+/- 0.1v) √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? | | |
|-----|------------------|--|--|
| Ch1 | $\sqrt{}$ | | |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | √ | | |

| Unit | Q_TOP21P | .Serial No | |
|---------------|----------|----------------|------|
| Test Engineer | Xen | | |
| Date | 17/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.4 | V |
| -7v | -17.2 | V | -17.2 | V | -17.2 | V | -17.1 | V |
| -5v | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ | -12.4 | $\sqrt{}$ | -12.3 | $\sqrt{}$ |
| -1v | -2.4 | $\sqrt{}$ | -2.42 | $\sqrt{}$ | -2.42 | $\sqrt{}$ | -2.41 | $\sqrt{}$ |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.42 | \checkmark | 2.42 | $\sqrt{}$ | 2.42 | | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | V | 17.2 | V | 17.1 | V |
| 10v | 24.5 | V | 24.3 | V | 24.5 | V | 24.4 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP21P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 17/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

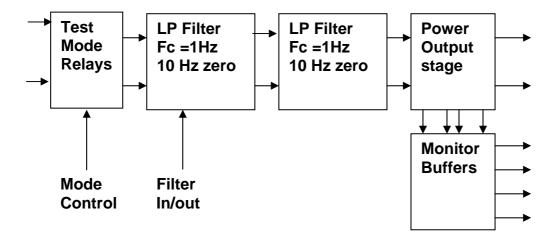
| Unit | Q_TOP22P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 18/2/10 | | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| UnitQ | TOP22P | Serial No |
|----------------|--------|-----------|
| Test EngineerX | | |
| Date18 | 3/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | .Q TOP22P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .17/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP22P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .17/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | √ |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

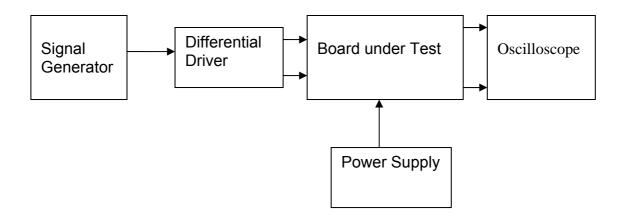
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | \checkmark |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP22P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 17/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 11.99 | 1mV | |
| +15v TP4 | 14.81 | 1mV | |
| -15v TP6 | -14.99 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP22P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | .Xen | |
| Date | .17/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | | V | V |
| Ch2 | | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q TOP22P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 18/2/10 | | |

8. Corner frequency tests

Ch4

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

4.85

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | | Output | Specification | Pass/Fail |
|---|-----|--------|---------------|-----------|
| Ī | Ch1 | 4.85 | 4.7 to 5v | |
| | Ch2 | 4.85 | 4.7 to 5v | |
| Ī | Ch3 | 4.85 | 4.7 to 5v | |

4.7 to 5v

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.35 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP22P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .18/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.3 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.49 | 0.4v to 0.5v | |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP22P | Serial No | |
|-----------------|----------|---------------|------|
| Test Engineer . | Xen | | |
| Date | 18/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | $\sqrt{}$ |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | .Q_TOP22P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | .Xen | |
| Date | .18/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.2 | |
| -5v | -12.3 | V | -12.2 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.4 | V | -2.42 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | $\sqrt{}$ | 2.42 | |
| 5v | 12.2 | V | 12.1 | V | 12.2 | V | 12.2 | |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | |
| 10v | 24.3 | V | 24.3 | V | 24.3 | V | 24.4 | |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Jnit | Q TOP22P | Serial No |
|--------|----------|-----------|
| | eerXen | |
| າate ັ | 18/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

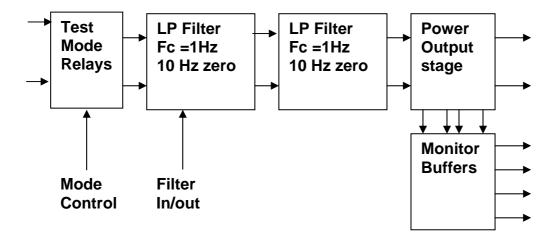
| Unit | Q TOP23P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 18/2/10 | | |

Contents

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- 2. Test Equipment
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- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP23P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 18/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP23P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 18/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP23P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 18/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

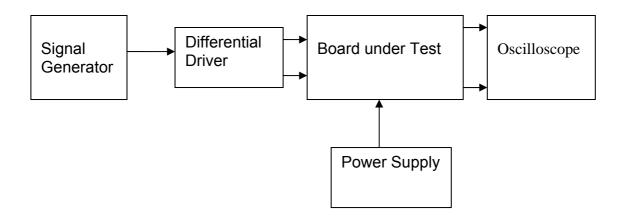
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | \checkmark |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit(| Q TOP23P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date1 | 8/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.04 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.84 | 1mV | V |
| -15v TP6 | -14.97 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current | |
|--------|---------|--|
| +16.5v | 400mA | |
| -16.5v | 300mA | |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP23P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .18/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | √ | √ | √ |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q TOP23P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 18/2/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | V |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4 85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.66 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP23P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .18/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.2 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.48 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP23P | Serial No | |
|-----------------|----------|---------------|------|
| Test Engineer . | Xen | | |
| Date | 18/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | V |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | V |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | $\sqrt{}$ |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP23P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | .18/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | V |
| -7v | -17.1 | V | -17.2 | V | -17.2 | V | -17.2 | V |
| -5v | -12.3 | $\sqrt{}$ | -12.3 | √ | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ |
| -1v | -2.41 | $\sqrt{}$ | -2.42 | √ | -2.42 | $\sqrt{}$ | -2.42 | $\sqrt{}$ |
| 0v | 0 | $\sqrt{}$ | 0 | √ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.42 | \checkmark | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.4 | V | 24.3 | V | 24.3 | V | 24.4 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP23P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 18/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.55 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

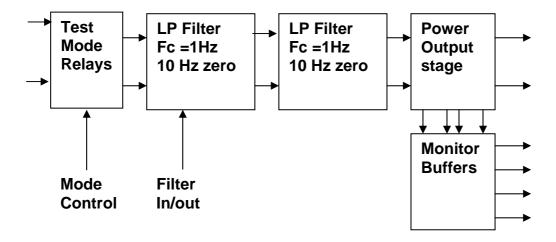
| Unit | Q TOP24P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | 18/2/10 | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| UnitQ | TOP24P | Serial No |
|----------------|--------|-----------|
| Test EngineerX | | |
| Date18 | 3/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP24P | Serial No |
|------|----------|-----------|
| | rXen | |
| Date | 18/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP24P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Data | 18/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | √ |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

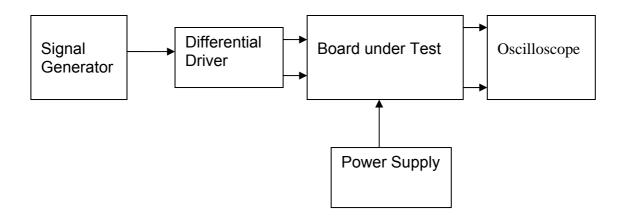
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP24P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 18/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.02 | 1mV | |
| +15v TP4 | 14.95 | 1mV | |
| -15v TP6 | -15.04 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP24P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 18/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | V | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | .Q TOP24P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .18/2/10 | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4 85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.35 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.66 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP24P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .18/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.2 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.25 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.48 | 0.4v to 0.5v | √ |
| Ch4 | 0.5 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | V |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP24P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 18/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | √ |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | V |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | V |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.398 | √ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | √ |

| Unit | Q TOP24P | .Serial No | |
|---------------|----------|------------|--|
| Test Engineer | Xen | | |
| Date1 | 18/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.4 | $\sqrt{}$ | -24.5 | $\sqrt{}$ |
| -7v | -17.1 | V | -17.2 | V | -17.0 | V | -17.2 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | |
| -1v | -2.42 | V | -2.42 | V | -2.4 | V | -2.42 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | |
| 5v | 12.1 | V | 12.2 | V | 12.2 | V | 12.2 | √ |
| 7v | 17.0 | V | 17.1 | V | 17.2 | V | 17.1 | V |
| 10v | 24.2 | V | 24.4 | V | 24.5 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP24P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | 18/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.58 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.55 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

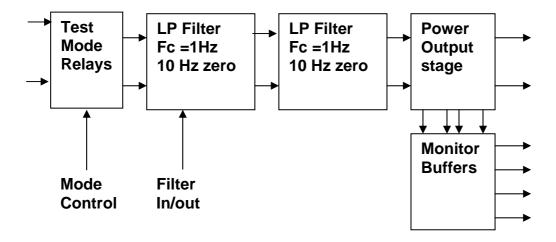
| Unit | Q TOP25P | Serial No | |
|------|----------|-----------|--|
| | rXen | | |
| Date | 23/2/10 | | |

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- 2. Test Equipment
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- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP25P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 23/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP25P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 22/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP25P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .22/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

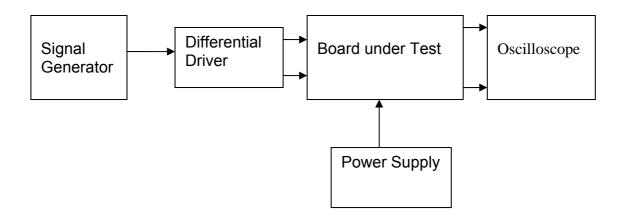
| PIN | SIGNAL | To J1 | PIN OK? |
|-----|--------|-------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | $\sqrt{}$ |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ √ |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | |
| 13 | 0V (TP3) | | |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP25P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 11.99 | 1mV | |
| +15v TP4 | 14.96 | 1mV | |
| -15v TP6 | -15.04 | 5mV | |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP25P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | | |
|---------|------|-----------|-----------|--|
| | ON | ON OFF | | |
| Ch1 | V | √ | V | |
| Ch2 | V | | $\sqrt{}$ | |
| Ch3 | V | | $\sqrt{}$ | |
| Ch4 | | √ | $\sqrt{}$ | |

Test Switches

| Channel | Indio | OK? | |
|---------|--------|-----|----------|
| | ON OFF | | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_T(| DP25P | Serial No | | |
|---------------|------|-------|---------------|------|--|
| Test Engineer | Xen. | | | | |

Date23/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | - 1 | ш | , |
|---|-----|---|---|
| U | | п | 4 |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.35 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP25P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .23/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | √ |
| Ch2 | 0.48 | 0.4v to 0.5v | √ |
| Ch3 | 0.49 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP25P | Seria | l No | |
|-----------------|----------|-------|------|--|
| Test Engineer . | Xen | | | |
| Date | 23/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | V |
| 3 | 0.37-0.41 | 0.394 | Pin 11 to Pin 12 | 0.396 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP25P | Serial No |
|-------------|----------|-----------|
| Test Engine | erXen | |
| Date | 23/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | $\sqrt{}$ | -24.5 | V | -24.4 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.0 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.2 | |
| -1v | -2.42 | V | -2.41 | V | -2.41 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | |
| 7v | 17.1 | V | 17.2 | V | 17.0 | V | 17.1 | |
| 10v | 24.5 | V | 24.5 | V | 24.3 | V | 24.5 | |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP25P | Serial No |
|------|----------|-----------|
| | erXen | |
| Date | 23/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----------|-----|
| Not Clipping? | $\sqrt{}$ | V | $\sqrt{}$ | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.54 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

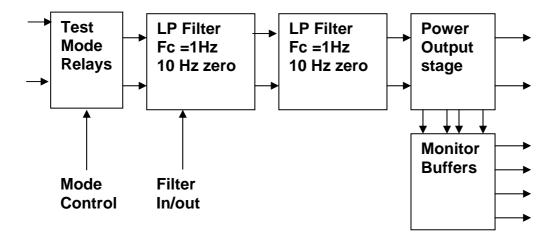
| Unit | Q TOP26P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 23/2/10 | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP26P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 23/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | .Q TOP26P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .23/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP26P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .23/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | √ |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

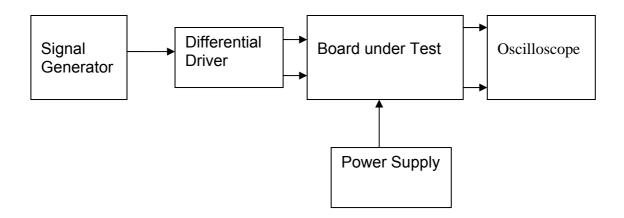
| PIN | SIGNAL | To J1 | PIN OK? |
|-----|--------|-------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | $\sqrt{}$ |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ √ |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP26P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.06 | 1mV | |
| +15v TP4 | 14.96 | 1mV | |
| -15v TP6 | -14.99 | 5mV | V |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP26P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .23/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|--------|-----------|-----------|
| | ON OFF | | |
| Ch1 | V | | |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | V |
| Ch4 | | | |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q_T | OP26P | Serial No |) | |
|-------------|-------|-------|---------------|---|------|
| Test Engine | erXen | | | | |

Date23/2/10......

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| \mathbf{a} | - 4 | | _ |
|--------------|-----|---|---|
| u | _ 1 | н | 7 |
| | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.35 | 3.3v to 3.7v | |
| Ch3 | 3.35 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.66 | 0.48 to 0.75v | √ |
| Ch4 | 0.66 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q TOP26P | Serial No |
|---------------|--------------|-----------|
| Test Engineer | _ | |
| Date | .23/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.2 | 3v to 3.4v | |
| Ch2 | 3.2 | 3v to 3.4v | |
| Ch3 | 3.2 | 3v to 3.4v | V |
| Ch4 | 3.2 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.46 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.48 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP26P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 23/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.395 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.396 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP26P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Data | 23/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | V |
| -7v | -17.2 | V | -17.2 | V | -17.2 | V | -17.2 | V |
| -5v | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ | -12.3 | $\sqrt{}$ |
| -1v | -2.42 | $\sqrt{}$ | -2.4 | $\sqrt{}$ | -2.42 | $\sqrt{}$ | -2.41 | $\sqrt{}$ |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.42 | \checkmark | 2.42 | $\sqrt{}$ | 2.42 | | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.1 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.4 | V | 24.3 | V | 24.3 | V | 24.3 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Jnit | Q TOP26P | Serial No |
|------|----------|-----------|
| | erXen | |
| Date | 23/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|----------|----------|----------|
| Not Clipping? | $\sqrt{}$ | √ | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

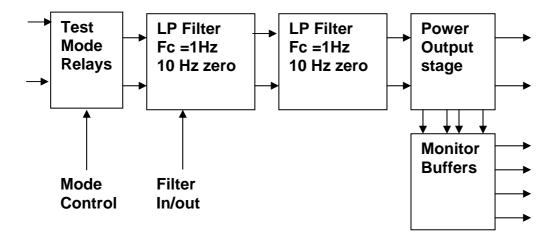
| Unit | .Q_TOP27P | Serial No | |
|---------------|-----------|-----------|------|
| Test Engineer | | | |
| Date | .24/2/10 | | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP27P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 24/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | .Q TOP27P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .23/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP27P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .23/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

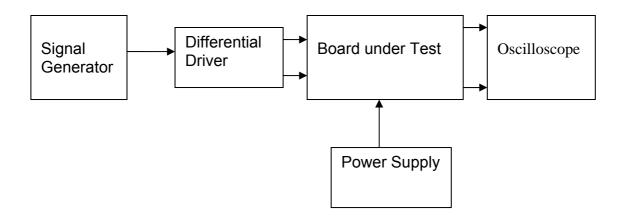
| PIN | SIGNAL | To J1 | PIN OK? |
|-----|--------|-------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ √ |
| 9 | Imon4N | 21 | $\sqrt{}$ |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP27P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 11.98 | 1mV | |
| +15v TP4 | 14.93 | 1mV | |
| -15v TP6 | -15.02 | 5mV | V |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP27P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | V | √ | √ |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q_TOP2 7 F | Seria | l No | |
|---------------|-------------------|-------|------|--|
| Test Engineer | Xen | | | |

Date23/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | 1 | Hъ | |
|---|-----|----|--|
| v | ••• | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch3 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch4 | 3.35 | 3.3v to 3.7v | |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP27P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .23/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | |
| Ch2 | 0.49 | 0.4v to 0.5v | V |
| Ch3 | 0.5 | 0.4v to 0.5v | V |
| Ch4 | 0.48 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification Pass/ | |
|-----|--------|---------------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | V |
| Ch3 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP27P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 23/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | √ |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | V |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | √ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP27P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Data | 24/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.3 | V | -24.3 | V | -24.3 | V | -24.3 | |
| -7v | -17.1 | V | -17.0 | V | -17.0 | V | -17.0 | |
| -5v | -12.3 | V | -12.2 | V | -12.2 | V | -12.2 | |
| -1v | -2.41 | V | -2.4 | V | -2.4 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.41 | V | 2.42 | $\sqrt{}$ | 2.42 | |
| 5v | 12.1 | V | 12.1 | V | 12.2 | V | 12.1 | |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | √ |
| 10v | 24.2 | V | 24.2 | V | 24.2 | V | 24.3 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP27P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 23/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----------|-----|
| Not Clipping? | $\sqrt{}$ | V | $\sqrt{}$ | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.57 | $\sqrt{}$ |
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LIGO-T0900231-v3 Advanced LIGO UK

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

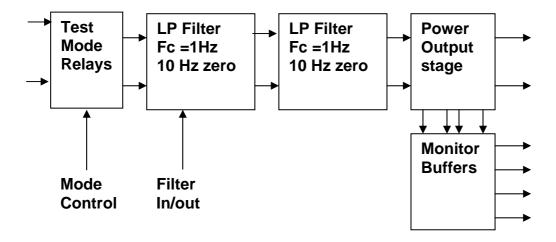
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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP28P | Serial No |
|------|----------|-----------|
| | rXen | |
| Date | 24/2/10 | |

2. Test equipment

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Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
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Analogue oscilloscope
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Relay test box

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| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP28P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 24/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP28P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .24/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

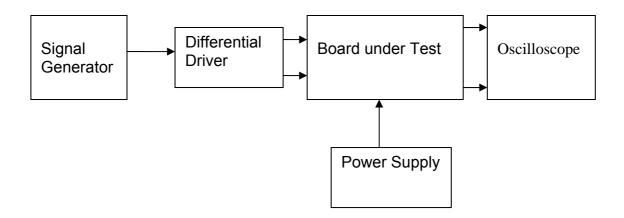
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP28P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 24/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 11.98 | 1mV | |
| +15v TP4 | 14.95 | 1mV | |
| -15v TP6 | -15.08 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q_TOP28P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 24/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | √ | √ | V |
| Ch2 | V | | V |
| Ch3 | V | | |
| Ch4 | √ | √ | √ |

Test Switches

| Channel | Indi | Indicator | | |
|---------|------|-----------|---|--|
| | ON | OFF | | |
| Ch1 | V | | V | |
| Ch2 | V | | V | |
| Ch3 | V | | V | |
| Ch4 | V | | V | |

| Unit | Q_T | OP28P | Serial N | 0 | | |
|---------------|-----|-------|--------------|---|------|--|
| Test Engineer | Xen | | | | | |

Date24/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.9 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.46 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP28P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .24/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.9 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.2 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.5 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP28P | Seria | al No | |
|-----------------|----------|-------|-------|--|
| Test Engineer . | Xen | | | |
| Date | 24/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.395 | Pin 7 to Pin 8 | 0.396 | √ |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | √ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | √ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | |
| Ch2 | |
| Ch3 | |
| Ch4 | \checkmark |

| Unit | Q_TOP28P | Serial No |
|-------------|----------|-----------|
| Test Engine | erXen | |
| Data | 24/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | V |
| -7v | -17.2 | V | -17.2 | V | -17.1 | V | -17.2 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.2 | V |
| -1v | -2.42 | V | -2.41 | V | -2.4 | V | -2.4 | V |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | V | 17.1 | V | 17.1 | V |
| 10v | 24.4 | V | 24.3 | V | 24.5 | V | 24.5 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Jnit | Q TOP28P | Serial No |
|--------|----------|-----------|
| | erXen | |
| Tate 0 | 24/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.55 | |
| Ch3 | 5v to 6v | 5.54 | |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

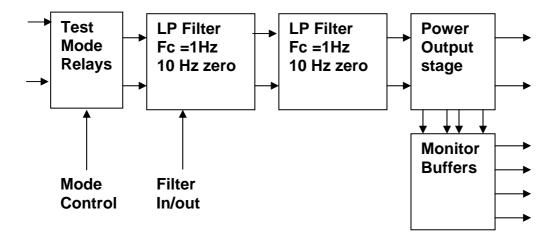
| Unit | Q TOP29P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 25/2/10 | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP29P | Serial No |
|------|----------|-----------|
| | erXen | |
| Date | 25/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP29P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 24/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP29P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .24/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | √ |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

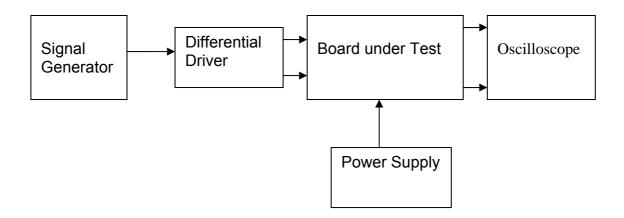
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP29P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .24/2/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.05 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.80 | 1mV | |
| -15v TP6 | -15.01 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q_TOP29P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .24/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON OFF | | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | $\sqrt{}$ | V | V |
| Ch4 | | V | V |

| Jnit | Q_ | 10P29P | Serial No | | |
|-------------|-------|--------|---------------|------|--|
| Test Engine | erXer | ۱ | | | |

Date24/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| 0 | ď | 1 | ŀ | 1 | Z | |
|---|---|---|---|---|---|--|
| | | | | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | √ |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP29P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .24/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | √ |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4 85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | V |
| Ch2 | 3.3 | 3v to 3.4v | √ |
| Ch3 | 3.3 | 3v to 3.4v | √ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.49 | 0.4v to 0.5v | |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.49 | 0.4v to 0.5v | |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP29P | Seri | ial No | |
|-----------------|----------|------|--------|--|
| Test Engineer . | Xen | | | |
| Date | 24/2/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | √ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | √ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP29P | Serial No |
|-------------|----------|-----------|
| Test Engine | erXen | |
| Data | 25/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | $\sqrt{}$ | -24.3 | $\sqrt{}$ | -24.3 | $\sqrt{}$ | -24.4 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.1 | V | -17.1 | V | -17.0 | |
| -5v | -12.5 | V | -12.3 | V | -12.1 | V | -12.2 | |
| -1v | -2.42 | V | -2.42 | V | -2.41 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.41 | V | 2.4 | V | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.1 | V | 12.1 | V | 12.2 | √ |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.2 | V | 24.2 | V | 24.3 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP29P | Serial No | |
|------|----------|-----------|--|
| | erXen | | |
| Date | 24/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|------------------|-----------|-----|-----------|--------------|
| Not Climping? | $\sqrt{}$ | V | $\sqrt{}$ | \checkmark |
| Clipping? | • | , | , | , |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.56 | |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

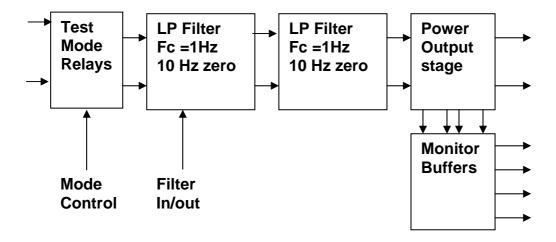
| Unit | .Q TOP30P | Serial No | |
|---------------|-----------|-----------|------|
| Test Engineer | | | |
| Date | .25/2/10 | | |

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- 2. Test Equipment
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- 5. Test Set Up
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- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| UnitQ | TOP30P | Serial No |
|----------------|--------|-----------|
| Test EngineerX | | |
| Date25 | 5/2/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP30P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 25/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP30P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .25/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

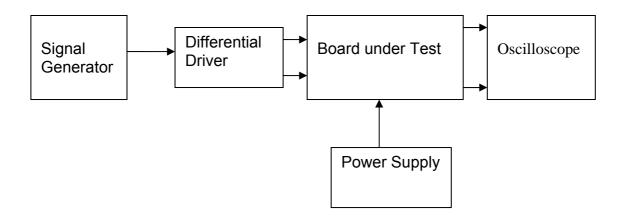
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP30P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 25/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.94 | 1mV | |
| -15v TP6 | -14.92 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | .Q TOP30P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .25/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP30P | Serial No | ١ | |
|---------------|----------|-----------|---|--|
| Test Engineer | Xen | | | |

Date25/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.9 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.35 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | V |

| Unit | .Q_TOP30P | .Serial No |
|---------------|-----------|------------|
| Test Engineer | | |
| Date | .25/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.5 | 0.4v to 0.5v | √ |
| Ch4 | 0.5 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP30P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 25/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | $\sqrt{}$ |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP30P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Date | 25/2/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.2 | V | -17.1 | V | -17.1 | |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.2 | |
| -1v | -2.42 | V | -2.42 | V | -2.4 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | $\sqrt{}$ | 2.42 | |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | |
| 7v | 17.2 | V | 17.1 | V | 17.0 | V | 17.0 | V |
| 10v | 24.5 | V | 24.3 | V | 24.4 | V | 24.2 | V |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP30P | Serial No | |
|------|----------|-----------|--|
| | rXen | | |
| Date | 25/2/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----|----------|
| Not Clipping? | $\sqrt{}$ | V | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.55 | |
| Ch2 | 5v to 6v | 5.57 | V |
| Ch3 | 5v to 6v | 5.54 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

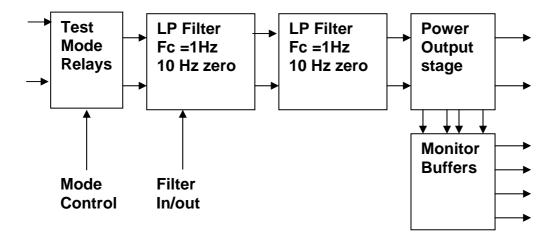
| Unit | .Q TOP31P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP31P | Serial No | |
|------|----------|-----------|------|
| | Xen | | |
| Date | 2/3/10 | | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP31P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | 25/2/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP31P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Data | 25/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | √ |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

J5

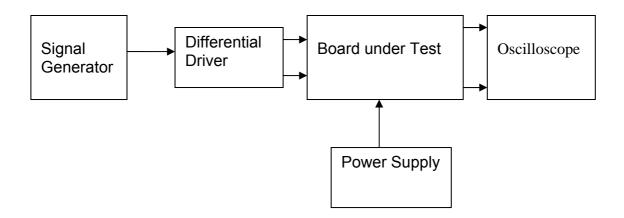
| PIN | SIGNAL | To J1 | PIN | OK? |
|-----|--------|-------|-----|--------------|
| 1 | Imon1P | 5 | | ✓ |
| 2 | Imon2P | 6 | | $\sqrt{}$ |
| 3 | Imon3P | 7 | | $\sqrt{}$ |
| 4 | Imon4P | 8 | | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | Imon1N | 18 | 3 | \checkmark |
| 7 | Imon2N | 19 | 9 | \checkmark |
| 8 | Imon3N | 20 |) | $\sqrt{}$ |
| 9 | Imon4N | 2 | 1 | V |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP31P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .2/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.05 | 1mV | |
| +15v TP4 | 14.85 | 1mV | |
| -15v TP6 | -15.05 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP31P | Serial No |
|------|----------|-----------|
| | eerXen | |
| Date | 2/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | $\sqrt{}$ |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q_ | TOP31P | Serial No |) | |
|---------------|----|--------|---------------|---|------|
| Test Engineer | Xe | n | | | |

Date2/3/10......

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| ^ | - 4 | | _ |
|---|-----|---|---|
| u | _ 1 | н | 7 |
| | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch3 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch4 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.68 | 0.48 to 0.75v | \checkmark |
| Ch2 | 0.68 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 067 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP31P | Serial No |
|---------------|-------------|-----------|
| Test Engineer | | |
| Date | .2/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | $\sqrt{}$ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.35 | 3v to 3.4v | |
| Ch2 | 3.25 | 3v to 3.4v | |
| Ch3 | 3.35 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch2 | 0.48 | 0.4v to 0.5v | V |
| Ch3 | 0.5 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch4 | 0.5 | 0.4v to 0.5v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch2 | 0.16 | 0.15v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | V |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | $\sqrt{}$ |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP31P | Serial No |) | |
|---------------|----------|-----------|---|--|
| Test Engineer | Xen | | | |
| Date | 2/3/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.203 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | Q_TOP31P | Serial No |
|-------------|----------|-----------|
| Test Engine | eerXen | |
| Data | 2/3/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.0 | V | -17.1 | V | -17.1 | |
| -5v | -12.3 | V | -12.2 | V | -12.2 | V | -12.3 | |
| -1v | -2.42 | V | -2.4 | V | -2.4 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.2 | V | 17.0 | 1 | 17.0 | V |
| 10v | 24.5 | V | 24.5 | V | 24.4 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP31P | Serial No | |
|------|----------|-----------|------|
| | Xen | | |
| Date | 2/3/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|--------------|
| Not | \checkmark | \checkmark | \checkmark | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

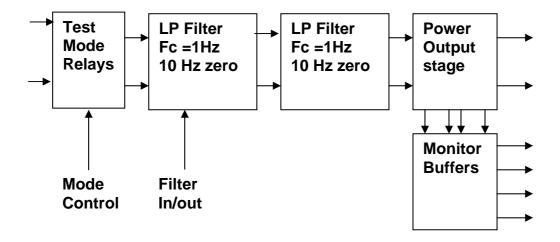
| Unit | Q_TOP32P. | Serial No . | |
|---------------|-----------|-------------|--|
| Test Engineer | Xen | | |
| Date | 2/3/10 | | |

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- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP32P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 2/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP32P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 2/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP32P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 2/3/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

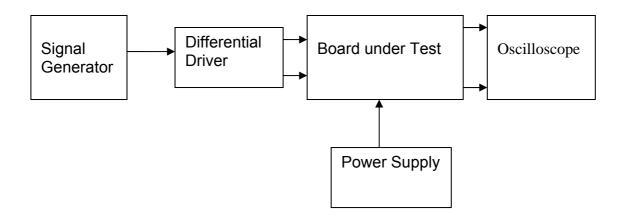
J5

| PIN | SIGNAL | То | J1 PIN | OK? |
|-----|--------|----|--------|--------------|
| 1 | Imon1P | | 5 | \checkmark |
| 2 | Imon2P | | 6 | \checkmark |
| 3 | Imon3P | | 7 | \checkmark |
| 4 | Imon4P | | 8 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | Imon1N | | 18 | \checkmark |
| 7 | Imon2N | | 19 | \checkmark |
| 8 | Imon3N | | 20 | |
| 9 | Imon4N | | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | V |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP32P | Serial No | 0 |
|---------------|----------|-----------|---|
| Test Engineer | Xen | | |
| Date | 2/3/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | |
| +15v TP4 | 14.80 | 1mV | |
| -15v TP6 | -14.97 | 5mV | V |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP32P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 2/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | | | V |
| Ch2 | $\sqrt{}$ | | V |
| Ch3 | | | V |
| Ch4 | | | V |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|-----|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q TOP32P | Serial No |
|------|----------|-----------|
| | erXen | |
| _ , | | |

Date.....2/3/10.....

8. Corner frequency testsApply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | V |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch4 | 3.35 | 3.3v to 3.7v | \checkmark |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.66 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.46 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | Q_TOP32P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 2/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | V |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.49 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q_TOP32P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Date | 2/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP32P | Serial No | |
|--------------|----------|-----------|--|
| Test Enginee | rXen | | |
| Data | 2/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.4 | $\sqrt{}$ |
| -7v | -17.1 | V | -17.0 | V | -17.2 | V | -17.1 | |
| -5v | -12.2 | V | -12.2 | V | -12.3 | V | -12.2 | |
| -1v | -2.42 | V | -2.41 | V | -2.42 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.41 | V | 2.42 | V | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | √ |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | √ |
| 10v | 24.2 | V | 24.3 | V | 24.3 | V | 24.5 | 1 |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP32P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 2/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|-----------|-----------|-----------|--------------|
| Not | $\sqrt{}$ | $\sqrt{}$ | $\sqrt{}$ | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.55 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

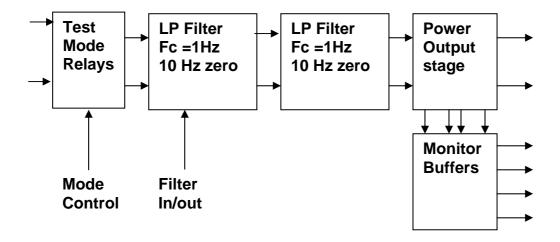
| Unit | Q_TOP33P | Serial No . | |
|---------------|----------|-------------|--|
| Test Engineer | Xen | | |
| Date | .3/3/10 | | |

Contents

- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP33P | Serial No |
|------|----------|-----------|
| | Xen | |
| _ | 3/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP33P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | 2/3/10 | | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP33P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 3/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | $\sqrt{}$ |
| 8 | PD3N | Photodiode C- | 16 | |
| 9 | PD4N | Photodiode D- | 17 | |

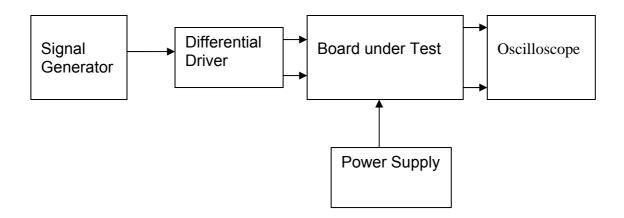
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | \checkmark |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | $\sqrt{}$ |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | \checkmark |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | \checkmark |
| 24 | 0V (TP3) | | |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Jnit | .Q TOP33P | .Serial No |
|------|-----------|------------|
| | .Xen | |
| Date | 3/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 11.97 | 1mV | √ |
| +15v TP4 | 14.82 | 1mV | √ |
| -15v TP6 | -14.96 | 5mV | \checkmark |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP33P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 3/3/10 | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | .Q TOP33P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | 3/3/10 | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.35 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | $\sqrt{}$ |
| Ch2 | 0.67 | 0.48 to 0.75v | √ |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP33P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | Xen | |
| Date | .3/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.25 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | .Q TOP33P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | Xen | |
| Date | .3/3/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.398 | Pin 7 to Pin 8 | 0.399 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | V |
| Ch2 | V |
| Ch3 | V |
| Ch4 | \checkmark |

| Unit | .Q TOP33P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | 3/3/10 | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 Ch1 | Ch1 | J3 pins 2,7 Ch2 | Ch2 | J3 pins 3,8 Ch3 o/p | Ch3 | J3 pins 4,9 Ch4 | Ch4 |
|------|--------------------|-------------|--------------------|-------------|------------------------|-------------|--------------------|----------|
| | o/p | stable ? | o/p | stable ? | | stable ? | o/p | stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.3 | V | -24.3 | V |
| -7v | -17.1 | V | -17.1 | V | -17.0 | V | -17.1 | V |
| -5v | -12.3 | V | -12.3 | V | -12.2 | V | -12.2 | V |
| -1v | -2.41 | V | -2.42 | V | -2.41 | V | -2.41 | V |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.4 | V | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.42 | |
| 5v | 12.1 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | √ | 17.0 | V | 17.0 | V | 17.0 | |
| 10v | 24.2 | 1 | 24.3 | V | 24.3 | V | 24.3 | |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|----------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP33P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 3/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----------|-----|
| Not Clipping? | $\sqrt{}$ | V | $\sqrt{}$ | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.58 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

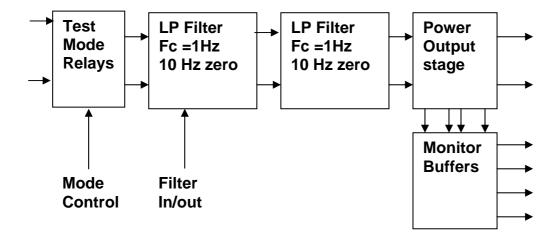
| Unit | .Q_ | TOP34P | .Serial No | | |
|---------------|-------|--------|----------------|------|--|
| Test Engineer | .Xer | n | | | |
| Date | .3/3/ | /10 | | | |

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- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Jnit | .Q TOP34P | Serial No |
|------|-----------|-----------|
| | .Xen | |
| Date | .3/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP34P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 3/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP34P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 3/3/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

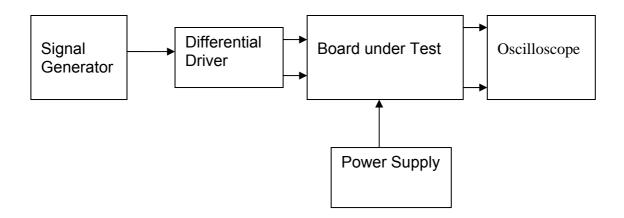
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | |
| 4 | Imon4P | 8 | √ |
| 5 | 0V | | |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP34P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 3/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.10 | 1mV | V |
| +15v TP4 | 14.92 | 1mV | V |
| -15v TP6 | -15.11 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP34P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 3/3/10 | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | V | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_ | _TOP34P | .Serial No | ٠ | |
|---------------|-----|---------|------------|---|--|
| Test Engineer | Xe | n | | | |
| Date | 3/3 | 3/10 | | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4 85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch4 | 3.4 | 3.3v to 3.7v | \checkmark |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP34P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | Xen | |
| Date | .3/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.25 | 3v to 3.4v | \checkmark |
| Ch3 | 3.3 | 3v to 3.4v | \checkmark |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP34P | .Serial No | |
|---------------|----------|------------|--|
| Test Engineer | Xen | | |
| Date | .3/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP34P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | ·Xen | | |
| Data | 3/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.4 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.0 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.2 | $\sqrt{}$ |
| -1v | -2.42 | V | -2.4 | V | -2.42 | V | -2.4 | $\sqrt{}$ |
| 0v | 0 | V | 0 | | 0 | V | 0 | $\sqrt{}$ |
| 1v | 2.41 | $\sqrt{}$ | 2.42 | | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | $\sqrt{}$ |
| 7v | 17.0 | V | 17.0 | √ | 17.0 | V | 17.0 | |
| 10v | 24.3 | V | 24.3 | √ | 24.3 | V | 24.3 | 1 |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|----------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP34P | Serial No |
|------|----------|-----------|
| | ·Xen | |
| Date | 3/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----------|-----|
| Not Clipping? | $\sqrt{}$ | V | $\sqrt{}$ | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.54 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

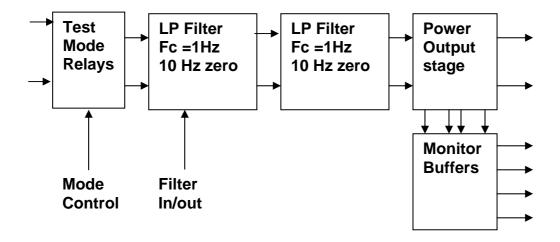
| Unit | .Q | TOP35P | Serial No | | |
|---------------|------|--------|---------------|------|------|
| Test Engineer | .Xe | n | | | |
| Date | .4/3 | 3/10 | | | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP35P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| _ | 4/3/10 | | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP35P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 3/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP35P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 3/3/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

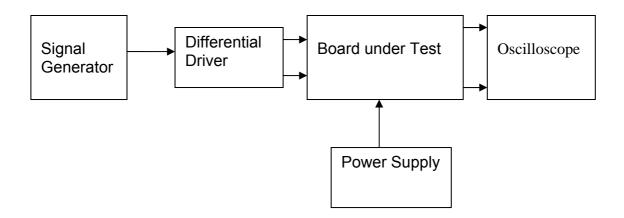
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | $\sqrt{}$ |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | $\sqrt{}$ |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ |
| 9 | Imon4N | 21 | √ |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | V |
| 10 | V+ (TP1) | +17v Supply | V |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | √ |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | √ |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP35P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 3/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.02 | 1mV | \checkmark |
| +15v TP4 | 14.95 | 1mV | \checkmark |
| -15v TP6 | -15.00 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP35P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 3/3/10 | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | | $\sqrt{}$ |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | V | |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | | $\sqrt{}$ | V |
| Ch2 | | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | √ | V | √ |

| Unit | Q TOP35P | .Serial No | |
|------|----------|------------|--|
| | Xen | | |
| Date | 4/3/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| n | 1 | Hz | |
|---|-----|----|--|
| v | ••• | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | V |
| Ch2 | 3.4 | 3.3v to 3.7v | V |
| Ch3 | 3.4 | 3.3v to 3.7v | V |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.68 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.46 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP35P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | Xen | |
| Date | .4/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.3 | 3v to 3.4v | √ |
| Ch3 | 3.3 | 3v to 3.4v | √ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.5 | 0.4v to 0.5v | √ |
| Ch2 | 0.49 | 0.4v to 0.5v | √ |
| Ch3 | 0.5 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP35P | Serial No |) | |
|---------------|----------|-----------|---|--|
| Test Engineer | Xen | | | |
| Date | 4/3/10 | | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP35P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 4/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | $\sqrt{}$ |
| -7v | -17.2 | V | -17.2 | V | -17.0 | V | -17.1 | $\sqrt{}$ |
| -5v | -12.3 | V | -12.3 | V | -12.2 | V | -12.2 | $\sqrt{}$ |
| -1v | -2.4 | V | -2.41 | V | -2.4 | V | -2.41 | $\sqrt{}$ |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | √ | 0 | $\sqrt{}$ |
| 1v | 2.41 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | |
| 7v | 17.0 | V | 17.1 | V | 17.0 | V | 17.0 | |
| 10v | 24.4 | V | 24.5 | V | 24.3 | V | 24.2 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|----------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | .Q TOP35P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 4/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----------|-----|
| Not Clipping? | $\sqrt{}$ | V | $\sqrt{}$ | V |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.56 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

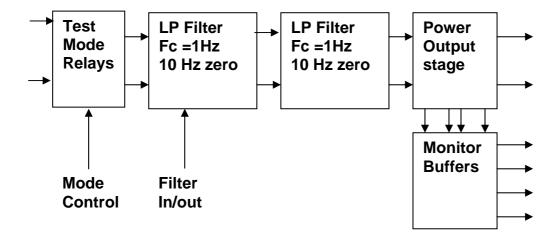
| Unit | .Q | TOP36P | .Serial No | | |
|---------------|------|--------|----------------|------|--|
| Test Engineer | .Xe | n | | | |
| Date | .4/3 | 3/10 | | | |

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- 2. Test Equipment
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- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP36P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP36P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP36P | .Serial No | |
|---------------|----------|------------|--|
| Test Engineer | Xen | | |
| Date | .4/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

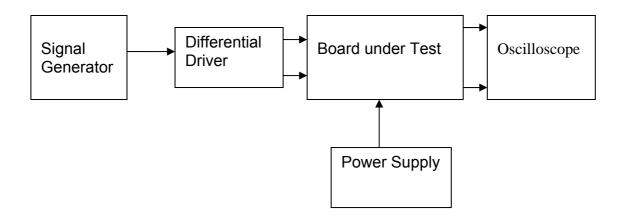
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | V |
| 6 | Imon1N | 18 | V |
| 7 | Imon2N | 19 | V |
| 8 | Imon3N | 20 | √ |
| 9 | Imon4N | 21 | √ |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | √ |
| 11 | V- (TP2) | -17v Supply | √ |
| 12 | V- (TP2) | -17v Supply | √ |
| 13 | 0V (TP3) | | √ |
| 22 | 0V (TP3) | | √ |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP36P | Serial No |
|------|----------|-----------|
| | erXen | |
| Date | 4/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.06 | 1mV | \checkmark |
| +15v TP4 | 14.93 | 1mV | \checkmark |
| -15v TP6 | -15.02 | 5mV | |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP36P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | | |
|---------|------|-----------|-----------|--|
| | ON | ON OFF | | |
| Ch1 | V | √ | V | |
| Ch2 | V | | $\sqrt{}$ | |
| Ch3 | V | | $\sqrt{}$ | |
| Ch4 | | √ | $\sqrt{}$ | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | .Q | TOP36P | Serial No |) |
|---------------|-----|--------|-----------|---|
| Test Engineer | .Xe | n | | |
| Date | | | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| ^ | | _ |
|---|-------|---|
| | н | 7 |
| | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | |
| Ch2 | 0.68 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.66 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.46 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | $Q_{}$ | TOP36P | Serial No | |
|---------------|--------|--------|-----------|--|
| Test Engineer | | | | |
| Date | .4/3 | 3/10 | | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.3 | 3v to 3.4v | \checkmark |
| Ch3 | 3.3 | 3v to 3.4v | $\sqrt{}$ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.5 | 0.4v to 0.5v | √ |
| Ch4 | 0.5 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP36P | Serial No | ٠ |
|----------------|----------|-----------|---|
| Test Engineer. | Xen | | |
| Date | 4/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP36P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Date | 4/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.3 | V | -24.3 | V | -24.4 | |
| -7v | -17.2 | V | -17.1 | V | -17.0 | V | -17.2 | V |
| -5v | -12.3 | V | -12.2 | V | -12.2 | V | -12.3 | |
| -1v | -2.42 | V | -2.41 | V | -2.4 | V | -2.4 | |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | √ | 0 | $\sqrt{}$ |
| 1v | 2.42 | $\sqrt{}$ | 2.42 | | 2.42 | \checkmark | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | √ | 12.2 | V | 12.2 | √ |
| 7v | 17.1 | V | 17.1 | √ | 17.1 | V | 17.1 | |
| 10v | 24.3 | V | 24.4 | V | 24.5 | V | 24.3 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP36P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | √ |
| Ch4 | 5v to 6v | 5.56 | |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

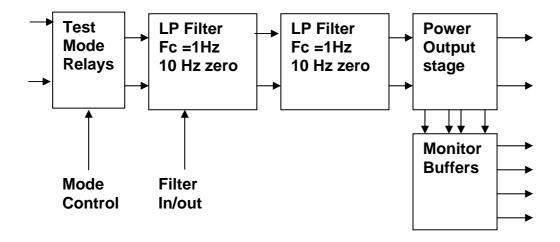
| Unit | .Q | TOP37P | Serial No . | | |
|---------------|-----|--------|-----------------|------|--|
| Test Engineer | .Xe | n | | | |
| Date | 4/3 | 3/10 | | | |

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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

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|------|-----------|-----------|
| | Xen | |
| Date | 4/3/10 | |

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Relay test box

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| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP37P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP37P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Date | 4/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

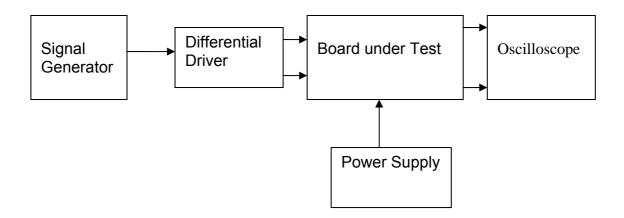
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | |
| 4 | Imon4P | 8 | √ |
| 5 | 0V | | |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP37P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 11.95 | 1mV | \checkmark |
| +15v TP4 | 14.92 | 1mV | \checkmark |
| -15v TP6 | -15.05 | 5mV | \checkmark |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP37P | Serial No . | |
|------|--------------------|-------------|--|
| | X <mark>e</mark> n | | |
| Date | 4/3/10 | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | √ | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit(| Q_TOP37P | Serial No |
|-------|----------|-----------|
| | Xen | |
| Date4 | J/3/10 | |

8. Corner frequency tests

Ch4

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

4.85

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | √ |
| Ch3 | 4.85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.35 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

4.7 to 5v

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.46 | 0.4v to 0.5v | V |
| Ch3 | 0.46 | 0.4v to 0.5v | V |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | Q TOP37P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | .4/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.35 | 3v to 3.4v | $\sqrt{}$ |
| Ch2 | 3.25 | 3v to 3.4v | $\sqrt{}$ |
| Ch3 | 3.3 | 3v to 3.4v | $\sqrt{}$ |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.5 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit(| Q_TOP37PSer | rial No |
|---------------|-------------|---------|
| Test Engineer | Xen | |
| Date4 | 1/3/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.397 | |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP37P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 4/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | V |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.1 | V |
| -5v | -12.3 | V | -12.2 | V | -12.3 | V | -12.2 | $\sqrt{}$ |
| -1v | -2.42 | √ | -2.41 | √ | -2.42 | $\sqrt{}$ | -2.42 | \checkmark |
| 0v | 0 | V | 0 | V | 0 | V | 0 | $\sqrt{}$ |
| 1v | 2.42 | \checkmark | 2.42 | $\sqrt{}$ | 2.41 | $\sqrt{}$ | 2.42 | √ |
| 5v | 12.2 | 1 | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | 1 | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.4 | V | 24.2 | V | 24.3 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP37P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 4/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | √ |
| Ch4 | 5v to 6v | 5.55 | |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

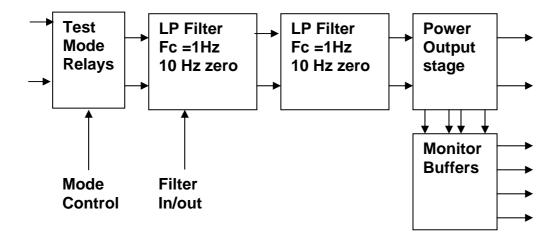
| Unit | .Q_ | TOP38P | .Serial No | | |
|---------------|------|--------|----------------|------|------|
| Test Engineer | .Xe | n | | | |
| Date | .5/3 | 3/10 | | | |

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- 1. Description
- 2. Test Equipment
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- 5. Test Set Up
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- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP38P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| _ | 5/3/10 | | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP38P | .Serial No |
|------|----------|------------|
| | Xen | |
| _ | 5/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Also, changed capacitors C50 and C51 from 4.7uF to the correct value of 10uF on CH1.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP38P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 5/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | $\sqrt{}$ |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

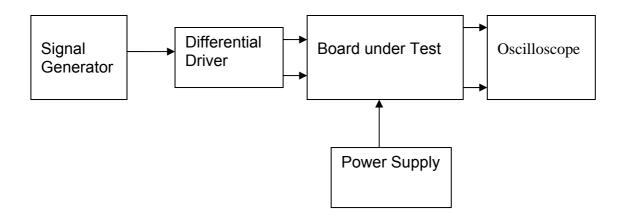
J5

| PIN | SIGNAL | То | J1 PIN | OK? |
|-----|--------|----|--------|--------------|
| 1 | Imon1P | | 5 | \checkmark |
| 2 | Imon2P | | 6 | \checkmark |
| 3 | Imon3P | | 7 | \checkmark |
| 4 | Imon4P | | 8 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | Imon1N | | 18 | \checkmark |
| 7 | Imon2N | | 19 | \checkmark |
| 8 | Imon3N | | 20 | |
| 9 | Imon4N | | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | V |
| 10 | V+ (TP1) | +17v Supply | V |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | √ |
| 13 | 0V (TP3) | | √ |
| 22 | 0V (TP3) | | √ |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP38P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 5/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 11.93 | 1mV | \checkmark |
| +15v TP4 | 14.93 | 1mV | \checkmark |
| -15v TP6 | -14.84 | 5mV | \checkmark |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP38P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 5/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | | |
|---------|------|-----------|-----------|--|
| | ON | OFF | | |
| Ch1 | V | √ | V | |
| Ch2 | V | | $\sqrt{}$ | |
| Ch3 | V | | $\sqrt{}$ | |
| Ch4 | | √ | | |

Test Switches

| Channel | Indi | Indicator | | |
|---------|----------|-----------|----------|--|
| | ON | OFF | | |
| Ch1 | | $\sqrt{}$ | V | |
| Ch2 | | $\sqrt{}$ | V | |
| Ch3 | V | $\sqrt{}$ | V | |
| Ch4 | √ | V | √ | |

| Unit | Q TOP38P | Serial No |
|---------------|----------|-----------|
| Test Engineer | Xen | |
| Date | 5/3/10 | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| , | ď | 1 | H | ľ | Z | |
|---|---|---|---|---|---|--|
| | | | | | | |
| | | | | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.9 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | √ |
| Ch2 | 3.35 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.68 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | V |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP38P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | .5/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.2 | 3v to 3.4v | |
| Ch2 | 3.3 | 3v to 3.4v | |
| Ch3 | 3.25 | 3v to 3.4v | √ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.46 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.49 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | √ |
| Ch2 | 0.16 | 0.15v to 0.16v | √ |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP38P | Serial No |
|---------------|----------|-----------|
| Test Engineer | Xen | |
| Date | 5/3/10 | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | V |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.395 | Pin 7 to Pin 8 | 0.396 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP38P | Serial No | |
|--------------|----------|-----------|--|
| Test Enginee | rXen | | |
| Data | 5/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.4 | V | -24.1 | |
| -7v | -17.1 | V | -17.2 | V | -17.1 | V | -17.0 | V |
| -5v | -12.3 | V | -12.3 | V | -12.2 | V | -12.1 | |
| -1v | -2.41 | V | -2.4 | V | -2.4 | V | -2.4 | |
| 0v | 0 | V | 0 | | 0 | V | 0 | $\sqrt{}$ |
| 1v | 2.42 | | 2.41 | | 2.42 | \checkmark | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | √ | 12.2 | √ | 12.2 | V | 12.0 | √ |
| 7v | 17.0 | V | 17.0 | √ | 17.0 | V | 16.9 | |
| 10v | 24.5 | 1 | 24.2 | √ | 24.4 | V | 24.2 | 1 |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | .Q TOP38P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 5/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|----------|----------|
| Not Clipping? | $\sqrt{}$ | V | √ | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch4 | 5v to 6v | 5.57 | $\sqrt{}$ |

LIGO Laboratory / LIGO Scientific Collaboration

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Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

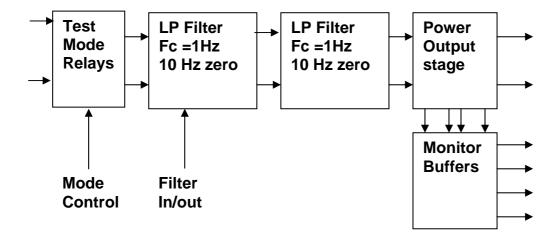
| Unit | .Q | TOP39P | .Serial No | | |
|---------------|------|--------|----------------|------|------|
| Test Engineer | .Xe | n | | | |
| Date | .5/3 | 3/10 | | | |

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- 3. Inspection
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- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP39P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | 5/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP39P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 5/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP39P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Date | 5/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

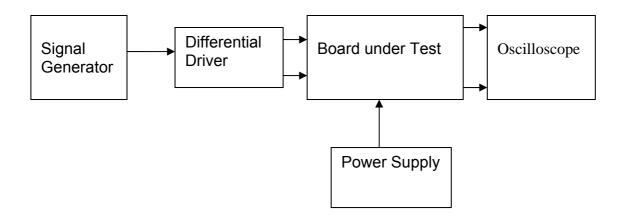
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | V |
| 8 | Imon3N | 20 | V |
| 9 | Imon4N | 21 | V |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | √ |
| 22 | 0V (TP3) | | √ |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | \checkmark |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | .Q TOP39P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 5/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.03 | 1mV | \checkmark |
| +15v TP4 | 14.98 | 1mV | \checkmark |
| -15v TP6 | -15.02 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP39P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 5/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | V | √ | √ |

Test Switches

| Channel | Indio | OK? | |
|---------|--------|----------|----------|
| | ON OFF | | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP39P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 5/3/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|-----------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| 0 | .1 | Hz |
|---|----|----|
| | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch4 | 3.4 | 3.3v to 3.7v | \checkmark |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.46 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.46 | 0.4v to 0.5v | V |
| Ch3 | 0.46 | 0.4v to 0.5v | V |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | $Q_{}$ | _TOP39P | Serial No | |
|---------------|--------|---------|-----------|--|
| Test Engineer | | | | |
| Date | .5/3 | 3/10 | | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | |
| Ch2 | 3.25 | 3v to 3.4v | V |
| Ch3 | 3.3 | 3v to 3.4v | V |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.5 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | √ |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification Pass/ | |
|-----|--------|---------------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP39P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 5/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP39P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Data | 5/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | |
| -7v | -17.2 | V | -17.1 | V | -17.1 | V | -17.0 | V |
| -5v | -12.3 | V | -12.2 | V | -12.3 | V | -12.2 | V |
| -1v | -2.42 | V | -2.41 | V | -2.4 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.2 | V | 24.3 | V | 24.2 | V | 24.3 | √ |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP39P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.55 | √ |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

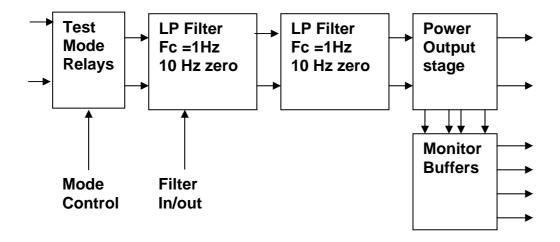
| Unit | .Q_TOP40P | Serial No | |
|---------------|-----------|-----------|--|
| Test Engineer | Xen | | |
| Date | .5/3/10 | | |

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- 1. Description
- 2. Test Equipment
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- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP40P | .Serial No |
|------|-----------|------------|
| | Xen | |
| Date | 5/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP40P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 5/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP40P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 5/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

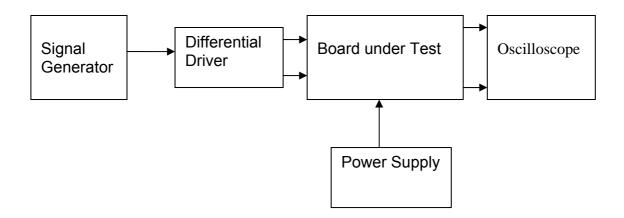
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | V |
| 3 | Imon3P | 7 | V |
| 4 | Imon4P | 8 | V |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | V |
| 8 | Imon3N | 20 | V |
| 9 | Imon4N | 21 | V |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | |
| 10 | V+ (TP1) | +17v Supply | |
| 11 | V- (TP2) | -17v Supply | V |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP40P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.01 | 1mV | |
| +15v TP4 | 14.96 | 1mV | |
| -15v TP6 | -15.03 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP40P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 5/3/10 | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | | |
|---------|------|-----------|----------|--|
| | ON | OFF | | |
| Ch1 | V | | V | |
| Ch2 | V | | | |
| Ch3 | V | | | |
| Ch4 | V | √ | √ | |

Test Switches

| Channel | Indi | Indicator | |
|---------|------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | $\sqrt{}$ | V |
| Ch3 | V | $\sqrt{}$ | V |
| Ch4 | V | | V |

| Unit | Q_ | _TOP40P | Serial No | |
|---------------|-----|---------|-----------|------|
| Test Engineer | Xe | n | | |
| Date | 5/3 | 3/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| ٠. | •• | - | | |
|----|----|---|--|--|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.35 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q | TOP40P | .Serial No | |
|---------------|------|--------|------------|--|
| Test Engineer | | | | |
| Date | .5/3 | 3/10 | | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.2 | 3v to 3.4v | √ |
| Ch3 | 3.2 | 3v to 3.4v | √ |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP40P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 5/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | V |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.396 | |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP40P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Data | 5/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.5 | V | -24.5 | V |
| -7v | -17.1 | V | -17.2 | V | -17.2 | V | -17.2 | V |
| -5v | -12.3 | V | -12.3 | V | -12.4 | V | -12.3 | V |
| -1v | -2.41 | V | -2.42 | V | -2.42 | V | -2.41 | V |
| 0v | 0 | V | 0 | $\sqrt{}$ | 0 | V | 0 | $\sqrt{}$ |
| 1v | 2.42 | V | 2.42 | V | 2.42 | $\sqrt{}$ | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.2 | V | 17.1 | V | 17.0 | V | 17.1 | V |
| 10v | -24.5 | 1 | 24.5 | V | 24.4 | V | 24.5 | √ |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|----------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP40P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 5/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.55 | $\sqrt{}$ |
| Ch3 | 5v to 6v | 5.56 | V |
| Ch4 | 5v to 6v | 5.55 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

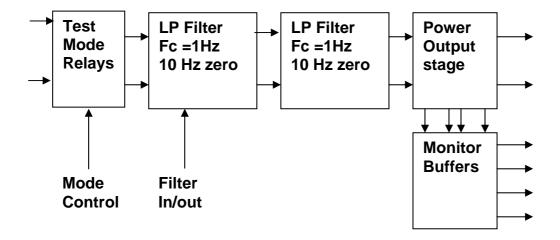
| Unit | Q_TOP41P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | .8/3/10 | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP41P | .Serial No |
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| _ | 8/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP41P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 8/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP41P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Date | 8/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | √ |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | |

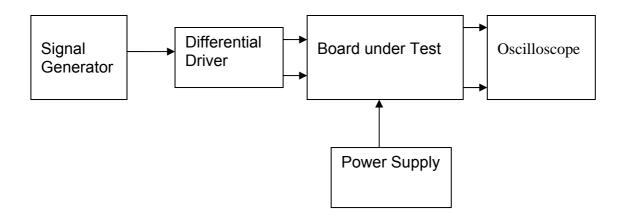
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | |
| 4 | Imon4P | 8 | √ |
| 5 | 0V | | |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | \checkmark |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | |
| 10 | V+ (TP1) | +17v Supply | |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | \checkmark |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP41P | .Serial No |
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| | Xen | |
| Date | 8/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.05 | 1mV | √ |
| +15v TP4 | 14.92 | 1mV | √ |
| -15v TP6 | -14.99 | 5mV | √ |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP41P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 8/3/10 | | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | | | V |
| Ch2 | $\sqrt{}$ | | V |
| Ch3 | | | V |
| Ch4 | | | V |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TOP41P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| | 8/3/10 | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 530 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | √ |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.35 | 3.3v to 3.7v | V |
| Ch4 | 3.4 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.66 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.46 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.46 | 0.4v to 0.5v | V |
| Ch3 | 0.46 | 0.4v to 0.5v | V |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP41P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | .8/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.2 | 3v to 3.4v | |
| Ch2 | 3.2 | 3v to 3.4v | |
| Ch3 | 3.2 | 3v to 3.4v | |
| Ch4 | 3.2 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.46 | 0.4v to 0.5v | √ |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | \checkmark |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP41P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 8/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.398 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.396 | $\sqrt{}$ |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP41P | Serial No | |
|----------------|----------|-----------|--|
| Test Engineer. | Xen | | |
| Date | 8/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.5 | V |
| -7v | -17.2 | V | -17.1 | V | -17.2 | V | -17.1 | V |
| -5v | -12.3 | V | -12.3 | V | -12.3 | V | -12.3 | V |
| -1v | -2.41 | V | -2.42 | V | -2.41 | V | -2.41 | V |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.42 | $\sqrt{}$ | 2.42 | | 2.42 | $\sqrt{}$ | 2.41 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | √ | 17.1 | V | 17.0 | V |
| 10v | 24.3 | V | 24.2 | V | 24.5 | V | 24.5 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP41P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 8/3/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----|----------|
| Not Clipping? | $\sqrt{}$ | V | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.57 | |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.55 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

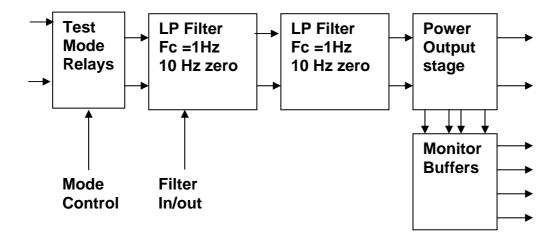
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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP42P | .Serial No |
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| Date | 8/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

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|------------------|------------------|---------|---------------|
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| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP42P | .Serial No |
|------|----------|------------|
| | Xen | |
| _ | 8/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP42P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 8/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | √ |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | |

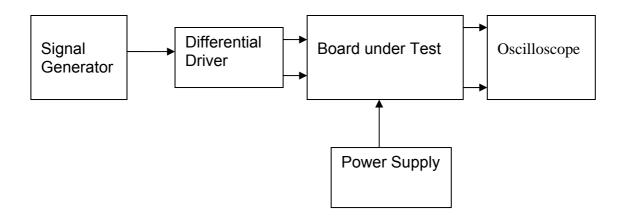
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | \checkmark |
| 3 | Imon3P | 7 | \checkmark |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | √ |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | √ |
| 22 | 0V (TP3) | | √ |
| 23 | 0V (TP3) | | √ |
| 24 | 0V (TP3) | | \checkmark |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP42P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 8/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator Output voltage Output noise Nomina | | | |
|--|--------|-----|-----------|
| | | | +/- 0.5v? |
| +12v TP5 | 11.99 | 1mV | V |
| +15v TP4 | 14.91 | 1mV | V |
| -15v TP6 | -15.06 | 5mV | |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP42P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 8/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|-----|-----|
| | ON | OFF | |
| Ch1 | | V | V |
| Ch2 | | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | .Q_TOP42P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | Xen | |
| Date | .8/3/10 | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| \mathbf{a} | - 4 | | _ |
|--------------|-----|---|---|
| u | _ 1 | н | 7 |
| | | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | √ |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.45 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | V |
| Ch3 | 0.69 | 0.48 to 0.75v | V |
| Ch4 | 0.66 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | V |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.46 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP42P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | .8/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.3 | 3v to 3.4v | √ |
| Ch3 | 3.3 | 3v to 3.4v | √ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.5 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | √ |
| Ch4 | 0.49 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP42P | .Serial No | |
|------|----------|------------|--|
| | Xen | | |
| Date | 8/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.203 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.203 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? |
|-----|-----------|--------------------|------------------|--------------------|----------------------|
| | | resistor | | | (+/- 0.1v) |
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.396 | |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.398 | |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.397 | |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP42P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 8/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.4 | V | -24.4 | V | -24.0 | V | -24.3 | V |
| -7v | -17.2 | V | -17.1 | V | -16.9 | V | -17.1 | V |
| -5v | -12.3 | V | -12.3 | V | -12.0 | V | -12.3 | V |
| -1v | -2.42 | $\sqrt{}$ | -2.41 | √ | -2.4 | $\sqrt{}$ | -2.4 | V |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.42 | \checkmark | 2.42 | $\sqrt{}$ | 2.4 | $\sqrt{}$ | 2.42 | √ |
| 5v | 12.2 | V | 12.2 | V | 12.0 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.0 | V |
| 10v | 24.3 | V | 24.3 | V | 24.3 | V | 24.3 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|----------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP42P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 8/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----|----------|
| Not Clipping? | $\sqrt{}$ | V | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.55 | |
| Ch2 | 5v to 6v | 5.56 | |
| Ch3 | 5v to 6v | 5.57 | V |
| Ch4 | 5v to 6v | 5.55 | |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

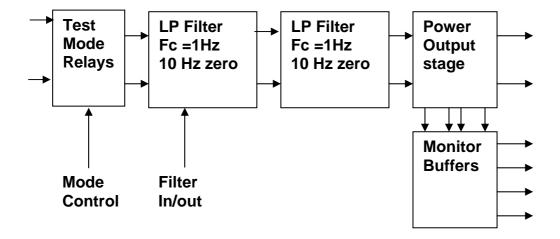
| Unit | .Q_TOP43P | Serial No | |
|---------------|-----------|-----------|--|
| Test Engineer | Xen | | |
| Date | .9/3/10 | | |

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- 2. Test Equipment
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- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP43P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | 9/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP43P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 3/2/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Also, IC4 and IC12 changed on CH3.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q TOP43P | Serial No |
|------|----------|-----------|
| | neerXen | |
| Date | 3/2/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | $\sqrt{}$ |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | $\sqrt{}$ |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

J5

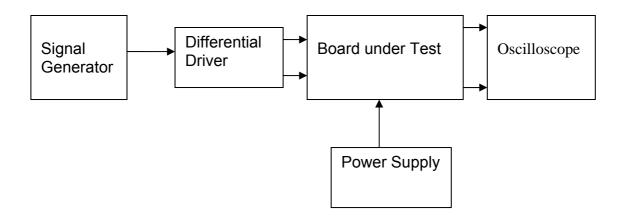
| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | $\sqrt{}$ |
| 2 | Imon2P | 6 | $\sqrt{}$ |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | \checkmark |
| 5 | 0V | | \checkmark |
| 6 | Imon1N | 18 | \checkmark |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | $\sqrt{}$ |
| 9 | Imon4N | 21 | $\sqrt{}$ |

Power Supply to Satellite box

J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----------|
| 9 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 10 | V+ (TP1) | +17v Supply | $\sqrt{}$ |
| 11 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 12 | V- (TP2) | -17v Supply | $\sqrt{}$ |
| 13 | 0V (TP3) | | $\sqrt{}$ |
| 22 | 0V (TP3) | | $\sqrt{}$ |
| 23 | 0V (TP3) | | $\sqrt{}$ |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q_TOP43P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | | | |
| Date | 3/2/10 | | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|-------------------|
| +12v TP5 | 12.03 | 1mV | |
| +15v TP4 | 14.92 | 1mV | |
| -15v TP6 | -15.04 | 5mV | |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP43P | Serial No |
|---------------|----------|-----------|
| Test Engineer | Xen | |
| Date | .3/2/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|----------|-----------|----------|
| | ON | OFF | |
| Ch1 | V | | V |
| Ch2 | V | | |
| Ch3 | V | | |
| Ch4 | √ | √ | √ |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_ | TOP43P. | Serial No | | |
|---------------|----|---------|---------------|------|------|
| Test Engineer | ٧a | n | | | |

Test EngineerXen....... Date3/2/10.....

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | V |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4.85 | 4.7 to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | $\sqrt{}$ |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | √ |
| Ch2 | 0.68 | 0.48 to 0.75v | √ |
| Ch3 | 0.68 | 0.48 to 0.75v | √ |
| Ch4 | 0.67 | 0.48 to 0.75v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q TOP43P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | | |
| Date | .3/2/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | V |
| Ch2 | 4.85 | 4.7v to 5v | |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.2 | 3v to 3.4v | \checkmark |
| Ch2 | 3.25 | 3v to 3.4v | \checkmark |
| Ch3 | 3.3 | 3v to 3.4v | \checkmark |
| Ch4 | 3.2 | 3v to 3.4v | $\sqrt{}$ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.48 | 0.4v to 0.5v | √ |
| Ch2 | 0.48 | 0.4v to 0.5v | |
| Ch3 | 0.49 | 0.4v to 0.5v | |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.15v to 0.16v | |
| Ch2 | 0.16 | 0.15v to 0.16v | |
| Ch3 | 0.16 | 0.15v to 0.16v | √ |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|-----------|
| Ch1 | 0.16 | 0.14v to 0.16v | |
| Ch2 | 0.16 | 0.14v to 0.16v | |
| Ch3 | 0.16 | 0.14v to 0.16v | V |
| Ch4 | 0.16 | 0.14v to 0.16v | V |

| Unit | Q TOP43P. | Serial No | |
|----------------|-----------|---------------|------|
| Test Engineer. | Xen | | |
| Date | 3/2/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.395 | Pin 3 to Pin 4 | 0.397 | |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | V |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | V |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | V |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | $\sqrt{}$ |
| Ch2 | V |
| Ch3 | V |
| Ch4 | V |

| Unit | .Q TOP43P | .Serial No | |
|---------------|-----------|------------|--|
| Test Engineer | .Xen | | |
| Date | .3/2/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.5 | $\sqrt{}$ | -24.4 | |
| -7v | -17.0 | V | -17.2 | V | -17.0 | V | -17.0 | |
| -5v | -12.2 | V | -12.2 | V | -12.2 | V | -12.2 | |
| -1v | -2.4 | V | -2.41 | V | -2.4 | V | -2.4 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.0 | V | 17.0 | V | 17.0 | V | 17.1 | V |
| 10v | 24.5 | V | 24.5 | V | 24.3 | V | 24.5 | √ |

| Unit | Serial No | |
|---------------|-----------|--|
| Test Engineer | | |
| Date | | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|-------------------|-------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP43P | Serial No |
|---------------|----------|-----------|
| Test Engineer | | |
| Date | 3/2/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|----------|--------------|-----|
| Not | \checkmark | √ | \checkmark | V |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----------|
| Ch1 | 5v to 6v | 5.56 | $\sqrt{}$ |
| Ch2 | 5v to 6v | 5.57 | V |
| Ch3 | 5v to 6v | 5.53 | V |
| Ch4 | 5v to 6v | 5.56 | V |

LIGO Laboratory / LIGO Scientific Collaboration

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30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

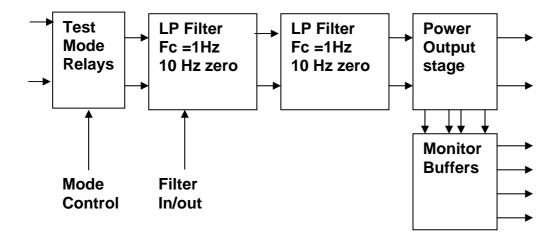
| Unit | .Q_ | TOP44P | Serial No | o | |
|---------------|------|--------|-----------|---|--|
| Test Engineer | .Xe | n | | | |
| Date | .9/3 | 3/10 | | | |

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- 1. Description
- 2. Test Equipment
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- 12. Crosstalk Tests
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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | .Q TOP44P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | 9/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP44P | .Serial No |
|------|----------|------------|
| | Xen | |
| _ | 9/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Also, replaced IC12 on CH4.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP44P | Serial N | ۱o | |
|---------------|----------|-----------------|----|--|
| Test Engineer | Xen | | | |
| Date | 8/3/10 | | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

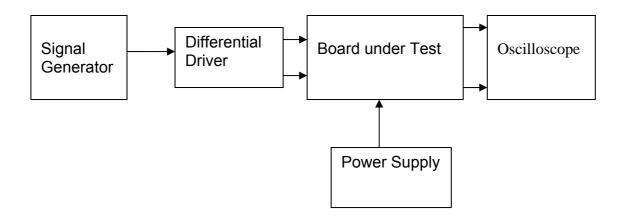
J5

| PIN | SIGNAL | То | J1 PIN | OK? |
|-----|--------|----|--------|--------------|
| 1 | Imon1P | | 5 | \checkmark |
| 2 | Imon2P | | 6 | \checkmark |
| 3 | Imon3P | | 7 | \checkmark |
| 4 | Imon4P | | 8 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | Imon1N | | 18 | \checkmark |
| 7 | Imon2N | | 19 | \checkmark |
| 8 | Imon3N | | 20 | |
| 9 | Imon4N | | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | V |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | V |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP44P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 8/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.02 | 1mV | \checkmark |
| +15v TP4 | 14.91 | 1mV | \checkmark |
| -15v TP6 | -14.99 | 5mV | $\sqrt{}$ |

| All Outputs smooth DC, no oscillation? | 1 | / |
|--|---|---|
|--|---|---|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP44P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 8/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|---|
| | ON | OFF | |
| Ch1 | V | | |
| Ch2 | V | | |
| Ch3 | V | | V |
| Ch4 | | | |

Test Switches

| Channel | Indi | Indicator | |
|---------|----------|-----------|-----------|
| | ON | OFF | |
| Ch1 | √ | V | V |
| Ch2 | V | | |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | √ | √ | |

| Unit | $Q_{}$ | _TOP44P | .Serial No | |
|------|--------|---------|------------|------|
| | | en | | |
| Date | | | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | √ |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | |
| Ch2 | 4.85 | 4.7 to 5v | |
| Ch3 | 4.85 | 4.7 to 5v | √ |
| Ch4 | 4.85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.35 | 3.3v to 3.7v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | V |
| Ch4 | 0.67 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | $\sqrt{}$ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | √ |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | Q_TOP44P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 8/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.3 | 3v to 3.4v | \checkmark |
| Ch2 | 3.3 | 3v to 3.4v | \checkmark |
| Ch3 | 3.3 | 3v to 3.4v | $\sqrt{}$ |
| Ch4 | 3.3 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.5 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.49 | 0.4v to 0.5v | √ |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | \checkmark |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP44P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 8/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | $\sqrt{}$ |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | $\sqrt{}$ |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | √ |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.396 | Pin 15 to Pin 16 | 0.398 | \checkmark |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP44P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 9/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.4 | V | -24.4 | V | -24.4 | V | -24.4 | V |
| -7v | -17.1 | V | -17.0 | V | -17.1 | V | -17.1 | V |
| -5v | -12.3 | V | -12.2 | V | -12.2 | V | -12.3 | V |
| -1v | -2.42 | V | -2.4 | V | -2.42 | V | -2.41 | V |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | √ | 0 | $\sqrt{}$ |
| 1v | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ | 2.41 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | V | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | V | 17.1 | V | 17.0 | V |
| 10v | 24.3 | V | 24.2 | V | 24.4 | V | 24.3 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP44P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 9/3/10 | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|--------------|--------------|--------------|-----------|
| Not | \checkmark | \checkmark | \checkmark | $\sqrt{}$ |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.57 | |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.57 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

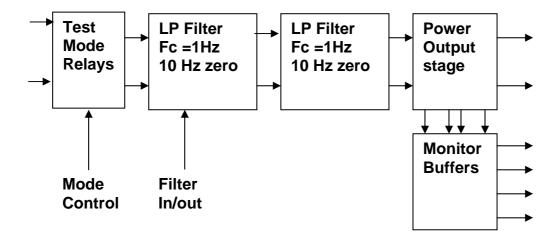
| Unit | Q_TOP45P | .Serial No |
|---------------|----------|------------|
| Test Engineer | Xen | |
| Date | 9/3/10 | |

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- 1. Description
- 2. Test Equipment
- 3. Inspection
- 4. Continuity Checks
- 5. Test Set Up
- 6. Power
- 7. Relay operation
- 8. Corner Frequency Tests
- 9. Monitor Outputs
- 10. Distortion
- 11. DC Stability
- 12. Crosstalk Tests
- 13. Dynamic range

1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP45P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 9/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP45P | .Serial No |
|------|----------|------------|
| | Xen | |
| - | 9/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Also, changed capacitors C50 and C51 on all channels from 4.7uF to 10uF.

I inks:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | .Q TOP45P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | 9/3/10 | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | $\sqrt{}$ |
| 5 | 0V | | | $\sqrt{}$ |
| 6 | PD1N | Photodiode A- | 14 | $\sqrt{}$ |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | \checkmark |
| 9 | PD4N | Photodiode D- | 17 | $\sqrt{}$ |

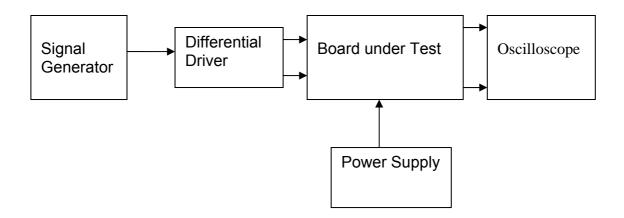
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|-----|
| 1 | Imon1P | 5 | |
| 2 | Imon2P | 6 | |
| 3 | Imon3P | 7 | |
| 4 | Imon4P | 8 | |
| 5 | 0V | | |
| 6 | Imon1N | 18 | |
| 7 | Imon2N | 19 | |
| 8 | Imon3N | 20 | |
| 9 | Imon4N | 21 | |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|-----|
| 9 | V+ (TP1) | +17v Supply | |
| 10 | V+ (TP1) | +17v Supply | √ |
| 11 | V- (TP2) | -17v Supply | |
| 12 | V- (TP2) | -17v Supply | V |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | √ |
| 25 | 0V (TP3) | | √ |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP45P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 9/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.06 | 1mV | $\sqrt{}$ |
| +15v TP4 | 14.90 | 1mV | √ |
| -15v TP6 | -15.09 | 5mV | V |

| All Outputs smooth DC, no oscillation? | ٧ | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q TOP45P | Serial No |
|------|----------|-----------|
| | Xen | |
| Date | 9/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indicator | | OK? |
|---------|-----------|----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|-----|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | V | V | V |
| Ch4 | V | V | V |

| Unit | Q_ | _TOP45P | Serial No | |
|---------------|-----|---------|-----------|------|
| Test Engineer | Xē | en | | |
| Date | 9/3 | 3/10 | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

| 0 | .1 | Hz |
|---|----|----|
| | | |

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 4.85 | 4.7 to 5v | \checkmark |
| Ch2 | 4.85 | 4.7 to 5v | \checkmark |
| Ch3 | 4.85 | 4.7 to 5v | \checkmark |
| Ch4 | 4.85 | 4.7 to 5v | \checkmark |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 3.35 | 3.3v to 3.7v | \checkmark |
| Ch2 | 3.4 | 3.3v to 3.7v | \checkmark |
| Ch3 | 3.45 | 3.3v to 3.7v | V |
| Ch4 | 3.4 | 3.3v to 3.7v | V |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.67 | 0.48 to 0.75v | V |
| Ch2 | 0.68 | 0.48 to 0.75v | V |
| Ch3 | 0.68 | 0.48 to 0.75v | V |
| Ch4 | 0.68 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | √ |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP45P | Serial No |
|------|-----------|-----------|
| | Xen | |
| Date | .9/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | V |
| Ch4 | 4.85 | 4.7v to 5v | √ |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.2 | 3v to 3.4v | |
| Ch2 | 3.2 | 3v to 3.4v | |
| Ch3 | 3.2 | 3v to 3.4v | |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.14v to 0.16v | √ |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Unit | Q TOP45P | .Serial No | |
|---------------|----------|------------|--|
| Test Engineer | Xen | | |
| Date | 9/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|------------------|--------------------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | \checkmark |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.202 | \checkmark |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | \checkmark |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | \checkmark |
| 2 | 0.37-0.41 | 0.396 | Pin 7 to Pin 8 | 0.397 | \checkmark |
| 3 | 0.37-0.41 | 0.395 | Pin 11 to Pin 12 | 0.397 | \checkmark |
| 4 | 0.37-0.41 | 0.397 | Pin 15 to Pin 16 | 0.399 | $\sqrt{}$ |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | √ |
| Ch2 | √ |
| Ch3 | √ |
| Ch4 | \checkmark |

| Unit | Q_TOP45P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 9/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.4 | V | -24.5 | V | -24.4 | V |
| -7v | -17.1 | V | -17.1 | V | -17.1 | V | -17.0 | V |
| -5v | -12.3 | V | -12.2 | V | -12.2 | V | -12.2 | V |
| -1v | -2.4 | V | -2.41 | V | -2.41 | V | -2.41 | |
| 0v | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ | 0 | $\sqrt{}$ |
| 1v | 2.42 | $\sqrt{}$ | 2.41 | | 2.42 | $\sqrt{}$ | 2.42 | $\sqrt{}$ |
| 5v | 12.2 | V | 12.2 | √ | 12.2 | V | 12.2 | V |
| 7v | 17.1 | V | 17.0 | √ | 17.0 | V | 17.0 | V |
| 10v | 24.5 | V | 24.3 | V | 24.4 | V | 24.5 | V |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT CHANNEL | OUTPUT CHANNEL | Output at 10Hz | Maximum o/p | @ Freq |
|------------------|-------------------|----------------|----------------|--------|
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP45P | Serial No | |
|------|----------|-----------|------|
| | Xen | | |
| Date | 9/3/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|-----------|-----------|-----------|-----------|--------------|
| Not | $\sqrt{}$ | $\sqrt{}$ | $\sqrt{}$ | \checkmark |
| Clipping? | | | | |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.56 | |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.57 | V |

LIGO Laboratory / LIGO Scientific Collaboration

LIGO-T0900231-v3 Advanced LIGO UK

30 November 2009

Quad TOP Coil Driver Board Test Plan

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html

http://www.eng-external.rl.ac.uk/advligo/papers_public/ALUK_Homepage.htm

QUAD TOP COIL DRIVER BOARD TEST PLAN

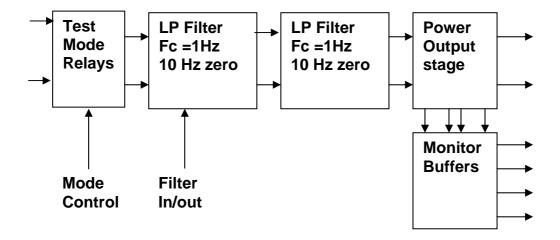
| Unit | Q_TOP47P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 10/3/10 | | |

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1. Description

Block diagram



2. Description

Each TOP Driver board consists of four identical channels and three power regulators, which provide regulated power to the four channels.

Taking the diagram block by block, the first block contains relays which switch the circuit between the normal inputs and the test inputs.

The second block contains a low pass filter with a corner frequency of 1Hz, followed by a complimentary zero at 10Hz. To a good approximation, the gain is reduced by a factor of 0.7 at 1Hz, the attenuation increases at a rate of 20dB/decade up to the corner frequency of the zero at 10 Hz, after which the characteristic levels off. This filter may be switched in and out as required by relay control. Operational amplifiers follow which have a gain of 1.2.

The third block contains a filter with a similar characteristic, the main difference being that this filter is not switchable.

This is followed by the output buffer stage, consisting of an operational amplifier followed by a power driver buffer. The power driver is unity gain, and the operational amplifier provides the gain in this stage. The loop is closed around the buffer/operational amplifier pair. The current limit is set to 0.25A.

The outputs are buffered by unity gain voltage followers which drive the monitor board.

| Unit | Q TOP47P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 10/3/10 | |

2. Test equipment

Power supplies (At least +/- 20v variable, 1A)
Signal generator (capable of delivering 10v peak, 0.1Hz to 10 KHz))
Digital oscilloscope
Analogue oscilloscope
Agilent Dynamic Signal Analyser (or similar)
Low noise Balanced Driver circuit
Relay test box

Record the Models and serial numbers of the test equipment used below.

| Unit (e.g. DVM) | Manufacturer | Model | Serial Number |
|------------------|------------------|---------|---------------|
| DVM | Fluke | 115 | |
| Signal Generator | Agilent | 33250A | |
| Oscilloscope | ISO-TECH | ISR622 | |
| PSU*2 | Farnell | L30-2 | |
| DVM | Fluke | 77111 | |
| DVM | TENMA | 72-7730 | |
| V/I calibrator | Time Electronics | 1044 | |

| Unit | Q TOP47P | .Serial No |
|------|----------|------------|
| | Xen | |
| _ | 9/3/10 | |

3. Inspection

Workmanship

Inspect the general workmanship standard and comment: $\sqrt{}$

Removed capacitors C102, C103, C104 and C105 on all channels and replaced C102 and C103 with 33pF polypropylene capacitors.

Also, U1 has been replaced.

Links:

Check that links W4 and W5 are present on each channel. If not, connect them.

| Unit | Q_TOP47P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 9/3/10 | | |

4. Continuity Checks

J2

| PIN | SIGNAL | DESCRIPTION | To J1 PIN | OK? |
|-----|--------|---------------|-----------|--------------|
| 1 | PD1P | Photodiode A+ | 1 | \checkmark |
| 2 | PD2P | Photodiode B+ | 2 | \checkmark |
| 3 | PD3P | Photodiode C+ | 3 | \checkmark |
| 4 | PD4P | Photodiode D+ | 4 | \checkmark |
| 5 | 0V | | | \checkmark |
| 6 | PD1N | Photodiode A- | 14 | \checkmark |
| 7 | PD2N | Photodiode B- | 15 | \checkmark |
| 8 | PD3N | Photodiode C- | 16 | V |
| 9 | PD4N | Photodiode D- | 17 | \checkmark |

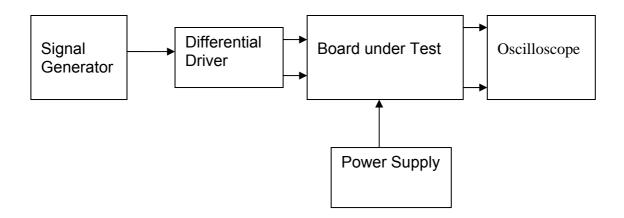
J5

| PIN | SIGNAL | To J1 PIN | OK? |
|-----|--------|-----------|--------------|
| 1 | Imon1P | 5 | \checkmark |
| 2 | Imon2P | 6 | $\sqrt{}$ |
| 3 | Imon3P | 7 | $\sqrt{}$ |
| 4 | Imon4P | 8 | $\sqrt{}$ |
| 5 | 0V | | $\sqrt{}$ |
| 6 | Imon1N | 18 | $\sqrt{}$ |
| 7 | Imon2N | 19 | \checkmark |
| 8 | Imon3N | 20 | √ |
| 9 | Imon4N | 21 | \checkmark |

Power Supply to Satellite box J1

| PIN | SIGNAL | DESCRIPTION | OK? |
|-----|----------|-------------|--------------|
| 9 | V+ (TP1) | +17v Supply | \checkmark |
| 10 | V+ (TP1) | +17v Supply | \checkmark |
| 11 | V- (TP2) | -17v Supply | \checkmark |
| 12 | V- (TP2) | -17v Supply | \checkmark |
| 13 | 0V (TP3) | | V |
| 22 | 0V (TP3) | | V |
| 23 | 0V (TP3) | | V |
| 24 | 0V (TP3) | | $\sqrt{}$ |
| 25 | 0V (TP3) | | V |

5. TEST SET UP



Note:

- (1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.
- (2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

Connections:

Differential signal inputs to the board under test:

```
J3 pins 1, 2, 3, 4 = positive input
J3 pins 6, 7, 8, 9 = negative input
J3 pin 5 = ground
```

Power

```
J1 pin 9, 10 = +16.5v
J1 pin 11,12 = -16.5
J1 pins 22, 23, 24, 25 = 0v
```

Outputs

| Ch1+ = J4 pin 1 | Ch1- = J4 pin 9 |
|-----------------|------------------|
| Ch2+ = J4 pin 3 | Ch2- = J4 pin 11 |
| Ch3+ = J4 pin 5 | Ch3- = J4 pin 13 |
| Ch4+ = J4 pin 7 | Ch4- = J4 pin 15 |

| Unit | Q TOP47P | .Serial No |
|------|----------|------------|
| | Xen | |
| Date | 9/3/10 | |

6. Power

Check the polarity of the wiring:

3 Pin Power Connector

Set the power supply outputs to zero.

Connect power to the unit

Increase the voltages on the supplies to +/-3V.

Determine that the supply polarities are correct on TP1 and TP2.

If they are, increase input voltages to +/- 16.5v.

Record the output voltages, measured on a 4 digit DVM, from each regulator Observe the output on an analogue oscilloscope, set to AC. Measure and record the peak to peak noise on each output.

Record regulator outputs:

| Regulator | Output voltage | Output noise | Nominal +/- 0.5v? |
|-----------|----------------|--------------|----------------------|
| +12v TP5 | 12.08 | 1mV | V |
| +15v TP4 | 14.92 | 1mV | V |
| -15v TP6 | -15.05 | 5mV | V |

| All Outputs smooth DC, no oscillation? | V | |
|--|---|--|
|--|---|--|

Record Power Supply Currents

| Supply | Current |
|--------|---------|
| +16.5v | 400mA |
| -16.5v | 300mA |

If the supplies are correct, proceed to the next test.

| Unit | Q_TOP47P | Serial No |
|---------------|----------|-----------|
| Test Engineer | Xen | |
| Date | 9/3/10 | |

7. Relay Operation

Operate each relay in turn.
Observe its operation. LEDs should illuminate when the relays are operated.

Filter

| Channel | Indi | Indicator | |
|---------|------|-----------|-----------|
| | ON | OFF | |
| Ch1 | V | √ | V |
| Ch2 | V | | $\sqrt{}$ |
| Ch3 | V | | $\sqrt{}$ |
| Ch4 | | √ | |

Test Switches

| Channel | Indicator | | OK? |
|---------|-----------|----------|----------|
| | ON | OFF | |
| Ch1 | V | V | V |
| Ch2 | V | V | V |
| Ch3 | | V | V |
| Ch4 | | V | V |

| Unit | Q_TC |)P47P | Serial No | |
|---------------|--------|-------|-----------|------|
| Test Engineer | Xen | | | |
| Date | 9/3/10 |) | | |

8. Corner frequency tests

Apply a signal to the input, amplitude 1v peak, Frequency 1Hz.

8.1 Both Filters out: Remove W4 and W5

Measure and record the Peak to Peak output between TP9 and TP13

at 1Hz, 10Hz and 100Hz for each channel

| | 1Hz | 10Hz | 100Hz | Specification | Pass/Fail |
|-----|------|------|-------|---------------|--------------|
| Ch1 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch2 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch3 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |
| Ch4 | 4.85 | 5.0 | 5.0 | 4.7v to 5v | \checkmark |

8.2 Switched filter in: Remove W5, insert W4

Switch in the filter and test the response at 0.1Hz, 1Hz, 10Hz, 100Hz and 1kHz. Measure and record the Peak to Peak output between TP9 and TP13.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7 to 5v | $\sqrt{}$ |
| Ch2 | 4.85 | 4.7 to 5v | $\sqrt{}$ |
| Ch3 | 4.85 | 4.7 to 5v | V |
| Ch4 | 4.85 | 4.7 to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.4 | 3.3v to 3.7v | |
| Ch2 | 3.4 | 3.3v to 3.7v | √ |
| Ch3 | 3.4 | 3.3v to 3.7v | √ |
| Ch4 | 3.4 | 3.3v to 3.7v | |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.68 | 0.48 to 0.75v | |
| Ch2 | 0.67 | 0.48 to 0.75v | V |
| Ch3 | 0.67 | 0.48 to 0.75v | √ |
| Ch4 | 0.66 | 0.48 to 0.75v | V |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 0.47 | 0.4v to 0.5v | |
| Ch2 | 0.47 | 0.4v to 0.5v | |
| Ch3 | 0.47 | 0.4v to 0.5v | V |
| Ch4 | 0.47 | 0.4v to 0.5v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.47 | 0.4v to 0.5v | √ |
| Ch4 | 0.46 | 0.4v to 0.5v | √ |

| Unit | .Q_TOP47P | Serial No |
|---------------|-----------|-----------|
| Test Engineer | .Xen | |
| Date | .10/3/10 | |

8.3 Fixed filter in: Remove W4, insert W5 Measure and record the peak to peak output between TP9 and TP13 at 0.1Hz. Repeat for 1Hz, 10Hz, 100Hz, and 1KHz.

0.1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 4.85 | 4.7v to 5v | |
| Ch2 | 4.85 | 4.7v to 5v | V |
| Ch3 | 4.85 | 4.7v to 5v | √ |
| Ch4 | 4.85 | 4.7v to 5v | V |

1Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|-----------|
| Ch1 | 3.3 | 3v to 3.4v | √ |
| Ch2 | 3.2 | 3v to 3.4v | √ |
| Ch3 | 3.25 | 3v to 3.4v | √ |
| Ch4 | 3.25 | 3v to 3.4v | √ |

10Hz

| | Output | Specification | Pass/Fail |
|-----|--------|---------------|--------------|
| Ch1 | 0.49 | 0.4v to 0.5v | \checkmark |
| Ch2 | 0.47 | 0.4v to 0.5v | \checkmark |
| Ch3 | 0.48 | 0.4v to 0.5v | \checkmark |
| Ch4 | 0.48 | 0.4v to 0.5v | √ |

100Hz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch2 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.15v to 0.16v | \checkmark |
| Ch4 | 0.16 | 0.15v to 0.16v | √ |

1kHz

| | Output | Specification | Pass/Fail |
|-----|--------|----------------|--------------|
| Ch1 | 0.16 | 0.14v to 0.16v | √ |
| Ch2 | 0.16 | 0.14v to 0.16v | \checkmark |
| Ch3 | 0.16 | 0.14v to 0.16v | √ |
| Ch4 | 0.16 | 0.14v to 0.16v | √ |

| Jnit | Q TOP47P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
|)ate | 10/3/10 | | |

9. Monitor Outputs

Remove W4 and W5. With a 39 ohm dummy load on each channel, apply a 1v r.m.s input at 10Hz and compare the differential output differential output on each monitor pair for each channel.

Voltage monitors

| Ch. | Nominal | Output: TP9 to TP13 | Monitor Pins Monitor Voltage Pin 1 to Pin 2 1.202 Pin 5 to Pin 6 1.203 Pin 9 to Pin 10 1.202 | | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|------------------------|--|-------|------------------------------------|
| 1 | 1.16-1.28 | 1.202 | Pin 1 to Pin 2 | 1.202 | |
| 2 | 1.16-1.28 | 1.202 | Pin 5 to Pin 6 | 1.203 | V |
| 3 | 1.16-1.28 | 1.202 | Pin 9 to Pin 10 | 1.202 | V |
| 4 | 1.16-1.28 | 1.202 | Pin 13 to Pin 14 | 1.202 | V |

Current monitors

| Ch. | Nominal | Output across coil resistor | Monitor Pins | Monitor Voltage | Pass/Fail: Equal? (+/- 0.1v) |
|-----|-----------|-----------------------------------|------------------|--------------------|------------------------------------|
| 1 | 0.37-0.41 | 0.396 | Pin 3 to Pin 4 | 0.397 | |
| 2 | 0.37-0.41 | 0.397 | Pin 7 to Pin 8 | 0.398 | |
| 3 | 0.37-0.41 | 0.396 | Pin 11 to Pin 12 | 0.397 | |
| 4 | 0.37-0.41 | 0.395 | Pin 15 to Pin 16 | 0.397 | |

10. Distortion

Filter out. Increase input voltage to 10v peak, f = 1kHz. Dummy 39 Ohm loads. Observe the voltage across each load with an oscilloscope.

| | Distortion Free? |
|-----|------------------|
| Ch1 | \checkmark |
| Ch2 | \checkmark |
| Ch3 | \checkmark |
| Ch4 | \checkmark |

| Unit | Q_TOP47P | Serial No | |
|---------------|----------|-----------|--|
| Test Engineer | Xen | | |
| Date | 10/3/10 | | |

11. DC Stability

Use the precision voltage source via a break out box on the input (J3). All filters off. Record the differential output voltage between TP7 and TP11. Check stability while slowly increasing the output voltage. (Link W2 in)

| | J3 pins 1,6 | | J3 pins 2,7 | | J3 pins 3,8 | | J3 pins 4,9 | |
|------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|
| | Ch1 o/p | Ch1 stable ? | Ch2 o/p | Ch2 stable ? | Ch3 o/p | Ch3 stable ? | Ch4 o/p | Ch4 stable ? |
| -10v | -24.5 | V | -24.5 | V | -24.4 | V | -24.5 | V |
| -7v | -17.2 | V | -17.1 | V | -17.1 | V | -17.2 | V |
| -5v | -12.2 | V | -12.2 | V | -12.2 | V | -12.3 | V |
| -1v | -2.41 | V | -2.41 | V | -2.4 | V | -2.41 | |
| 0v | 0 | V | 0 | V | 0 | V | 0 | V |
| 1v | 2.42 | V | 2.42 | V | 2.42 | V | 2.42 | V |
| 5v | 12.2 | V | 12.2 | V | 12.1 | V | 12.2 | V |
| 7v | 17.1 | V | 17.1 | V | 17.0 | V | 17.1 | V |
| 10v | 24.3 | V | 24.5 | V | 24.3 | V | 24.5 | √ |

| Unit | .Serial No |
|---------------|------------|
| Test Engineer | |
| Date | |

12. Crosstalk Tests

The purpose of these tests is to determine the level of crosstalk between each of the channels. As this is a lengthy test, and is mainly a function of board layout, it may be decided to perform the full test on a sample board only, and repeat the quick test on subsequent units.

12.1 Full Test

As crosstalk is a function of board layout, this test is only necessary on a sample basis.

Use the HP Dynamic signal analyser to measure the cross talk between adjacent channels.

Apply the source, set at 1v r.m.s, to each channel in turn, via the differential driver, while grounding the inputs to adjacent channels.

Measure the transfer function to adjacent channels.

Record the maximum outputs on adjacent channels, and record the frequency at which this occurs. (Assuming an output signal is detectable).

| INPUT | OUTPUT | Output at | Maximum | @ Freq |
|-----------|-----------|-----------|---------|--------|
| CHANNEL | CHANNEL | 10Hz | o/p | |
| Channel 1 | Channel 2 | | | |
| Channel 2 | Channel 1 | | | |
| Channel 2 | Channel 3 | | | |
| Channel 3 | Channel 2 | | | |
| Channel 3 | Channel 4 | | | |
| Channel 4 | Channel 3 | | | |

| Unit | Q TOP47P | Serial No | |
|------|----------|-----------|--|
| | Xen | | |
| Date | 10/3/10 | | |

13. Dynamic Range Tests

In this test, the board is tested at maximum dynamic range. Connect a 39 Ohm, 1W (or more) load resistor to the output of each channel. Switch out the input filter. Apply a 10v peak sinusoidal signal at 10Hz to the input to the input. Check that the signal on TP10 on one of the channels is 10v peak.

Observe the differential output voltage across the load resistors with an oscilloscope. Check that the waveforms are not clipping.

| | Ch1 | Ch2 | Ch3 | Ch4 |
|---------------|-----------|-----|-----|----------|
| Not Clipping? | $\sqrt{}$ | V | V | √ |

If the waveforms are not clipping, measure the output peak differential voltage across each load resistor, and record it in the table below.

| | Theoretical o/p | Measured | OK? |
|-----|-----------------|----------|-----|
| Ch1 | 5v to 6v | 5.56 | |
| Ch2 | 5v to 6v | 5.57 | |
| Ch3 | 5v to 6v | 5.55 | V |
| Ch4 | 5v to 6v | 5.55 | V |