LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Technical Note LIGO-E080541-v5 11/29/10

Quick Start Guide
Optical Timing Distribution System
Advanced LIGO

Imre Bartos, Rolf Bork, Maxim Factourovich, Jay Heefner, Szabolcs Márka,
Zoltán Raics, Paul Schwinberg and Daniel Sigg

This is an internal working note
of the LIGO Project.

California Institute of Technology
LIGO Project – MS 51-33
Pasadena CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project, MIT NW22-295,
185 Albany St.,Cambridge, MA 02139 USA
Phone (617) 253 4824
Fax (617) 253 7014
E-mail: info@ligo.mit.edu

Columbia University
Columbia Astrophysics Laboratory
Pupin Hall - MS 5247
New York NY 10027
Phone (212) 854-8209
Fax (212) 854-8121
E-mail: geco.cu@gmail.com

WWW: http://www.ligo.caltech.edu

Quick Start Guide: Optical Timing Distribution System for Advanced LIGO

This document provides a Quick Start Guide for the Optical Timing Distribution System of Advanced LIGO. Its intended purpose is to facilitate quick system deployment.

FEATURES

- Synchronized clocks
- Low phase noise
- GPS/UTC synchronization
- Multi-level self diagnostics
- Master/FanOut/Slave modules
- Scalable star topology
- Optical fiber coupled nodes
- Automatic fiber delay correction
- Flexible platform (i.e., FPGA)
- Open source
    - hardware,
    - firmware (FPGA) and
    - software (communication with external computer)
- Expandable hardware
    - 64 avail. LVDS lines – different platforms can be designed and connected

1. Overview

The Advanced LIGO Optical Timing Distribution System (OTD) provides synchronized timing information to detector subsystems. It synchronizes its central component (central node) to an external timing source, such as a GPS Receiver synchronized to Coordinated Universal Time (UTC). It synchronizes the remotely located nodes of the rest of the system to this central node. The remote nodes are then used to provide timing signals and diagnostics to AdvLIGO subsystems, therefore maintain their synchronization to UTC.

The OTD provides synchronized (i) 2^N clock signals, (ii) 1 pulse per second (thereafter, '*1PPS*') signal and (iii) so-called *DuoTone* signals (sum of 960 Hz and 961 Hz sinusoids phase synchronized to the 1PPS). These signals are used to clock external devices and to inject traceable timing diagnostics/calibration information. Nodes of the OTD can be located anywhere within 10km from each other, and the OTD automatically compensates for this distance while synchronizing.

The central unit of the OTD is called *'Master'* (LIGO-D070011 & LIGO-D080094). The Master board features an internal Oven Controlled Crystal Oscillator (thereafter, *'OCXO'*) that has excellent phase noise characteristics and naturally operates on a 2^N base frequency. The Master board provides synchronized timing information (2^{23} Hz clock signal and 1PPS signal) to other parts of the system: up to 16 FanOut and/or Slave boards.

FanOut boards (LIGO-D070011) are subcomponents of the OTD system. They receive timing information from the Master board or another FanOut board, and provide synchronized timing information (2^{23} Hz clock signal and 1PPS signal, identical to timing information from the Master board) to up to 16 more FanOut and/or Slave boards.

Slave boards (LIGO-D070071) are at the end of the OTD system chain. They receive timing information from a Master or FanOut board. They provide 1PPS/UTC synchronized 2^{16}Hz clock, GATE, and DuoTone signals to devices external to the OTD system. Each Slave board assembly incorporates a DuoTone board (LIGO-D080335) as a communication interface.

Status information of each board is readily shown by LEDs located on each front panel and can also be transmitted through the internet for data logging purposes. On the Master and FanOut boards, both the upstream and downstream synchronization status is shown by LEDs on the front panel, while the Slaves indicate the upstream synchronization status.

2. Front and Rear Panel Functions

2.1 Master/FanOut Board Front Panel

The front panels of the Master and FanOut boards have identical connectors and LEDs (see Figure 1). The only difference between them is the names 'Timing Master' and 'Timing Fanout'. Below, we describe the function of each connector and LED, indicating the differences between the roles of the two board types.

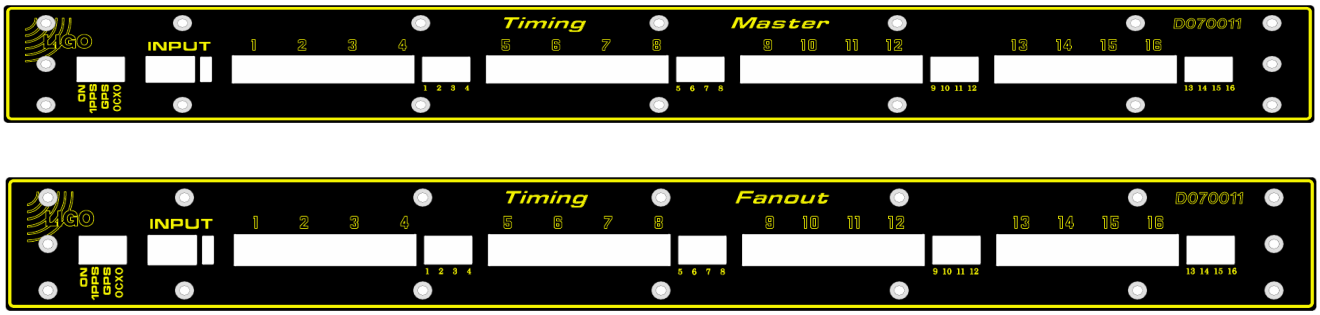


Figure 1. Master and FanOut board front panels (D080517-C).

ON LED – indicates that the Master board is on and is ready to distribute timing information.

2. It toggles every time the board's internal clock generates a 1PPS signal, therefore it is ON for one second and OFF for the next second (thereafter, '*½ Hz blink*') if the board operates properly.
3. It is constantly OFF (thereafter, '*OFF*') if the board is turned OFF and/or does not generate 1PPS signals.

1PPS LED[1] – indicates that an external 1PPS signal is received by the Master board through the *1PPS IN* connector (see rear panel, Figure 2).

1. It is *OFF* if the board does not receive a signal (e.g. the *1PPS IN* cable is disconnected).

- It exhibits *½ Hz blink* if it receives 1PPS signal.

GPS LED[2] - indicates that the internal GPS signal is received by the Master board through the GPS connector (see rear panel, Figure 2).

- It is OFF if no internal GPS receiver board is attached to the Master board.
- It exhibits *2 Hz blink* (on for 250 millisecond and off for the next 250ms) if the GPS receiver board is attached to the Master board but the GPS antenna is disconnected, or if the internal GPS receiver board is NOT locked to satellites.

It exhibits *½ Hz blink* if the GPS antenna is connected and the internal failover GPS receiver board is locked properly. This indicates that the GPS operates properly.

[1] This LED is NOT USED on FanOut boards.
[2] This LED is NOT USED on FanOut boards.

OCXO LED[3] – indicates the proper operation of the OCXO on the Master board.

1. It is OFF if OCXO is NOT present (therefore the module is a FanOut).
2. It exhibits *2 Hz blink* if OCXO is present but it is not locked to the external 1PPS.
3. It exhibits *½ Hz blink* if OCXO is present and is locked, toggling every time the OCXO generates a 1PPS signal.

INPUT[4] Connector– is a 2xLC Female fiber connector. The FanOut board receives timing and timing diagnostics information from a Master or FanOut board through this connector. It should be connected to one of the 16 numbered output connectors (*Output*) on the front panel of a Master or FanOut board upstream

INPUT LED[5] – indicates that timing information is received through the INPUT connector on the front panel of the FanOut board.

- It exhibits *2 Hz blink* if the INPUT connector is connected to a Master or FanOut board (front panel) and the board is *NOT* synchronized to the upstream clock.
- It exhibits *½ Hz blink* if the board is synchronized to the incoming 1PPS signal, i.e. properly.

1, 2, …, 16 Connectors - identical 2xLC Female connectors (on removable SFP transceiver modules) for *Output*. They are used to transmit and receive timing and timing diagnostics information from FanOut or Slave boards via optical fibers. They should be connected to the INPUT connectors on the front panels of FanOut or Slave boards.

- **1, 2, …, 16 LEDs** – they provide visual feedback on the synchronization status of the FanOut or Slave boards connected to the corresponding *Output* connectors. Each LED is *OFF* if the corresponding *Output* connector is not connected to an operating FanOut or Slave board.
- Each LED exhibits *2 Hz blink* if a FanOut or Slave board is connected to the corresponding *Output* connector but it is NOT LOCKED.
- Each LED exhibits *½ Hz blink* if a FanOut or Slave board connected to the corresponding *Output* connector is LOCKED.

[3] This LED is NOT USED on FanOut boards.
[4] The INPUT connector is NOT USED on the Master board (any input received on the Master board INPUT connector is ignored).
[5] The information received through the INPUT connector is NOT USED by the Master board. However, the INPUT LED does indicate signal reception on the INPUT connector (i.e. toggling every time it receives a 1PPS signal).

2.2 Master Board Rear Panel

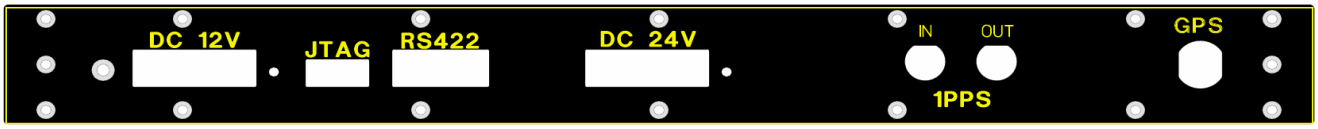


Figure 2. Master board rear panel (D080517-D).

DC 12V and DC 24V Connectors – both are D-sub 3w3 Male (FCI D3W3P36A6GX08LF) power supply connectors, one of them is a 12 VDC (min 40W) input, while the other one is 24VDC (min 10W). Facing the rear panel, the leftmost is the positive voltage pin, the middle is the ground pin, while the rightmost pin is not connected.

JTAG Connector – the board can be programmed using a computer through this connector.

RS422 Connector – is a DB9 Female connector. It sends status and other diagnostic information to a remote host computer or a Universal Device Server (e.g. Lantronix).

1PPS IN and 1PPS OUT Connectors - the Master board can receive an external 1PPS signal through its 1PPS IN connector, and send out a 1PPS signal synchronized to its internal clock through its 1PPS OUT connector. Both are BNC Female connectors and use TTL voltage levels.

GPS Connector – is an N Female input connector that can be connected to a GPS antenna and receive UTC GPS signal which is processed by the GPS board attached to the Master board.

Additional *blue LEDs* are located next to each power supply connector. They indicate the proper operation of the power supplies. If a connector is receiving the required power, the blue LED next to it is ON, otherwise it is OFF.

2.3 FanOut Board Rear Panel

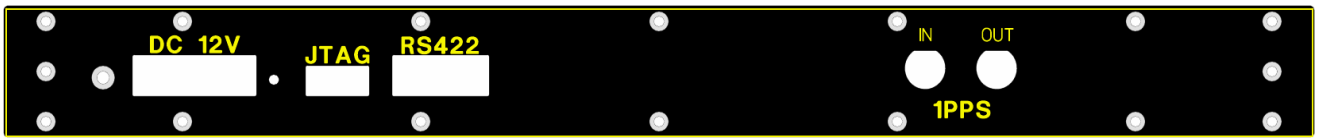


Figure 3. FanOut board rear panel (D080518-D).

DC 12V Connector – is a D-sub 3w3 Male (FCI D3W3P36A6GX08LF) power supply connector with 12 VDC (min 40W) input. Facing the rear panel, the leftmost is the positive voltage pin, the middle is the ground pin, while the rightmost pin is not connected.

JTAG Connector – the board can be programmed using a computer through this connector.

RS422 Connector – is a DB9 Female connector. It sends status and other diagnostic information to a remote host computer.

1PPS IN and 1PPS OUT Connectors – on the FanOut board, the 1PPS IN connector is NOT USED. The FanOut board sends out a 1PPS signal synchronized to its internal clock through its 1PPS OUT connector (BNC Female, uses TTL voltage levels).

An additional ***blue* LED** is located next to the power supply connector. It indicates the proper operation of the power supply. If the required power is received, the blue LED is ON, otherwise it is OFF.

2.4 Slave Board Front Panel

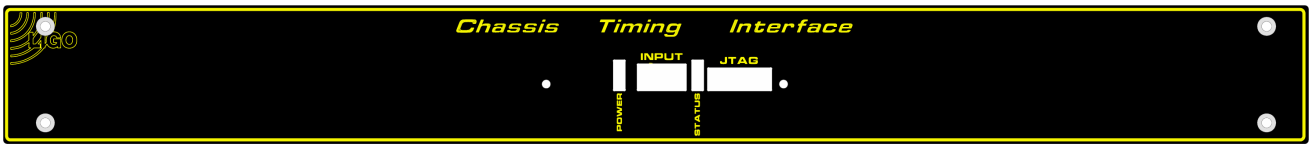


Figure 4. Slave board front panel. The image shows the connectors and LEDs of the Slave board. There might be other connectors or LEDs depending on other integrated parts of the Chassis Timing Interface.

POWER LED – is ON if the Slave board is ON, otherwise it is OFF.

INPUT Connector – is a 2xLC Female fiber connector. The Slave board transceives timing and timing diagnostics information from and to a Master or FanOut board through this connector. It should be connected to one of the 16 numbered output connectors (*Output*) on the front panel of a Master or FanOut board.

INPUT LED – indicates that timing information is received through the INPUT connector on the front panel of the Slave board.

- It exhibits *2 Hz blink* if the INPUT connector is connected to a Master or FanOut board (front panel) and the board is *NOT* synchronized to the upstream clock.
- It exhibits *½ Hz blink* if the board is synchronized to the incoming 1PPS signal, i.e.the board operates properly.

JTAG Connector – the board can be programmed using a computer through this connector.

2.5 Slave Board Rear Connector

DC 12V – is an SL 5.08/2 power supply connector with 12 VDC (min 15W) required input. Facing the rear panel, the left pin is the positive voltage, and the right pin is the ground.

2.6 DuoTone Board Connections

The DuoTone board (LIGO-D080335) is attached to the top of the Slave board. The external connections of the board are shown in Figure 5. The DuoTone board has six I/O headers (P3 – P8), of which P4, P5, P7 and P8 are presently used and these are described below.

P4 - configurable output header, with 4 possible outputs: DO[3..0]. DO0 outputs the Gate Signal (see section 3 for description), while DO[3..1] are set to GND.

P5 - configurable input header, with 6 possible inputs: DI[5..0]. DI0 is used for Gate Request Signal input (see section 3 for description), while DI[5..1] are not in use.

P7 - DAC clock output header with the following outputs:

CLOCK0, CLOCK4	-	DAC_CLK
CLOCK1, CLOCK5	-	**NOT** (DAC_CLK)
CLOCK2, CLOCK6	-	DAC_CLK **AND** GATE
CLOCK3, CLOCK7	-	**NOT** (DAC_CLK **AND** GATE)

where DAC_CLK is a 2^{16} Hz TTL clock signal, with its rising edge synchronized to the rising edge of the UTC 1PPS; **NOT** and **AND** are logic functions. See Section 6 for description of GATE signal and DAC clock signal.

P8 - DuoTone and DuoTone clock output header.

1. DUOTONE 0 and 1 are used for DuoTone signal outputs. The 960 Hz and 961 Hz DuoTone sinusoid components have equal weights in the sum, and both are at zero phase at the rising edge of the UTC 1PPS.
2. CLOCK_DUOTONE[1..0] are available for future use.

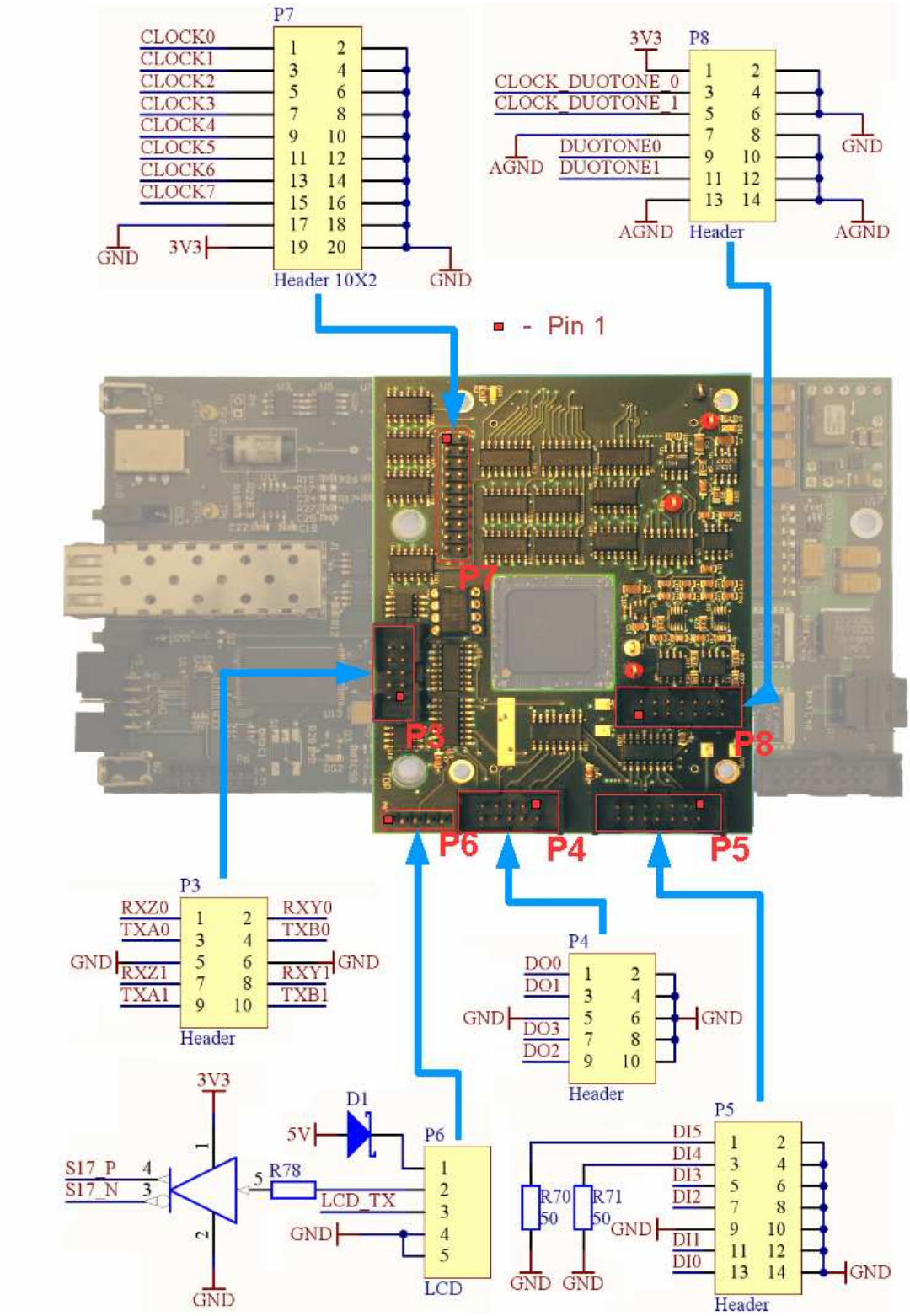


Figure 5 External connections of the DuoTone interface board.

3. Quick Start Guide to the Global OTD Assembly

The following steps (1-8) are also depicted in the Appendix.

3.1 Turn on Boards

1. Master board - connect 12 VDC (min 40W) and 24 VDC (min 10W) power supplies to the **DC 12V** and **DC 24V** connectors on the rear panel, respectively.
2. FanOut board - connect 12 VDC (min 40W) power supply to the **DC 12V** connector on the rear panel.
3. Slave board - connect 12 VDC (min 15W) power supply to the **DC 12V** connector on the rear panel.

3.2 Connect Boards

4. Master board - Connect the external 1PPS source, e.g. a GPS receiver, to the **1PPS IN** connector.
5. Master board - Connect a 3V GPS antenna to the **GPS** connector (note that only 3V antennas can be used). If the external 1PPS source on the **1PPS IN** connector is not available, the board will use 1PPS from the GPS antenna. Serially connect a GPS Lightning Arrestor between the GPS antenna and the Master board. If the distance between the Antenna and the Master board exceeds 200ft, serially connect GPS Line Amplifiers between the Antenna and the Master board.
6. FanOut and Slave boards - Connect the **INPUT** connector of each FanOut board and Slave board to one of the numbered **[1..16]** *Output* connectors of the appropriate Master or FanOut board to which the FanOut or Slave board should be synchronized.
7. Slave board – connect DAC board I/O to the appropriate pins of the DuoTone board.
8. OPTIONAL: To be able to transfer diagnostic information to a remote computer from the OTD, connect the **RS422** connector of the Master and FanOut boards to an external device server (Lantronix UDS2100). Connect the external device server to the Internet using an Ethernet connector.

3.3 Check Proper Operation of Boards[6]

9. When the power supply connectors are connected and the powers are on, the blue LEDs next to each power supply connector on Master or FanOut boards should be ON.

[6] On the front and rear panel of the OTD board, LEDs indicate board status. The four possible states are:
- OFF
- ON
- 2 Hz blink – the LED is on for 250ms and off for the next 250ms. The sign of improper operation.
- ½ Hz blink – the LED is on for one second and off for the next second. The sign of proper operation.

10. When the power supply is connected, the **POWER** LED on Slave boards should be ON.
11. If a Master or FanOut board is turned on, the **ON** LED should exhibit *½ Hz blink*.
12. If the Master board receives proper 1PPS signal through its **1PPS IN** connector, the **1PPS** LED should exhibit *½ Hz blink*.
13. If the Master board receives proper 1PPS signal through its **GPS** connector, the **GPS** LED should exhibit *½ Hz blink*.
14. If a FanOut board receives proper 1PPS signal through its **INPUT** connector, the **INPUT** LED should exhibit *½ Hz blink*.
15. If a Slave board receives proper 1PPS signal from a Master or FanOut board through its INPUT connector, the **INPUT** LED should exhibit *½ Hz blink*.
16. If the Master board is turned on and is connected to an external 1PPS source, it starts locking its OCXO to the external 1PPS signal. This can take up to a few minutes as locking is done through a low pass filter to filter out high frequency noise. When OCXO is properly locked, the **OCXO** LED exhibits *½ Hz blink*.
17. If a FanOut or Slave board is connected to one of the 16 Output connectors of a Master or FanOut board, and their internal clocks are locked, the corresponding **[1..16]** LEDs on both ends of the connection should exhibit *½ Hz blink*.

~

Under proper operating conditions,

- **Master board**: **ON** LED, **OCXO** LED and either **1PPS** LED or **GPS** LED exhibits *½ Hz blink*.
- **FanOut board**: **ON** LED and **INPUT** LED exhibit synchronous *½ Hz blink*.
- **Slave board: POWER** LED is ON and **INPUT** LED exhibits *½ Hz blink*.
- **Master and FanOut boards: [1..16]** *Output* LEDs exhibit *½ Hz blink* if their corresponding [1..16] *Output* connectors are connected to properly operating FanOut or Slave boards.

~

4. Slave Output Signals

The purpose of the Slave is to provide synchronized clock, gate and DuoTone signals to the ADC/DAC boards. Besides a constant and synchronized clock signal, the Slave board also defines when to start the conversion process as shown in.Figure 6.

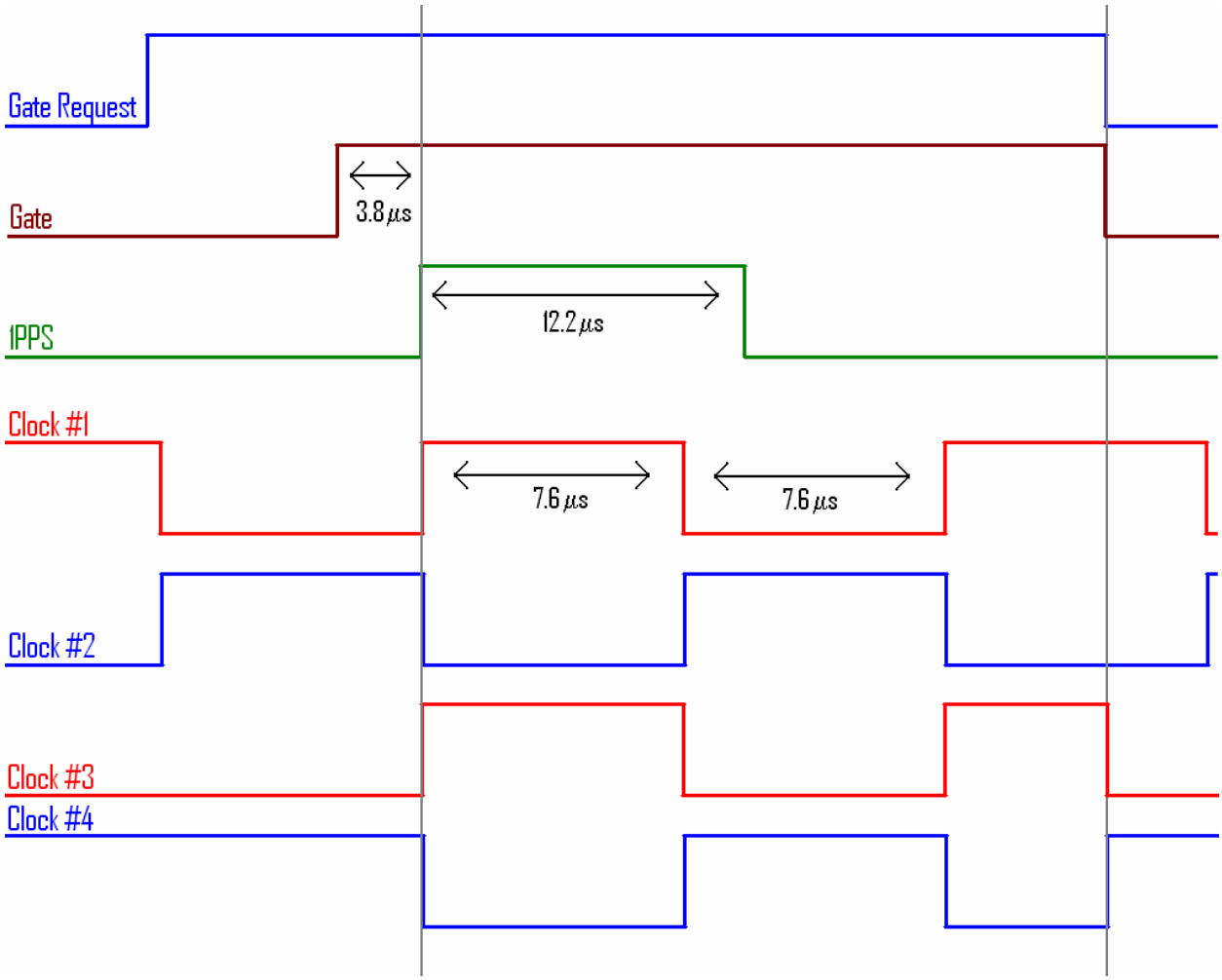


Figure 6. Timing of Gate Request, Gate, 1PPS and ADC/DAC clock signals.

Gate and Gate Request: Some ADC/DAC boards need a separate 2^{16}Hz Clock signal and a Gate signal. A conversion happens at the rising edge of each clock. The ADC/DAC board does not send the acquired data upstream until the Gate signal goes high. Consequently a properly timed Clock/Gate signal set can ensure that the first communicated conversion happens exactly at the rising edge of the 1PPS/UTC second tic. The Slave ensures that the Clock is synchronized to 1PPS/UTC and that the Gate rising edge is placed just right preceding the 1PPS/UTC rising edge. In practice, this is determined based on the user input that sends a Gate Request signal to the Slave board. Gate Request informs the Slave that conversion should start at the next available 1PPS signal

rising edge. In response, the Slave issues a Gate signal to the ADC/DAC boards ~4 µs before the consecutive 1PPS signal rising edge (after the arrival to the Gate Request signal). A 180° phase shifted Clock signal is also provided if needed. See Gate Request, Gate, 1PPS, Clock#1 and Clock#2 signal timing in Figure 6.

Gated Clock: Some DAC/ADC boards do not have separate Clock and Gate inputs, only a Clock input. These converter boards are able to do the conversion at the first incoming Clock rising edge. Therefore, the Slave also provides gated clock signals. After the Gate Request signal turns on, the Gated Clocks will turn on at the next consecutive rising edge of the 1PPS/UTC signal. A 180° phase shifted Clock signal is also provided if needed. See Gate Request, Gate, 1PPS, Clock#3 and Clock#4 signal timing in Figure 6.

The Gate and Gated Clock signals turn off immediately when Gate Request turns off.

APPENDIX A. Fiber Transceivers and Cables for the Timing System

The Advanced LIGO ODT uses SFP (Small Form Factor Pluggable) fiber transceivers which are rated for 100base-FX and/or OC-3. There are 2 types: a 1300nm LED based multi-mode module and a 1300nm laser based single-mode module. The multi-mode transceiver modules for 1000base-SX use a 880nm LED and are not interchangeable with the 100base-FX/OC-3 modules. Single-mode fiber transceivers need to have a range of at least 4km (intermediate range modules) for LIGO applications.

Supported Fiber Transceiver Modules

Type	Manufacturer	Part Number	Distributor	Order Number
multi-mode	Avago	HFBR-57E0PZ	Mouser	630-HFBR-57E0PZ
			Avnet	HFBR-57E0PZ
			Newark	74K5206
		HFBR-57E0LZ	Mouser	630-HFBR-57E0LZ
			Avnet	HFBR-57E0LZ
			Newark	74K5205
	Finisar	FTLF1217P2BTL	Digi-Key	775-1011-ND
		FTLF1217P2WTL	Avnet	FTLF1217P2WTL
single-mode	Avago	AFCT-5760TPZ	Mouser	630-AFCT-5760TPZ
			Avnet	AFCT-5760TPZ
			Newark	02M9340
		AFCT-5760TLZ	Mouser	630-AFCT-5760TLZ
			Avenet	AFCT-5760TLZ
			Newark	02M9339
	Finisar	FTLF1323P1BTR	Digi-Key	775-1019-ND
			Avnet	FTLF1323P1BTR

Cables

The fiber transceivers use LC connectors and either single-mode or multi-mode LC fiber patch cables have to be used.

APPENDIX B. Specifications

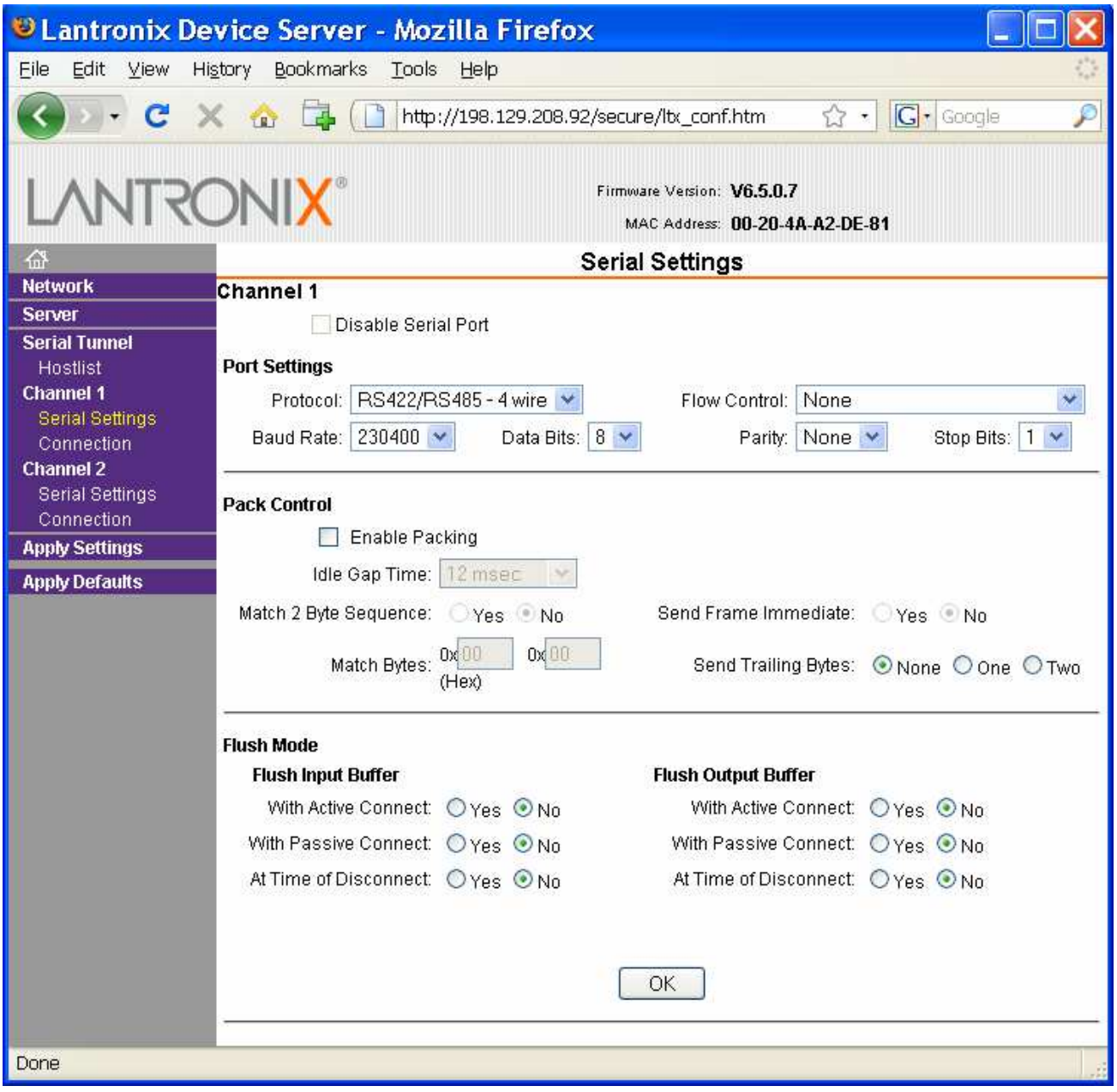
Module	I/O type	Connector	
Master	Input	1PPS IN	TTL
		GPS	3 VDC
		JTAG	
	Output	1PPS OUT	TTL
FanOut	Input	JTAG	
	Output	1PPS OUT	TTL
Slave	Input	JTAG	

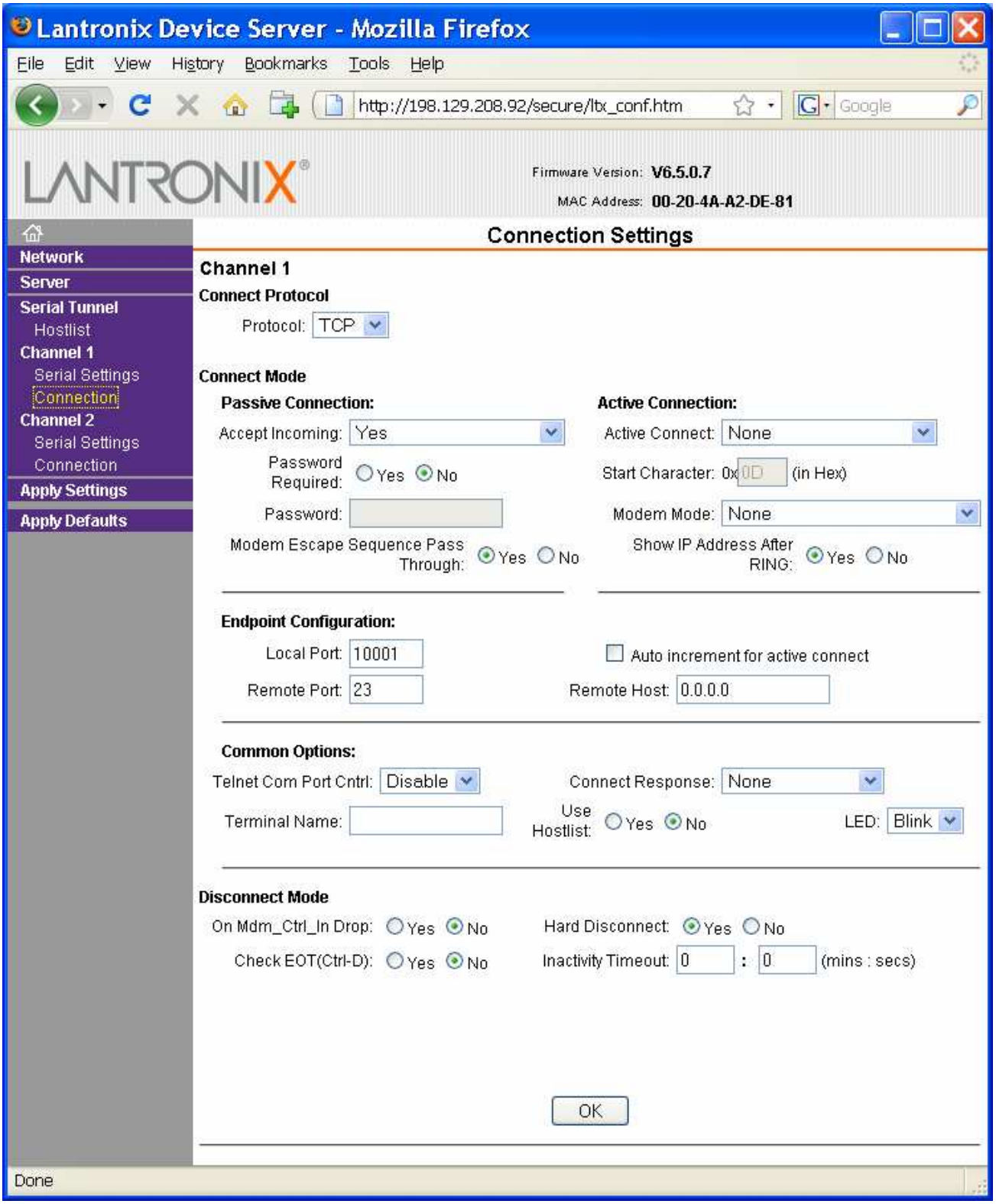
Power Requirement:

Master board: 12 VDC (min 40W)
24 VDC (min 10W)
FanOut board: 12 VDC (min 40W)
Slave board: 12 VDC (min 15W)

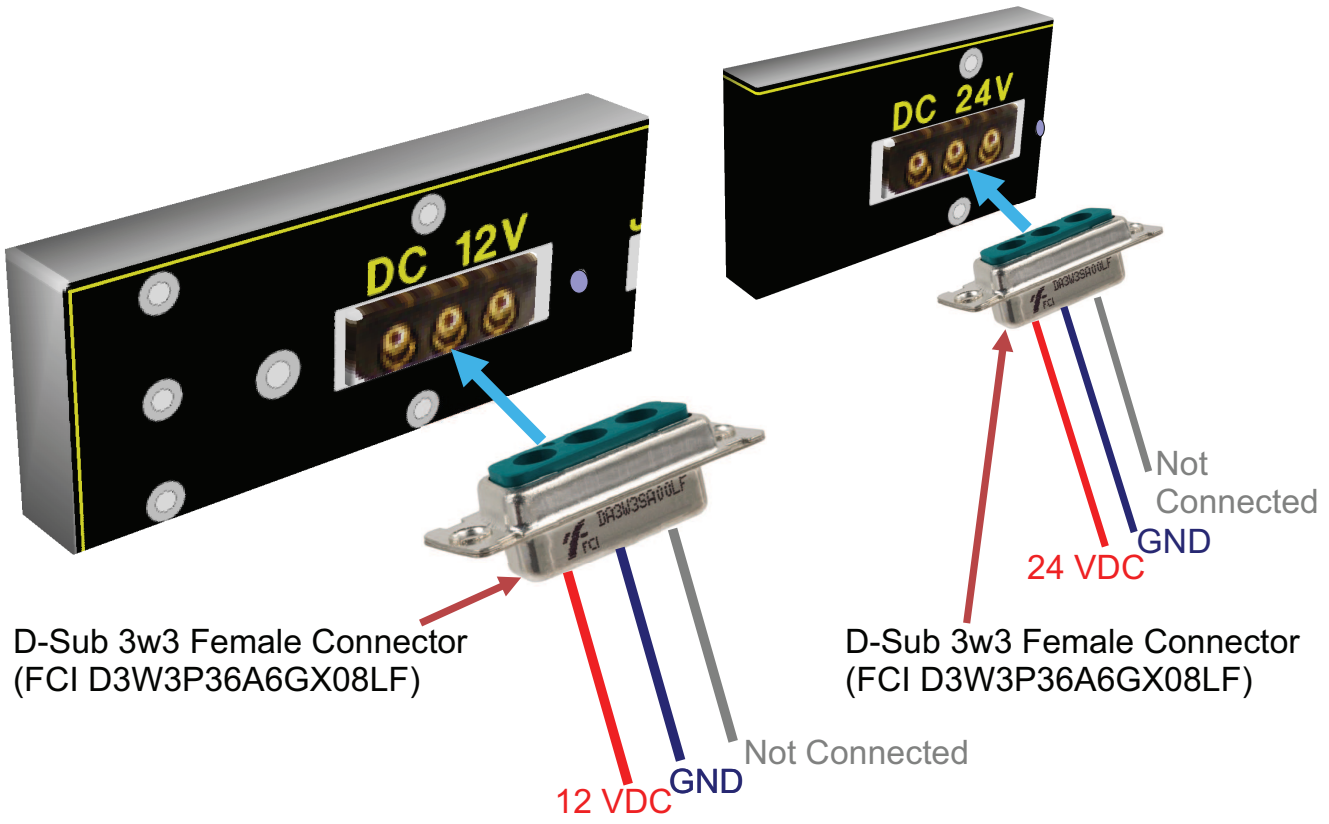
APPENDIX C. Lantronix UDS2100 Configuration for MFO

The picture below shows an example for Lantronix UDS2100 configuration. The UDS2100 module can be accessed and configured through the internet using its assigned IP address. Tthe IP address varies for every Lantronix module. One can obtain the IP address for a Lantronix module using the software given with it. See the Lantronix manual for further instructions.

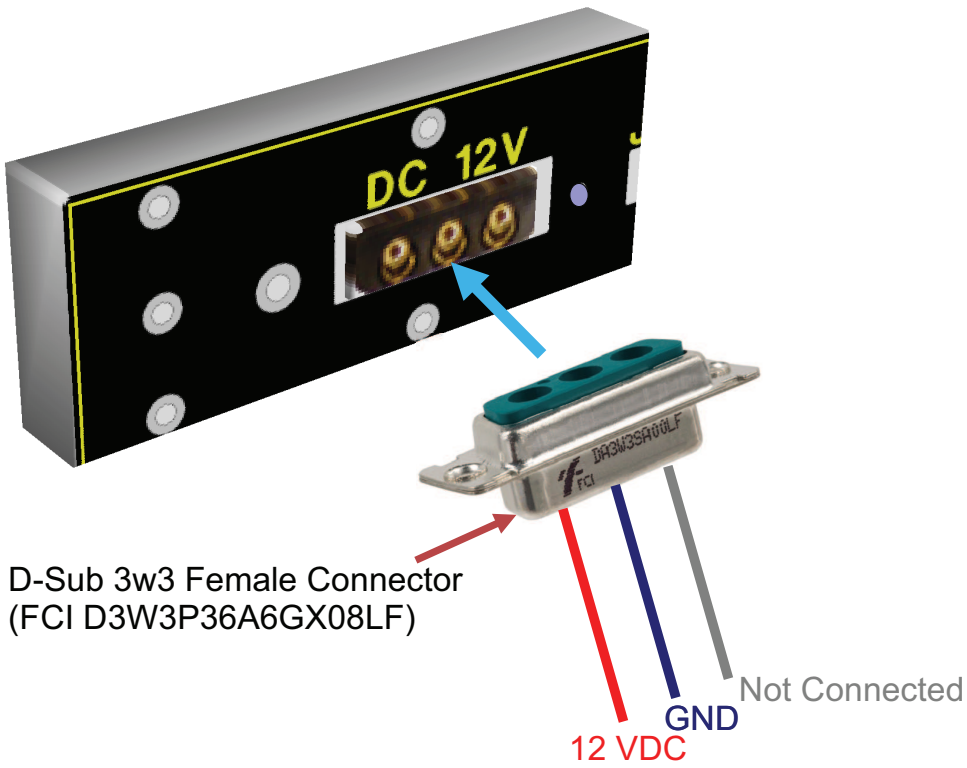



Lantronix Device Server - Mozilla Firefox
File Edit View History Bookmarks Tools Help
http://198.129.208.92/secure/ltx_conf.htm
Google
LANTRONIX
Firmware Version: V6.5.0.7
MAC Address: 00-20-4A-A2-DE-81
Network
Server
Serial Tunnel
Hostlist
Channel 1
Serial Settings
Connection
Channel 2
Serial Settings
Connection
Apply Settings
Apply Defaults
Connection Settings
Channel 1
Connect Protocol
Protocol: TCP
Connect Mode
Passive Connection:
Accept Incoming: Yes
Password Required: Yes No
Password:
Modem Escape Sequence Pass Through: Yes No
Active Connection:
Active Connect: None
Start Character: 0x 0D (in Hex)
Modem Mode: None
Show IP Address After RING: Yes No
Endpoint Configuration:
Local Port: 10001
Auto increment for active connect
Remote Port: 23
Remote Host: 0.0.0.0
Common Options:
Telnet Com Port Cntrl: Disable
Connect Response: None
Terminal Name:
Use Hostlist: Yes No
LED: Blink
Disconnect Mode
On Mdm_Ctrl_In Drop: Yes No
Check EOT(Ctrl-D): Yes No
Hard Disconnect: Yes No
Inactivity Timeout: 0 : 0 (mins : secs)
OK
Done

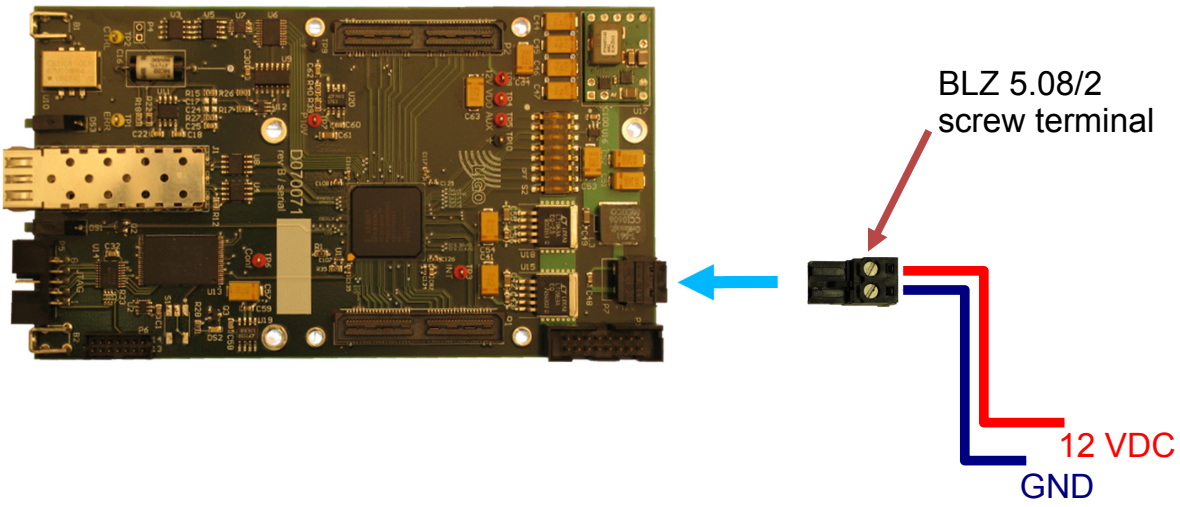
APPENDIX D. Visual Assembly Procedures.



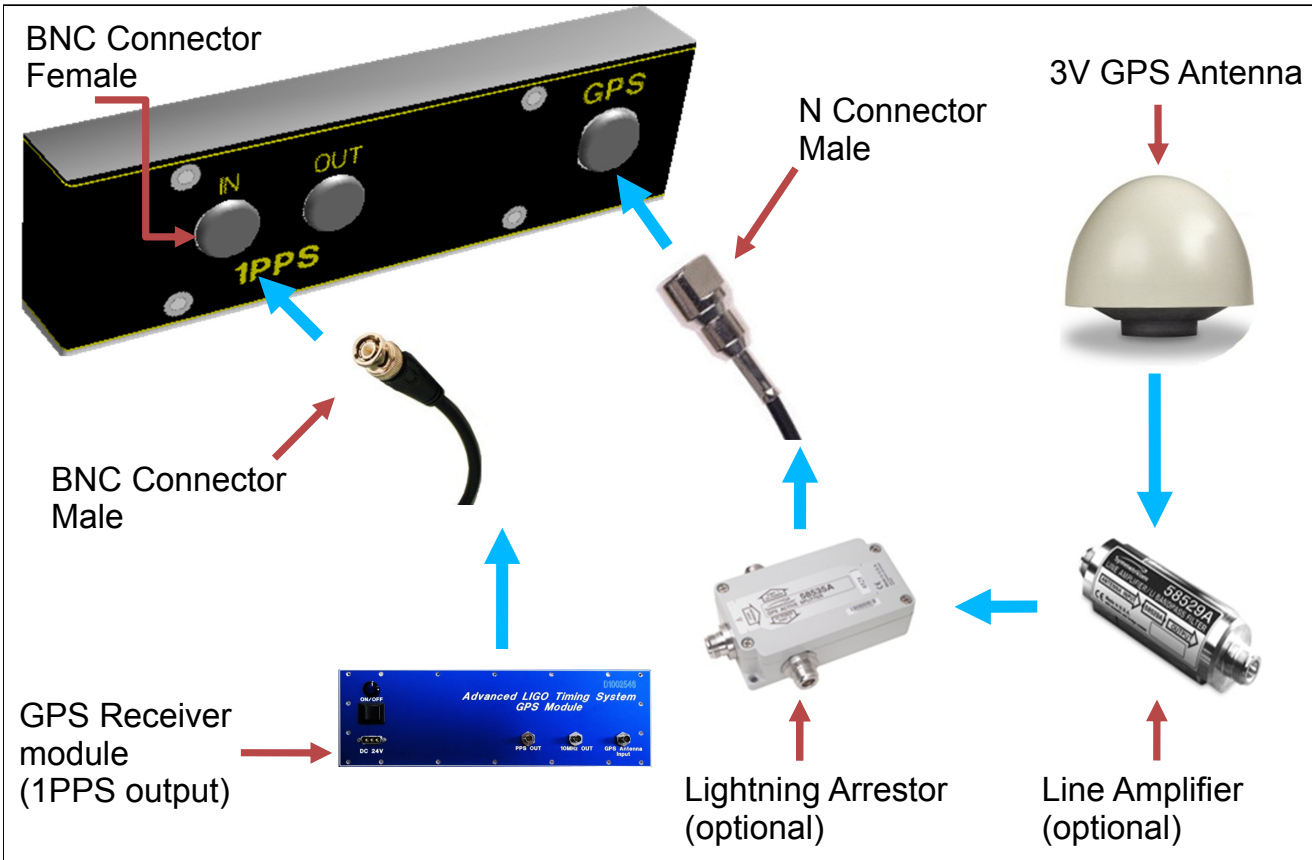
Step 1. Master board – connect VDC power supplies to the DC 12V (min 40W) and DC 24V (min 10W) connectors on the rear panel, respectively.



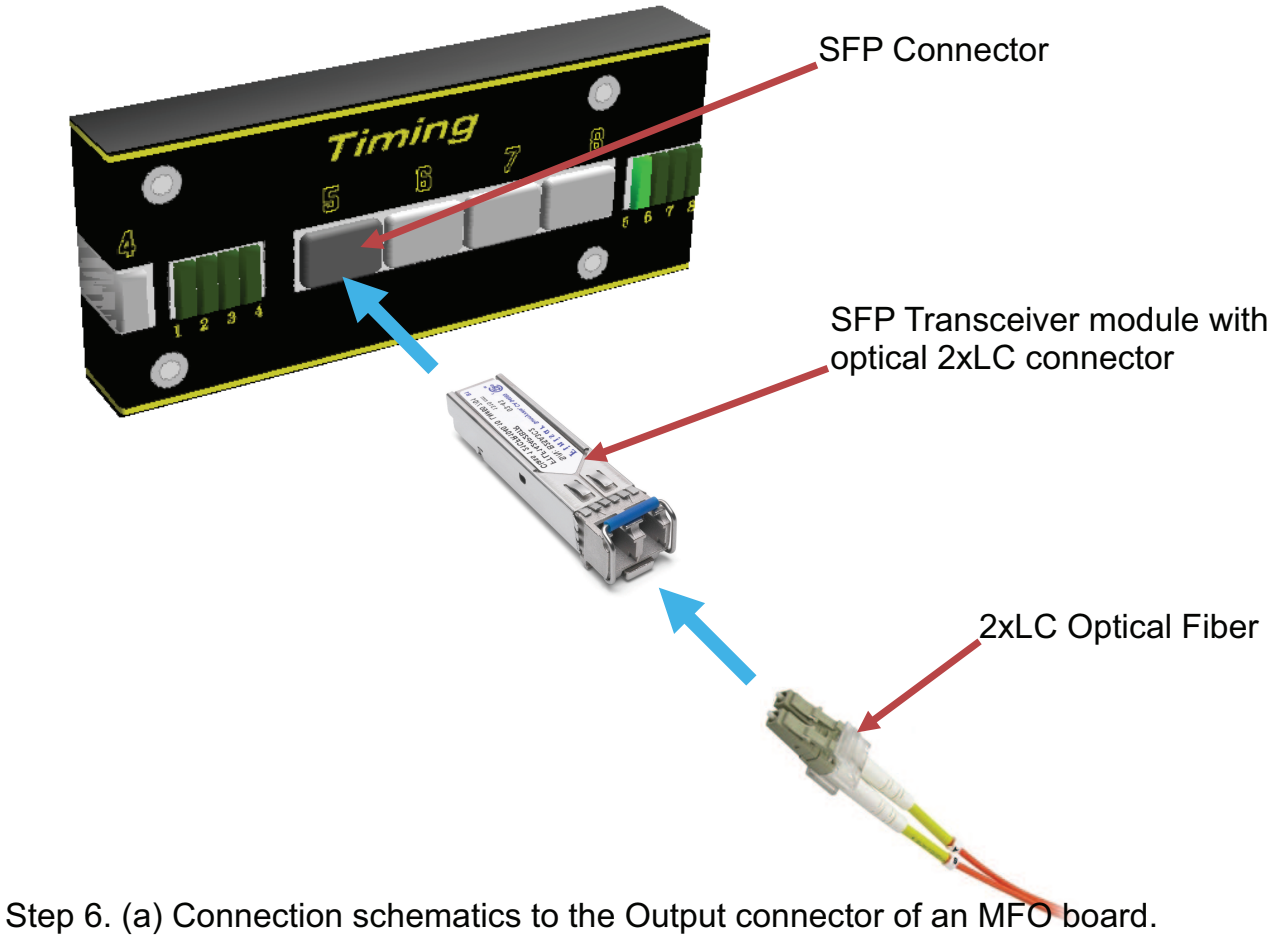
Step 2. FanOut board - connect 12 VDC (min 40 W) power supply to the DC 12V connector on the rear panel.



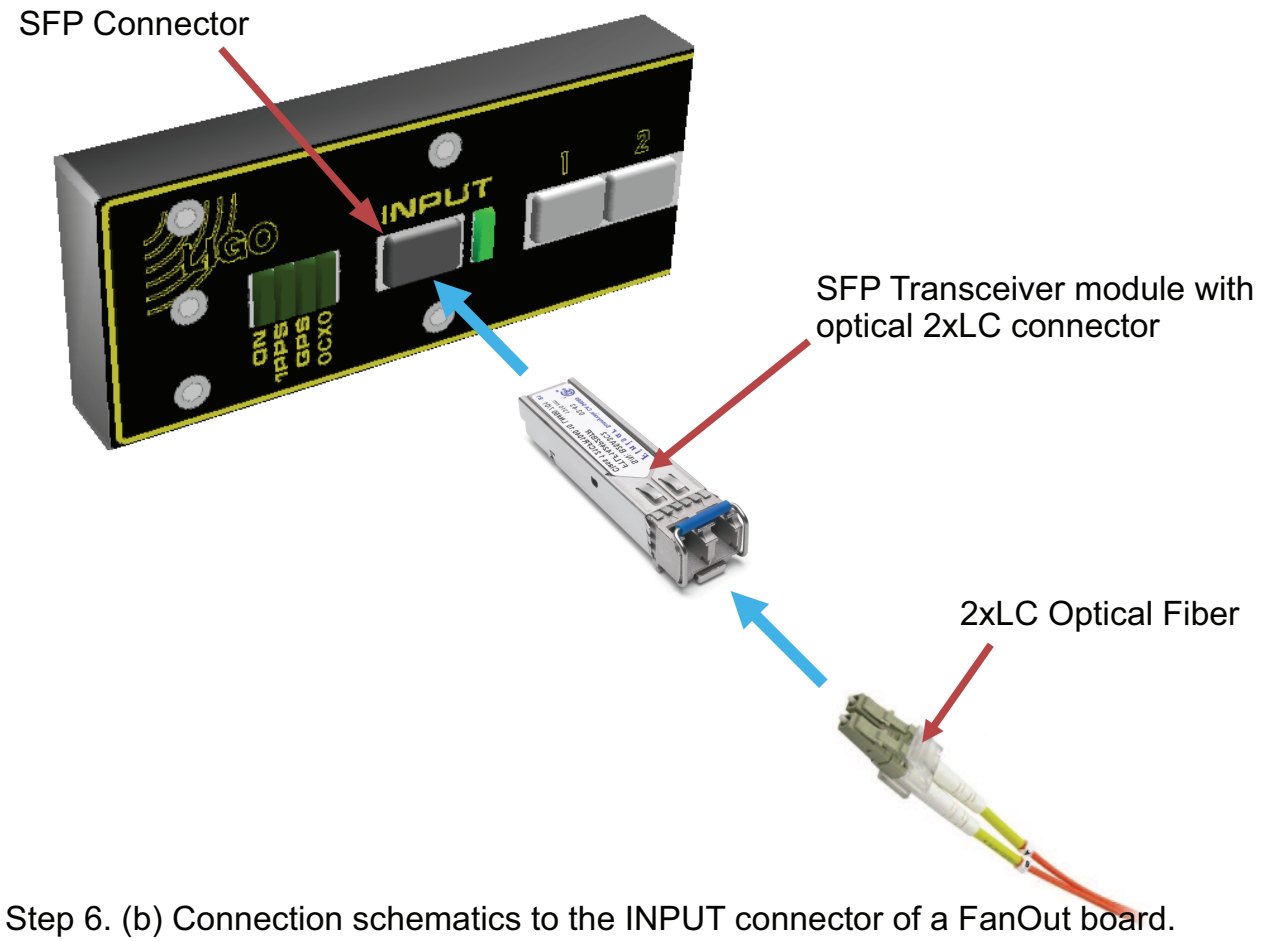
Step 3. Slave board - connect 12 VDC (min 15 W) power supply to the DC 12V connector on the rear panel.



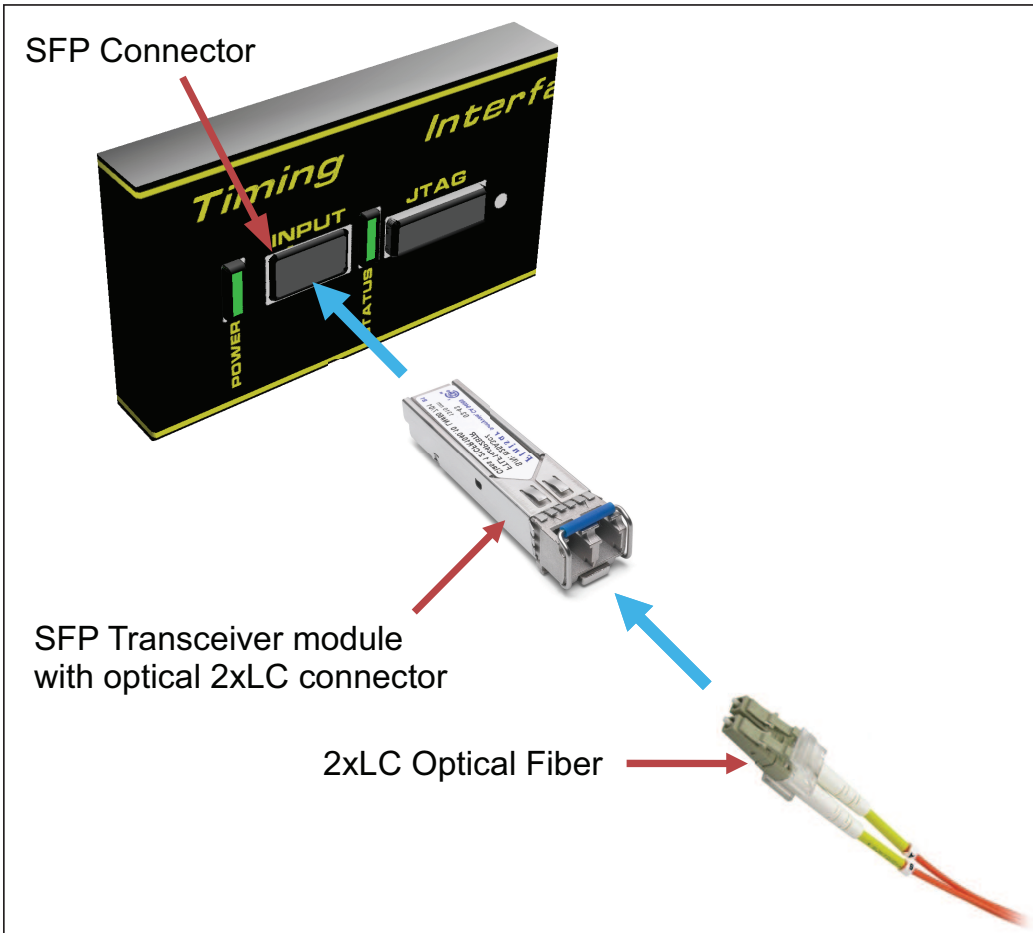
Steps 4. and 5. Master board: connect external 1PPS source, typically GPS receiver module [D1002546], to IN_1PPS connector. Connect 3V GPS antenna to the GPS connector (optionally through a GPS Lightning Arrestor and/or GPS Line Amplifiers).



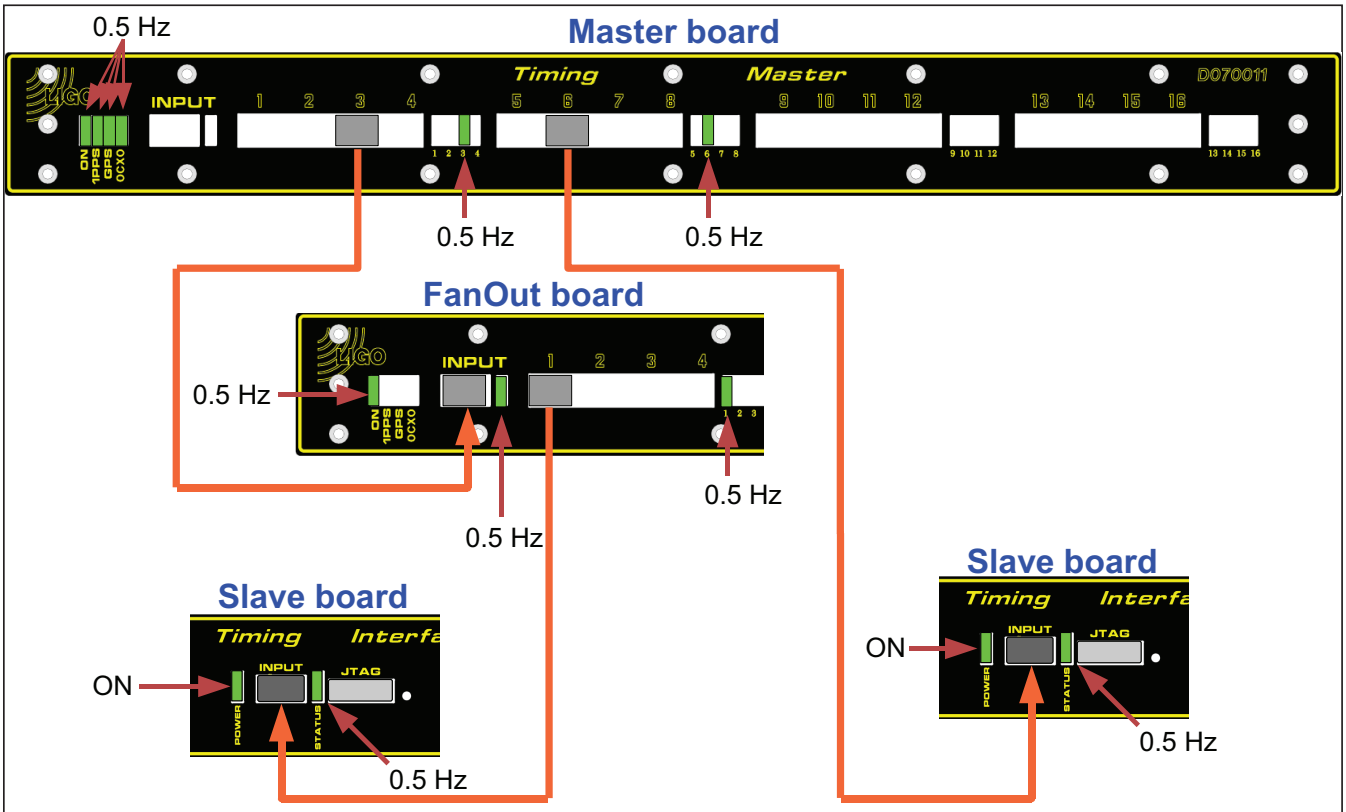
Step 6. (a) Connection schematics to the Output connector of an MFO board.



Step 6. (b) Connection schematics to the INPUT connector of a FanOut board.

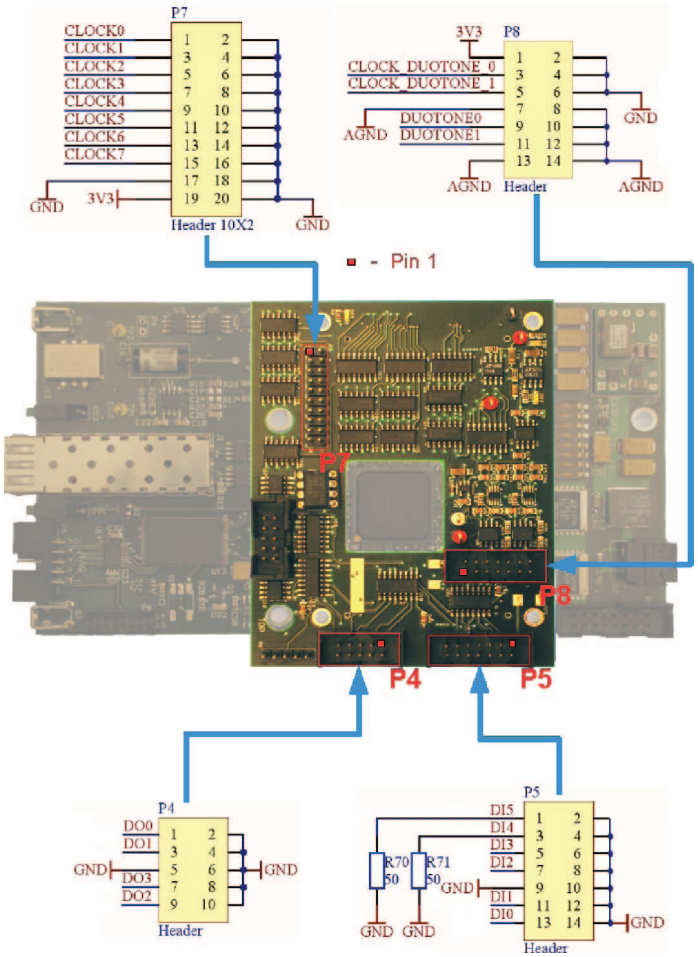


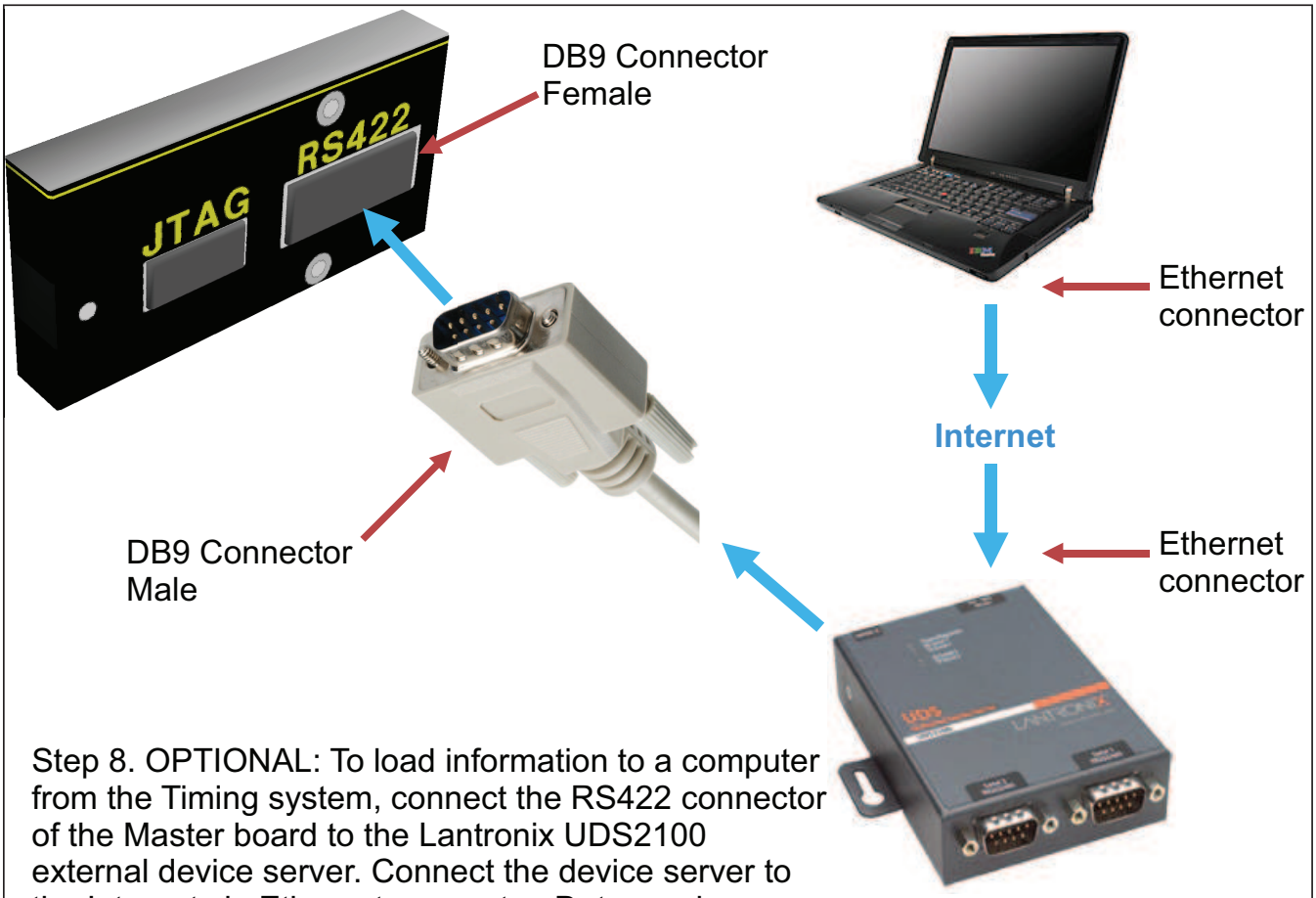
Step 6. (c) Connection schematics to the INPUT connector of a Slave board.



6. (d) Global connection overview: connect the INPUT connector of each FanOut and Slave board to the Output connector of the appropriate MFO to which the FanOut or Slave board will be synchronized. LEDs are shown for standard functioning. The above figure is an example for two connected Slave board. More FanOut and/or Slave boards can be connected.

Step 7. Connect DAC board I/O to the appropriate pins of the DuoTone board.

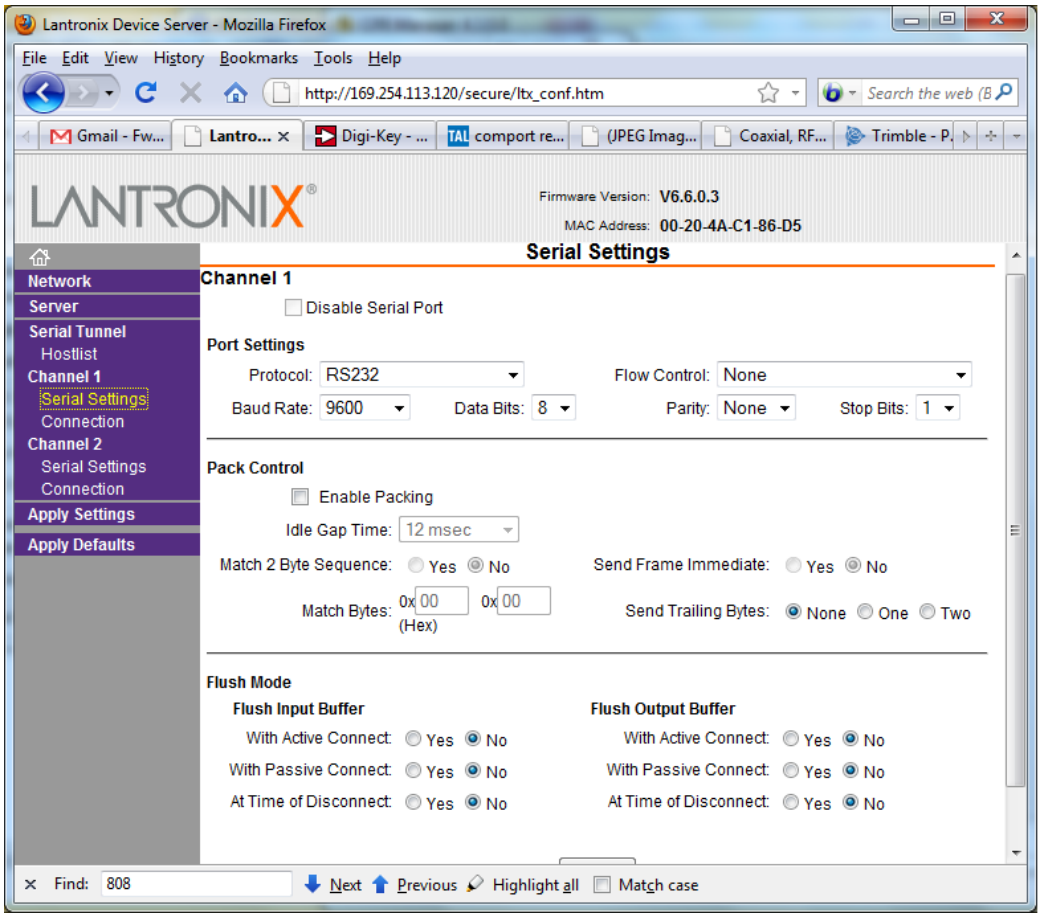


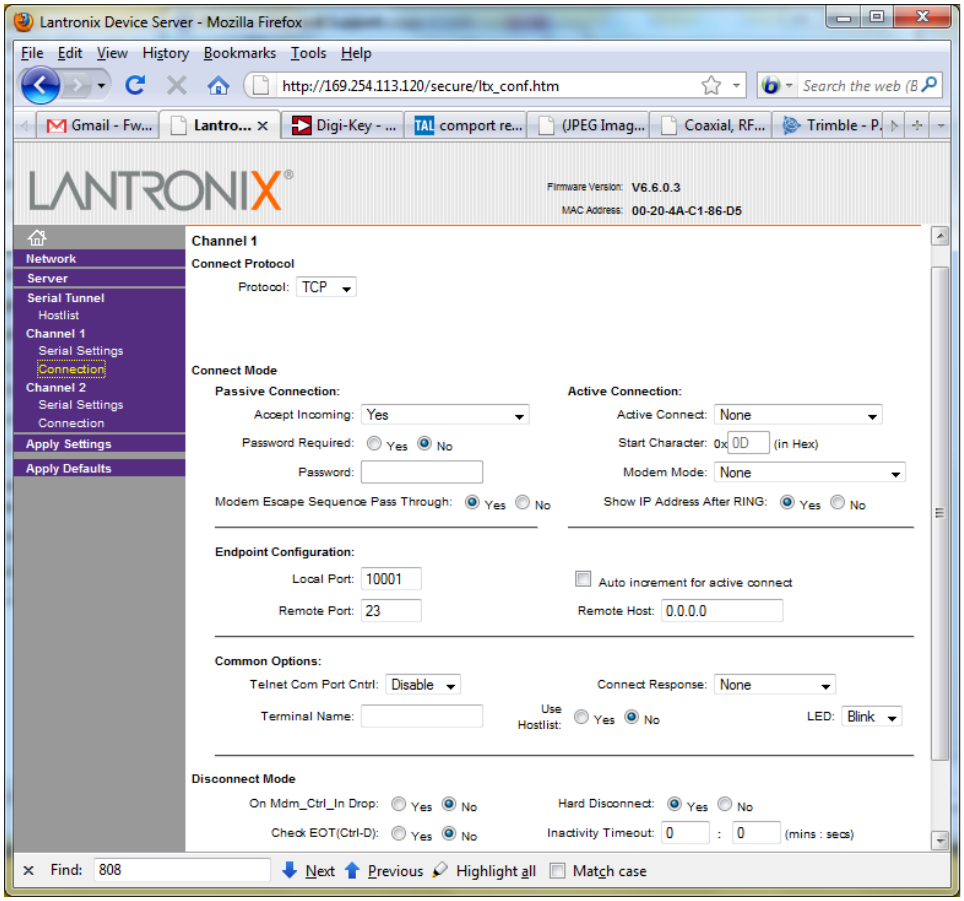


Step 8. OPTIONAL: To load information to a computer from the Timing system, connect the RS422 connector of the Master board to the Lantronix UDS2100 external device server. Connect the device server to the Internet via Ethernet connector. Data can be loaded to a computer via Internet.

APPENDIX E
Lantronix® UDS2100 Setup for Trimble ThunderBoltE GPS clock

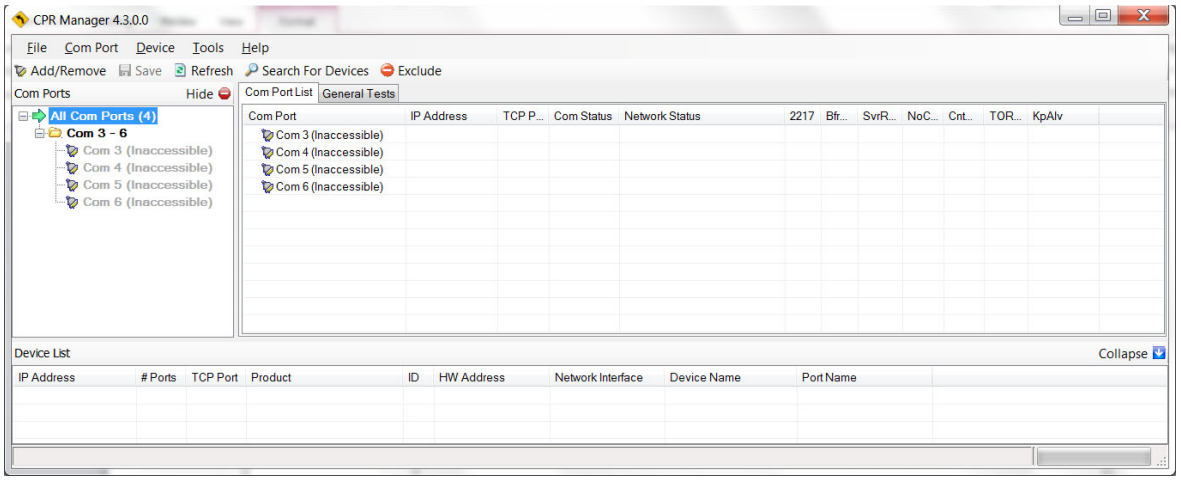
- First, note the assigned static IP address for Lantronix UDS2100. If it has not IP address assigned, please follow device installation procedure in section 3 (also see Lantronix® UDS2100 manual for further detail).
- The UDS2100 module can be accessed and configured through the internet using its assigned static IP address. The IP address should vary for every UDS2100 module. Please note the Lantronix settings for Trimble GPS communication on the picture below:



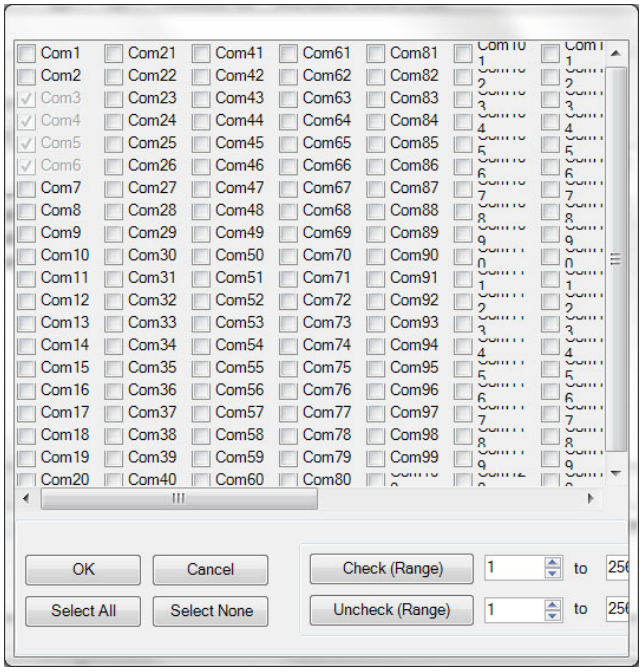


- Afterwards, you need to create a virtual COM serial port using **Lantronix® CPR Manager software**[1]:

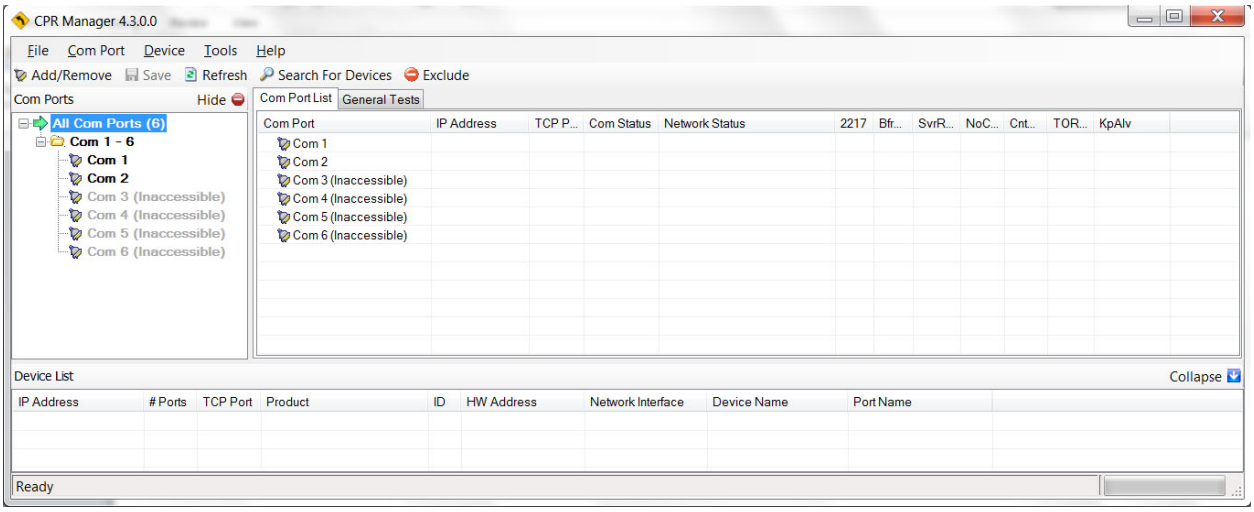
[1] All Lantronix® software can be downloaded from the Lantronix website: http://www.lantronix.com/support/downloads/



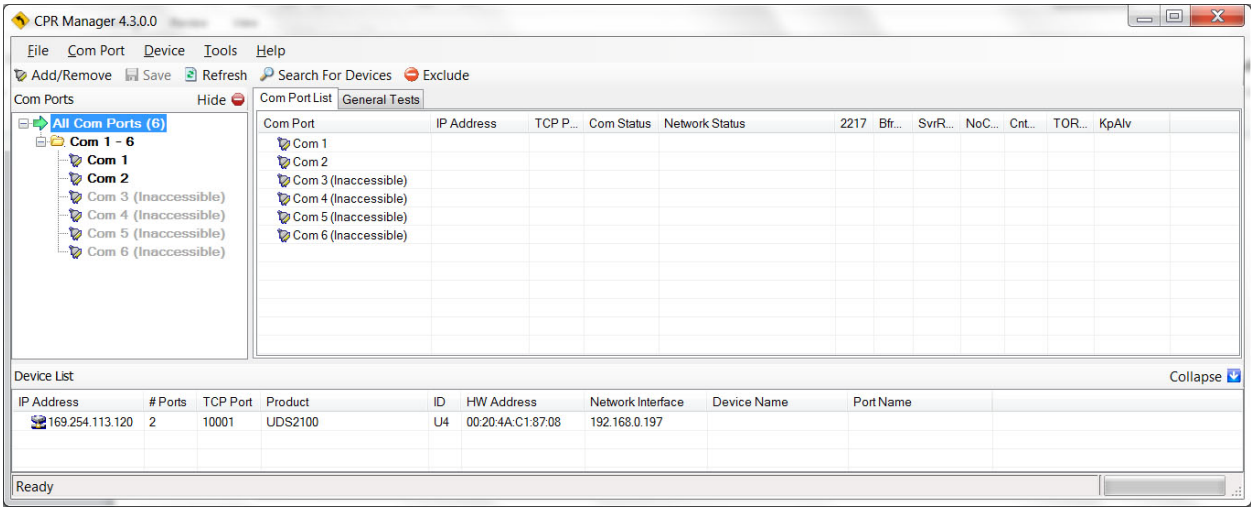
- Click on “Add/Remove” and check any available COM (e.g. Com1 and Com2) port; click “OK”:



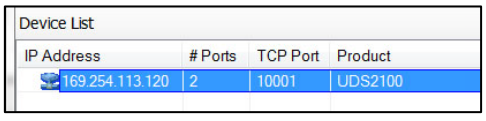
- Click on “Refresh”; confirm the changes by clicking on “Yes” and “Yes”;
- When the Refresh is done, restart the CPR Manager program. Now it should look like this (notice the appearance of new Com port(s)):



- Make sure that your UDS2100 is connected to the computer via Ethernet port or a router;
- Click on “Search For Devices”; after few seconds, the UDS2100 will appear in the Device List:

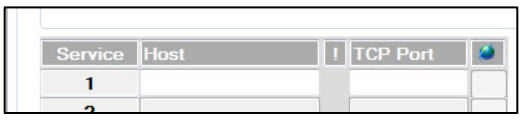


- Single-click on any new Com port in the Com Ports view; scroll the main view all the way down (you may also re-scale the program window, to allow viewing of all port settings);
- Click on “Add Rx Port” button; confirm the action by choosing “Yes”;
- Now go to the Device List view; drag the IP Address of the newly discovered UDS2100 to the available Host field, then click on refresh and confirm the action:



(drag here)

→→→→→



- You may now monitor your GPS receiver via newly created virtual serial port.