LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
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Technical Note **LIGO-E050262- 00- W** 09/04/08

Test procedure for the Timing Slave Board Advanced LIGO

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This is an internal working note
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Board document LIGO DCC # **070071**

Board Revision **B**

Board Serial # _____

Board Type **Slave**

Test Engineer _____

Test Date: _____

Overall MFO board testing: **PASSED** **FAILED**

Signature: _____

The following Test Procedure describes the test of proper operation of the Timing Slave board (LIGO-D070071, thereafter, Slave). Slaves provide 1PPS/UTC synchronous timing and diagnostic signals to external devices that are needed to be synchronized in different, possibly distant parts of the detector. The Slave receives 1PPS/UTC synchronous timing signal from a FanOut or Master upstream[1] (LIGO-D070011) that it synchronizes to.

In the Test Procedure, one will need to use a Test Daughterboard (LIGO-D080192) that will be attached to the Slave to facilitate the test of its connectors. At the start of the Test Procedure, the Test Daughterboard should NOT be attached to the Slave. In the Test Procedure, ground will be denoted with GND. Measured voltages on the Slave or Test Daughterboard should be referenced to GND, which is available on test points TP9 and TP10 on the Slave and TP1 on the Test Daughterboard.

1) Verify the proper current draw. Using a bench DC power supply apply +12V to the *Slave*. Connect +12V to port 1 of the SL 5.08/2 screw terminal and GND to port 2 (note that there is a '*+12V*' marking next to port 2, but the +12V should be connected to port 1). Measure the current draw of the board. Check if the power LED (DS3) is ON after you apply the voltage.

+12V at < 430 mA Measured_____ mA Pass Fail

Power LED is on. Yes No

[1] In some cases, the *Slave* board might be directly connected to the *Master*, or there might be several *FanOut* boards serially connected between the *Master* and the *Slave*.

2) Verify that the power supply rails are at the correct voltages. Measure the voltages at the following test points. If any of these indicators of proper operation are not present the problem must be fixed before proceeding with the test.

TP8 (12V), +12V ± 5% Measured _____ V Pass Fail

TP4 (VDD), +3.3V ± 5% Measured _____ V Pass Fail

TP5 (AUX), +2.5V ± 5% Measured _____ V Pass Fail

TP3 (INT), +1.2V ± 10% Measured _____ V Pass Fail

TP6 (Conf), +1.8V ± 10% Measured _____ V Pass Fail

TP7 (P10V), +10V ± 5% Measured _____ V Pass Fail

3) Check if the JTAG connector works properly. Connect the JTAG Interface to the JTAG connector of the *Slave*. Program the *Slave* with the *FGPA_SLAVE_TEST* program. In the Altium Designer program, open the digital I/O unit called U_Test. In the upper left corner of the window, the JTAG variable is should be 0 if the program has loaded properly.

JTAG connector works properly. Yes No

For the following tests the FGPA_SLAVE_TEST program should be loaded onto the Slave board, and the Slave should be connected to a FanOut (or Master) board with 2xLC optical fiber. The optical fiber should be connected to the SYNCIN connector (J1) of the Slave through an SFP Transceiver module with optical 2xLC connector. This transceiver module is removable and should be placed in the SFP connector of the board.

4) Verify the proper operation of HF PLL. Using a Voltmeter, measure the voltage on the Control Mon output TP2 (CTRL). With no SYNCIN signal, the control voltage should be at the negative rail, which is 0V, indicating that the loop is unconnected. The 1PPSIN LED (DS1) should be off. Now connect the optical fiber with the SYNCOUT signal from the *FanOut* (or *Master*) to the SYNCIN connector (J1). First, the 1PPSIN LED (DS1) should be ON for 250 ms and OFF for the next 250 ms (thereafter, *'2 Hz blink'*), indicating that the board receives the SYNCIN signal, but it is not locked to the *FanOut* (or *Master*) yet. After locking, the LED will be ON for one second and OFF for the next second (thereafter, *'½ Hz blink'*). For this part of the Test, exhibiting *2 Hz blink* or *½ Hz blink* are both acceptable. If HF PLL is locked, the control voltage will no longer be railed and should be roughly 5V. Record the locked control voltage. Also check if the power draw of the *Slave* has changed significantly due to the connection of the optical fiber (a significant change shows improper operation - some components are probably shorted).

TP2 (locked, connected fiber) at 5V ± 1V Measured _____ V Pass Fail
TP2 (locked, disconnected fiber) at 0V ± 0.1V Measured _____ V Pass Fail

+12V at < 430 mA Measured _____ mA Pass Fail

1PPSIN LED works properly (exhibits either *2 Hz* or *½ Hz blink*). Yes No

5) Write down the value of the VCXO Control ADC and compare with the analog readback. In Altium Designer, open the U_Test digital I/O of the *FGPA_SLAVE_TEST* program. Compare the value of the variable VCXO_CONTROL[15..0] (shown with decimal numbers) with the Control Mon output TP2 (CTRL) on the *Slave*. The value of VCXO_CONTROL[15..0] can be converted to Volts with the following formula:

$$V\_OCXO\ [V] = VCXO\_CONTROL[15..0] \ / \ 65536.$$

If the ADC works properly, V_OCXO and TP2 should be roughly equal. Check it for the cases of connected and disconnected optical fiber separately.

V_OCXO (connected fiber)	Measured_____V	Pass	Fail
V_OCXO (disconnected fiber)	Measured_____V	Pass	Fail
ADC works properly.		Yes	No

6) Verify the synchronization of the 1PPS signal. Connect the 1PPS OUT output (J8) of the *FanOut* (or *Master*), and pins 15 (SYNCLK_P), and 16 (SYNCLK_N) of the P3 header of the *Slave* to an oscilloscope using 50 Ohm termination, and trigger on the signal from the *FanOut* (or *Master*). Each monitor output should be putting out a positive going, 10µs wide 1PPS signal. The 1PPS signal from the *Slave* should be properly synchronized, i.e. its leading edge should match the leading edge of the 1PPS signal from the *FanOut* (or *Master*) within ± 60ns. The synchronization should disappear when the link between them is disconnected. If the 1PPS signals are synchronized, the SYNCOUT and SYNCIN LEDs on the *FanOut* (or *Master*) and the *Slave*, respectively, should exhibit *½ Hz blink*. If the 1PPS signal is not synchronized but the boards are connected, the LEDs on both boards should exhibit *2 Hz blink*. If there is no 1PPS signal present, but the boards are connected, the LED is constantly ON.

1PPS signal is synchronized.	Yes	No
SYNCIN LED on the *Slave* exhibits *½ Hz blink*.	Yes	No

7) Test the P3 header of the *Slave*. Pins 1-8, 10, 12 and 14 should be tested with a Voltmeter. Their outputs should be the following:

2, 4, 6, 8, 10, 12, 14:	GND
1, 3:	+12V
5, 7:	+3.3V

Measure pin 9 with an Ohmmeter. It should be toggling between shorted and non-conducting states each second (grounded for a second and then non-conducting for the next second). In 5) pins 15 and 16 were already tested.

P3 header on the Slave works properly.	Yes	No

For the following tests, the Test Daughterboard should be placed onto the Slave board and the FPGA_SLAVE_TEST program should be installed.

7) Test the S[64..1] ports on the *Slave* board. In the *FGPA_SLAVE_TEST* program, every even port (i.e. S2, S4, etc.) is output, while every odd port is input. The outputs are all HIGH for one second and then LOW for the next second. The *Test Daughterboard* connects the even ports to the odd ports: even port S[2n] is connected to odd port S[2n-1]. In Altium Designer, open the digital I/O unit U_Test of the *FGPA_SLAVE_TEST* program. The states of the S[64..1] ports are shown by LEDs:

S[16..1] => S_A[16..1],
S[32..17] => S_B[16..1],
S[48..33] => S_C[16..1],
S[64..49] => S_D[16..1].

If the *Test Daughterboard* and the ports work properly, all LEDs should exhibit *½ Hz blink*. Note that sometimes it is difficult to properly place the *Test Daughterboard*, therefore it might not connect all 64 ports properly. If some of the ports do not connect, try to re-seat the *Test Daughterboard* before concluding that some ports do not work.

S[64..1] ports work properly. Yes No

8) Test the DIP-8 socket on the *Test Daughterboard* with a scope. Test each pin except pin 2 with a Voltmeter. Their outputs should be the following:

1, 5, 6: *½ Hz* toggling (HIGH for a second and then being LOW for the next second)
3, 7, 8: HIGH
4: LOW

Check if the input pin, pin 2, works properly. Turn on the U_Test digital I/O in the Altium Designer. The LED called CFG_SI should be OFF since there is no input. Now connect pin 2 with pin 1: CFG_SI should exhibit *½ Hz blink*.

DIP-8 works properly. Yes No

9) Test switches 1 to 8 on the *Slave* and switches 1 and 2 on the *Test Daughterboard.* In Altium Designer, open the U_Test digital I/O of the *FGPA_SLAVE_TEST* program. The SW[10..1] bus gives the SW inputs. SW[8..1] represent the switches located on the *Slave*, while SW9 and SW10 correspond to Switch2 and Switch1, respectively, on the *Test Daughterboard*. If SW9 and SW10 are not pressed, the corresponding values in the digital I/O should be HIGH. If the switches are pressed, these values should go LOW as long as the switches are pressed. The values of SW[8..1] can be set manually with the S2 unit on the *Slave*. On S2 you find eight switches that can set the values of these switches to HIGH or LOW. Test if these switches induce the desired changes in the SW[8..1] values as seen on the digital I/O unit. Note that, if these switches have not been used before, they have a thin safety cover on them that has to be broken in order to be able to use the switches.

Switches 1 to 8 on the *Slave* work properly. Yes No

Switches 1 and 2 on the *Test Daughterboard* work properly. Yes No

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